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doi: 10.35848/1347-4065/ab79f0

Capacitance extraction method of a free-standing bilayer lipid membrane formed over an aperture in a nanofabricated silicon chip

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A bilayer lipid membrane (BLM) is a main component of a cell membrane of living organisms, which can be formed artificially. Although a specific capacitance of a BLM is known to be in the range of 0.4 – 1.0 μF cm^{-2}, many previous works forming free-standing BLMs over an aperture in silicon chips reported larger values beyond this typical range, which suggests that the equivalent circuit models are not adequate. In this work, we modified the equivalent circuit model by adding a resistance element of silicon. To evaluate the validity of the modified model, we applied the model to the results of electrochemical impedance spectroscopy (EIS) for free-standing BLMs formed over an aperture in nanofabricated silicon chip. The derived specific capacitance values were 0.57 ± 0.08 μF cm^{-2}, which was settled in the typical range.

1. Introduction

The human body comprises of several cells. The main component of cell membranes is a double layer of phospholipids. Phospholipids bilayers can be formed artificially and are expected to be applied for not only pharmaceutical products as well as electronics components. Among many forming methods, a membrane formed over an aperture is referred to as a free-standing bilayer lipid membrane (BLM). BLMs were formed over an aperture in Teflon films in early days;[1)] now there are many reports about BLMs formed on various platforms such as a porous alumina,[2,3)] an indium tin oxide (ITO),[4)] and so on.[5,6)] Especially, a silicon chip has an advantage in utilization of micro-nano-fabrication technologies. As examples of experiments using micro- and nano-fabricated silicon chips,[5,6)] ion-current recordings of cell-free-synthesized hERG channels embedded in a BLM[7,8)] and photomodulation of electrical conductivity of a PCBM-doped BLMs[9)] have been reported.

BLM capacitances per unit area (specific capacitances) have been reported to be in the range of 0.4 – 1.0 μF cm^{-2} in many previous works.[1-4,10-16)] To determine the specific capacitance of a BLM, time-domain measurements[1,6,16,17)] (triangle waveform sweep, transient response) and frequency-domain measurement[3-5,10-13,15,18-24)] (electrochemical impedance spectroscopy: EIS) are often conducted. No matter what kind of measurement method is used, however, to determine the specific capacitance, experimental results are analyzed using the equivalent circuit of the system. Historically, specific capacitances of BLMs formed over an aperture in Teflon films were determined within the typical range (0.4 – 1.0 μF cm^{-2})[1)], whereas those in silicon chips were often reported to be larger values than 1.0 μF cm^{-2}.[17-22)] Since experiments were successful for both Telfon and silicon platforms, fault derivation for silicon chips were supposed to originate from equivalent circuits.

In this work, in order to determine the specific capacitances of BLMs formed over an aperture in nanofabricated silicon chips, we modified the equivalent circuit model, and conducted series experiments. We determined the parameters of the modified equivalent circuit, in which both capacitance and resistance of the silicon chip were included, by analyzing EIS results. In addition, we measured triangle waveform responses and compared them with circuit simulation of the equivalent circuit. Below we describe the validity of the modified circuit model both in the frequency- and time-domain. Determination of the BLM capacitance and resistance is also presented.

2. Experimental methods

Figure 1 shows our experimental setup with detailed illustrations and photomicrographs. A

nanofabricated silicon chip was placed between two Teflon chambers as shown in Fig 1(a). Figure 1(b) shows detailed design of the silicon nanofabricated chip and a free-standing BLM. The fabrication process of an aperture in silicon chips was described in Refs. 7, 8, and 25. Figure 1(c) shows optical photomicrographs of apertures in two silicon chips. The aperture areas (S_{ap}) of Chips A and B are 4910 and 1980 μm^2, respectively. Figure 1(d) shows stereo microscope images of the Teflon chambers and the nanofabricated silicon chip sandwiched in between. The area of the silicon chip (S_{CHIP}) contacting with buffer solution is 3.14 mm^2. Teflon chambers with a nanofabricated silicon chip were placed in a Faraday cage on an anti-vibration table as shown in Fig. 1(e).

1,2-diphytanoyl-sn-glycero-3-phosphocholine (DPhPC) bilayer was formed by using Montal-Mueller's method[1]. Firstly, the buffer solution of 2 M KCl mixed with 5 mM HEPES was poured in both wells (1400 μl). Then, the buffer solution levels were lowered by operating syringes via Teflon tubes. Next, 5 mg ml^{-1} solution of DPhPC (the solvent: chloroform / *n*-hexane, 1:1) was dropped in both wells. After the evaporation of the solvent, the buffer solution levels were raised slowly; a free-standing BLM was finally formed over an aperture in the nanofabricated silicon chip. Electrical measurements were conducted via silver-silver chloride electrodes. EIS was conducted with a chemical potentiostat (Bio-Logic, SP-200) in the frequency range from 3 MHz to 1 mHz with the input voltage of 70.7 mV$_{peak}$. Triangle waveform response was measured with a function generator (Tektronix, AFG3252), a low noise current preamplifier (Stanford Research Systems, SR570), and an oscilloscope (Rohde & Schwarz, RTB2004). The amplitude and frequency of the triangle waveform were respectively set at 100 mV$_{p\text{-}p}$ (high level: 50 mV, low level: –50 mV) and 5 kHz.

EIS results were analyzed by using an equivalent circuit modeling software (ZView®, Scribner Associates), by which circuit parameters were determined. Then, triangle waveform response was simulated with the derived parameters by using an electronic circuit simulator (LTspice®, Linear Technology) and compared with the experimental results of triangle waveform responses.

3. Capacitance extraction method

3.1 Triangle waveform simulation

Under certain restrictions, a BLM capacitance can be extracted by using triangle waveform sweep[6,16]. This method is based on the theory that constant current I_{out} is observed for the slope of a triangle waveform voltage applied to a capacitor. That is, I_{out} is expressed as

$$I_{\mathrm{out}} = \frac{\mathrm{d}q}{\mathrm{d}t} = \frac{\mathrm{d}(C_{\mathrm{triangle}}V_{\mathrm{in}})}{\mathrm{d}t} = C_{\mathrm{triangle}}\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} = 2V_{\mathrm{p-p}}f_{\mathrm{in}}C_{\mathrm{triangle}}. \quad (1)$$

Here, q is the charge on the capacitor, C_{triangle} is the capacitance, V_{in} is the applied input voltage. $\mathrm{d}V_{\mathrm{in}}/\mathrm{d}t$ of the gradient of a triangle can be transformed as $2V_{\mathrm{p\text{-}p}}f_{\mathrm{in}}$, where $V_{\mathrm{p\text{-}p}}$ is the amplitude, and f_{in} is the frequency ($V_{\mathrm{p\text{-}p}}$ = 100 mV, f_{in} = 5 kHz). The capacitance C_{triangle} can be calculated from the constant current I_{out} and the known values of $V_{\mathrm{p\text{-}p}}$ and f_{in}. This method is quite effective in case of BLMs formed on insulative platforms such as a Teflon film,[1] a porous alumina,[2-3] and other insulative ones[6,16] for which a BLM can be simplified to a resistor-capacitor parallel model; when a BLM resistance is sufficiently high, the circuit model can be further simplified as a single capacitor.

Figure 2(a) shows a resistor-capacitor parallel model (Circuit 1, C_1 = 20 pF and R_1 = 1 TΩ). A triangle waveform simulation result for Circuit 1 is presented in Fig. 2(c) as a dashed curve. In simulation, ($\mathrm{d}V_{\mathrm{in}}/\mathrm{d}t$) at the slope was set at ±1000 V/s (0.1V/100μs). The constant value of I_{out} was ± 20 nA, by substituting these values into Eq. (1), C_{triangle} becomes 20 pF, which agreed with the configured value of C_1 of 20 pF. Contrary, if a platform is not insulative, a circuit model becomes more complicated with the capacitance C_2 and resistance R_2 of the platform, which is shown in Fig. 2(b) (Circuit 2, C_1 = 20 pF, R_1 = 1 TΩ, C_2 = 100 pF, and R_2 = 100 kΩ). Figure 2(c) presents a triangle waveform simulation result for Circuit 2 as a thick solid curve. As can be seen, the observed current is distorted, whereas the constant current value is increased to 120 nA; the calculated capacitance C_{triangle} using Eq. (1) becomes the sum of two parallel capacitances ($C_{\mathrm{triangle}} = C_1 + C_2$ = 120 pF). As the circuit model becomes more detailed, the triangle waveform method with Eq. (1) cannot be used. Therefore, to divide the parallel capacitance, another method is required.

3.2 EIS and equivalent circuit analysis

In this work, we took advantage of EIS and equivalent circuit analysis employed in many previous works.[3-5,10-13,15,18-24] Figure 3(a) shows an equivalent circuit for a BLM and a silicon chip having been used.[18-24] It is found that no resistance element of a silicon chip is included. Actually, although our previously proposed model succeeded to reproduce experimental model precisely, it was impossible to extract BLM capacitance because it did not take characteristics of a silicon chip into consideration.[26] Figure 3(b) shows a schematic illustration of a nanofabricated silicon chip with our modified equivalent circuit including the resistance of the silicon chip. As shown in Fig 1(b), the silicon body is covered by a Si_3N_4 layer and a CYTOP® layer. (The insulative CYTOP® layer is employed to reduce current

noise.[27]) The model shown in Fig. 3(b) is then finally employed in the whole circuit model between two Ag/AgCl electrodes as shown in Fig. 3(c). The parallel R_{BLM} and C_{BLM} correspond to the BLM resistance and capacitance respectively. The series R_{CHIP} and C_{CHIP} correspond to the silicon chip's resistance and capacitance respectively [Fig 3(b)]. The parallel R_{EDL} and Q_{EDL} are electrical double layer (EDL) parameters; the Q_{EDL} is known as a constant phase element (CPE).[5,11,19,20,28-30] The CPE reproduces the impedance of an EDL, which is written as

$$Z_{CPE} = \frac{1}{(j\omega)^{\alpha} Q_{EDL}}. \quad (2)$$

Here, α is a constant value which moves in the range from 1 to 0. When $\alpha = 1$, it behaves as a capacitor, while $\alpha = 0$, it behaves as a resistor. The parameter of Q_{EDL} has a complex unit of F $s^{\alpha-1}$, where F is Farad, and s is second. The effective capacitance C_{EDL} can be calculated with the EDL parameters of R_{EDL} and α, which is written as

$$C_{EDL} = Q_{EDL}^{1/\alpha} R_{EDL}^{(1-\alpha)/\alpha}. \quad (3)$$

The parallel R_M and C_M correspond to the parasitic parameters of our experimental setup. The R_S corresponds to the series resistance, most of which is occupied by an access resistance[31,32] around the aperture in the nanofabricated silicon chip. The access resistance is expressed as

$$R_{ac} = \frac{1}{2\kappa r}. \quad (4)$$

Here, κ is the conductivity of the buffer solution ($\kappa = 0.23$ S cm^{-1}, 2 M KCl), and r is the radius of the aperture [Fig. 1(c)].

4. Results and discussion

4.1 Equivalent circuit fitting and evaluation

Figure 4(a) shows examples of EIS using Chip A and fitting results, in which the modulus and phase angle of impedance are plotted as functions of frequency, whereas Fig. 4 (b) shows an equivalent circuit model with the parameters obtained by fitting. The fitting curves agree well with the experimental results.

We conducted seven experiments in total (Chip A, $n = 7$). Membrane resistances R_{BLM} were extracted within a wide range from 12.2 GΩ to 7.00 TΩ, which are sufficiently high values to observe channel recordings. The maximum resistance of 7.00 TΩ (and its normalized value of R_{BLM} S_{ap} = 344 MΩ cm^2) obtained in the series experiments is higher than the values reported in previous works.[1,3-5,10-13,18-24,33,34] Such a high membrane resistance indicates that the micro- and nano-tapered apertures fabricated in silicon chips

enhance not only the mechanical stability but also the electrical resistance of BLMs. Notably, previous researches forming free-standing BLMs, membrane resistances over apertures in silicon chips reported BLM resistances as high as 4.7 GΩ (160 MΩ cm^2, DPhPC),[3] 157 GΩ (12.3 MΩ cm^2, POPC),[17] 74 GΩ (6.0 Ω cm^2, DPPE / DPPS),[19] 53.6 GΩ (0.96 MΩ cm^2, DPhPC);[20] membrane resistances appear to be dependent on not only lipid molecules but also platform's micro- and/or nano-structures.

Membrane capacitances C_{BLM} were obtained as 28 ± 4 pF. The specific capacitance calculated by C_{BLM} / S_{ap} (S_{ap} = 4910 μm^2 is the aperture area of the nanofabricated chip [Fig. 1(c)]) was 0.57 ± 0.08 μF cm^{-2}. This value falls within the range of 0.4 – 1.0 μF cm^{-2} that have been reported in previous works.[1-4,10-16]

The resistance of the silicon chip R_{CHIP} was extracted as 92 ± 15 kΩ. Then, the resistivity of the chip can be calculated as follows:

$$\rho \simeq \frac{S_{CHIP}}{l} R_{CHIP}. \quad (5)$$

Here, S_{CHIP} of 3.14 mm^2 is the area of the nanofabricated silicon chip [Fig. 1(d)], l is the thickness of the silicon layer [Fig. 1(b)]. By using the Eq. 5, the resistivity of the chip becomes 1.4 ± 0.2 kΩ m, which agrees with the resistivity of high purity silicon crystal. The capacitance of the silicon chip C_{CHIP} was extracted as 0.96 ± 0.74 nF. The relatively large deviation in C_{CHIP} was likely to attribute to the deviation in the spectra in low frequency (< 1 Hz) regions, where relatively long time was necessary for measurements, and hence, external noise and time evolution of BLM characteristics could be included. In addition, the chip surface modified and covered with a silane coupling agent and CYTOP® layer [Fig. 1(b)] was gradually changed, resulting in variation of C_{CHIP}.

R_S was extracted as 1.0 ± 0.4 kΩ, which is slightly higher than the calculated access resistance of 0.42 kΩ (using Eq. (4), r = 39.5 μm). R_M and C_M were extracted respectively as 16 ± 2 kΩ and 7 ± 1 pF. We considered that R_M and C_M come from the low-current detection unit in the chemical potentiostat and the stray capacitance. EDL capacitances C_{EDL} were obtained as 50 ± 10 pF, which was calculated from extracted parameters of R_{EDL}, α, and Q_{EDL} (R_{EDL}: 3.2 ± 0.6 GΩ, α: 0.97 ± 0.01, Q_{EDL}: 51 ± 11 pF s$^{\alpha-1}$) by using Eq. (5).

4.2 Triangle waveform analysis

Besides frequency-domain characteristics discussed above, we also measured and analyzed time-domain characteristics by using triangle waveform sweep. We simulated a triangle waveform response by using the equivalent circuit with obtained parameters shown in Fig.

4(b). Figure 5 shows experimental and numerical results of triangle waveform response. Numerical results agree well with the experimental results, which supports that the EIS analysis with our modified equivalent circuit works effectively. From the gradient of the triangle ($dV_{in}/dt = 100\ mV_{p\text{-}p} / 100\ \mu s = 10^3\ V\ s^{-1}$) and the observed constant current (30 nA), $C_{triangle}$ was calculated by Eq. (1) as 30 pF. This value is larger than C_{BLM} of 22.6 pF shown in Fig. 4(b), which shows the traditional method overestimates the C_{BLM} value for BLMs formed over an aperture in silicon chips, as described in the Sect. 3.1.

4.3 Reproducibility of the capacitance extraction method

In order to confirm reproducibility of the capacitance extraction method, successive experiments were conducted. In these experiments, two silicon chips with different aperture dimensions shown in Fig. 1(c) were used. Figures 6(a) and 6(b) show the specific capacitances calculated from the extracted membrane capacitances of BLMs on Chips A and B, respectively. In the experiment using Chip A, seven experiments were conducted; EIS was conducted once in each experiment on a different day. In the experiment using Chip B, EIS was conducted every 1 hour to observe the time evolution of the specific capacitances (t of 0 represents the time of the BLM formation in Fig. 6(b)). As a result, the all specific capacitances fell into the range of 0.4 – 1.0 μF cm^{-2} (at most 1.02 μF cm^{-2}, t = 5.5 hours in Fig. 6(b)). In addition, it should be noted that continuous increases in the specific capacitances were observed, which were often reported in previous works.[11,13,19,24,34)]

5. Conclusion

We formed the free-standing BLMs over an aperture in nanofabricated silicon chips. We measured frequency characteristics to evaluate the electrical characteristics of the free-standing BLMs. The specific capacitances of BLMs were calculated using the experimental frequency characteristics and our modified equivalent circuit model including the silicon chip resistance in series with its capacitance. The membrane resistances were successfully extracted, up to 7.00 TΩ (334 MΩ cm^2). This value is higher than the reported values in previous works. The specific capacitances were obtained as 0.57 ± 0.08 μF cm^{-2}, which fell into the range of 0.4 – 1.0 μF cm^{-2}. We also confirmed that specific capacitances were obtained within the range of 0.4 – 1.0 μF cm^{-2} throughout successive experiments. We also measured the triangle waveform responses to compare them with the numerical responses of the modified equivalent circuit model. The numerical results reproduced the experimental

results. These results demonstrated that the capacitance extraction method using EIS measurements and the modified equivalent circuit worked effectively for the free-standing BLMs formed over an aperture in silicon chips.

Acknowledgments

This work was partly supported by JST-CREST Grant Number JPMJCR14F, and by JSPS KAKENHI Grant Number 17K04979. Nation-wide Cooperative Research Projects, Research Institute of Electrical Communication, Tohoku University are also acknowledged.

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Figure Captions

Fig. 1. (Color online) (a) Schematic illustration of Teflon chambers with a sandwiched nanofabricated silicon chip. (b) Detailed illustrations of the cross-sectional view of the nanofabricated silicon chip and a free-standing bilayer lipid membrane (BLM) formed over an aperture in the chip. (c) Optical photomicrographs of apertures in two silicon chips (Chips A and B). (d) Stereo microscope images of the Teflon chambers and the nanofabricated silicon chip sandwiched in between. (e) Schematic illustration of the overall experimental setup with the block diagram of measuring equipment used for triangle waveform sweep.

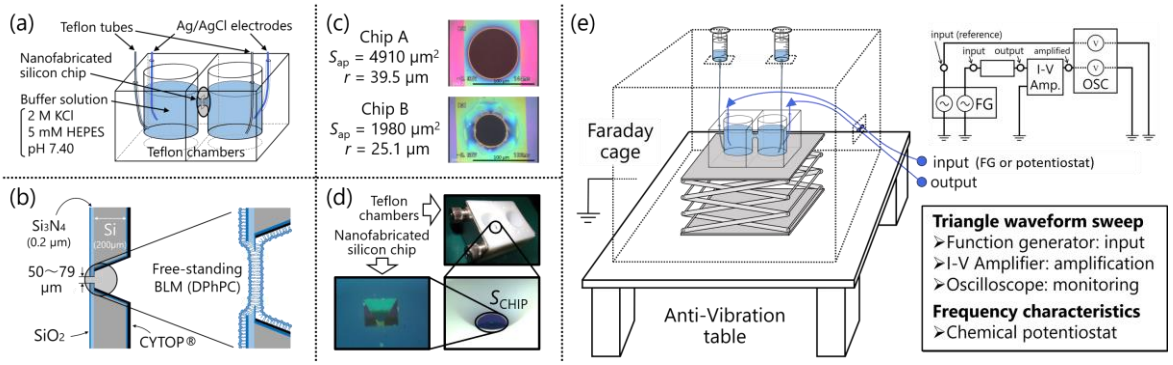
Fig. 2. (Color online) (a) Traditional *RC* parallel circuit (Circuit 1) of a BLM. Electric elements of the platform are ignored. (b) Circuit model (Circuit 2) including R_2 and C_2 of the semiconducting platform. (c) Simulation results of triangle waveform sweep. Observed current I_{out} of Circuit 1 (dashed line), and Circuit 2 (solid line) are shown. The amplitude and the frequency of the input triangle potential V_{in} are 100 $mV_{p\text{-}p}$ at 5 kHz.

Fig. 3. (Color online) (a) Equivalent circuit model used in previous works. Total capacitance C_{Total} is the sum of the membrane capacitance C_{BLM} and the chip capacitance C_{CHIP}. (b) Schematic illustration of a silicon chip and its detailed equivalent circuit. (c) Whole circuit model between two Ag/AgCl electrodes.

Fig. 4. (Color online) (a) Examples of EIS results plotted with fitting curves. (b) Equivalent circuit model with the extracted parameters. The fitting was performed using ZView®.

Fig. 5. (Color online) Experimental and numerical results of triangle waveform response. Numerical simulation was executed by using the equivalent circuit model and parameters presented in Fig. 4(b).

Fig. 6. (Color online) Specific capacitances obtained from the EIS experiment and fitting method using the modified equivalent circuit. (a) Results for Chip A. (b) Results for Chip B. All values were settled within the range of 0.4 – 1.0 μF cm^{-2} except for one result at t = 5.5 h in Chip B.



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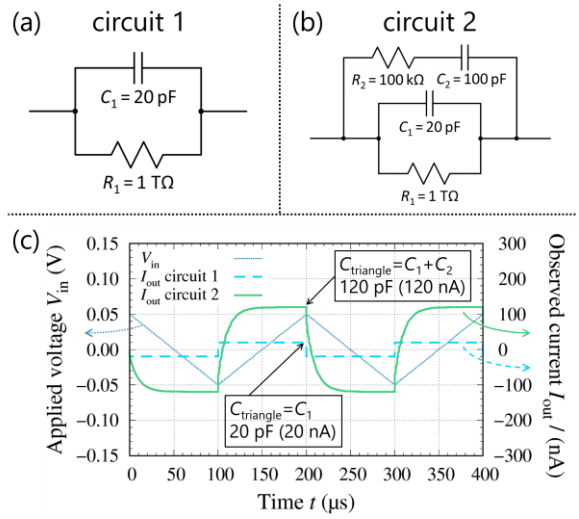

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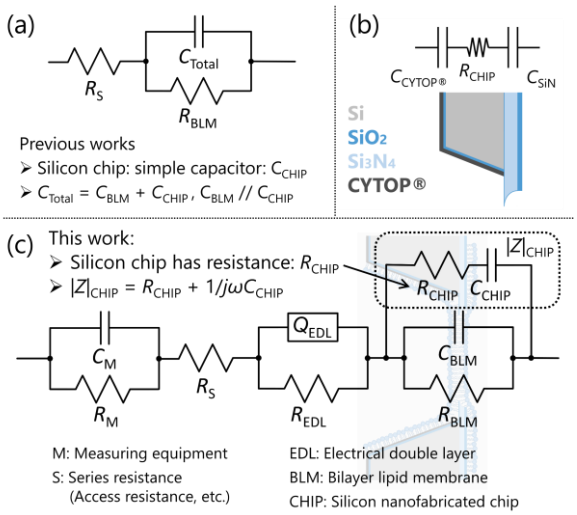

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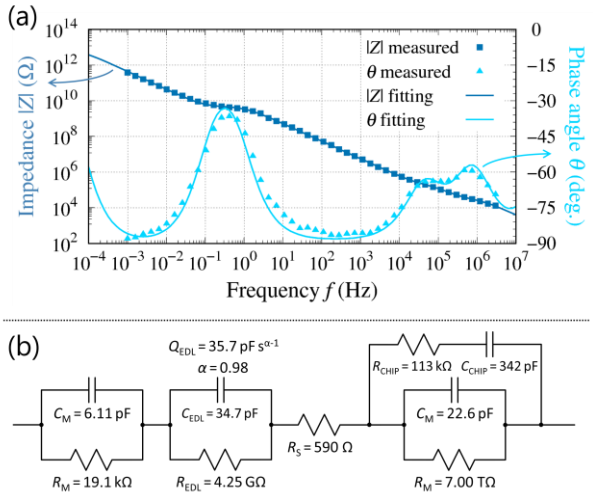

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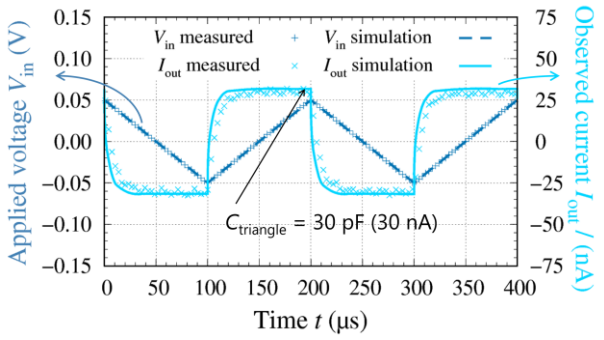

Fig. 5. (Color online)

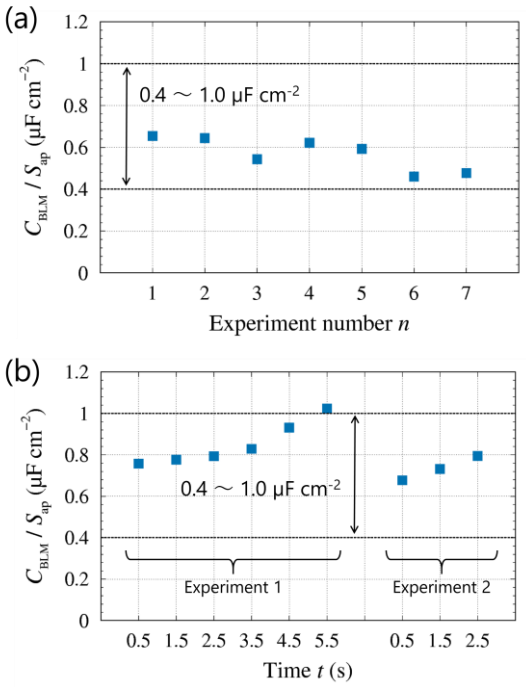

Fig. 6. (Color online)