A Novel Low-Voltage Reconfigurable ΣΔ Modulator for 4G Wireless Receivers

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***Abstract* – This paper presents a new adaptable cascade ΣΔ modulator architecture for low-voltage multi-standard applications. It uses two reconfiguration strategies: a programmable global resonation and a variable loop-filter order. These techniques are properly combined in a novel topology that allows to increase the effective resolution in a given bandwidth, whereas keeping relaxed output swing requirements and high robustness to mismatch and to non-linearities of the amplifiers. Time-domain simulations including the main circuit-level non-idealities are shown to demonstrate the benefits of the presented modulator when it is configured to cope with the requirements of GSM, UMTS, WLAN and Wi-Max.**[†]

I. INTRODUCTION

Sigma-Delta Modulators (ΣΔMs) are very suited for the implementation of reconfigurable Analog-to-Digital Converters (ADCs) required for the fourth generation (4G or Beyond-3G) of wireless hand-held devices [1]. Based on the combined use of oversampling and noise shaping, ΣΔMs can adapt their dynamic ranges to different specifications with large hardware re-use, reduced power consumption and at the lowest cost [2]-[9].

Although changing the sampling frequency has been the reconfiguration strategy most commonly applied, the mandatory use of low OverSampling Ratios (*OSR*s) in wideband communication standards has forced ΣΔMs to achieve the required dynamic ranges by resorting to different strategies, including: high-order shaping [2][6][8][9], switchable cascade topologies [5][9]; programmable notches within the signal band [2][8]; and multi-bit embedded quantizers [3][7][9]. However, the efficient implementation of these techniques requires to explore new ΣΔM topologies capable of adapting their performance to as many specifications as possible while keeping high robustness to circuit errors.

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The modulator presented in this paper is based on three strategies to adapt its functionality to different specifications. First, the modulator loop-filter order can be varied according to the required performance by connecting or disconnecting low-order stages in a cascade topology. Second, resonation is used to optimally distribute the zeroes of the Noise Transfer Function (NTF) within the required signal bandwidth. Third, a unity Signal Transfer Function (STF) is employed in all stages of the cascade for reducing the amplifier output swing requirements [10]. The above-mentioned strategies are combined in a novel reconfigurable cascade ΣΔM topology that maximizes the effective resolution within a given bandwidth with reduced circuit complexity, low sensitivity to element mismatches and high robustness with respect to opamp non-linearities.

II. PROPOSED MODULATOR

Fig.1 shows the proposed modulator architecture. It consists of a reconfigurable cascade topology that makes use of two concepts, namely: unity STF [10] and global resonation [11]. The former is implemented by the feedforward paths that connect the input of each stage with the corresponding quantizer inputs, whereas global resonation is achieved thanks to the inter-stage paths (highlighted in Fig.1) that feed back a delayed scaled version of the last-stage quantization error at the input of the first-stage quantizer. One important advantage of the proposed modulator is that, on the contrary to the one reported in [11], only Forward-Euler (FE)

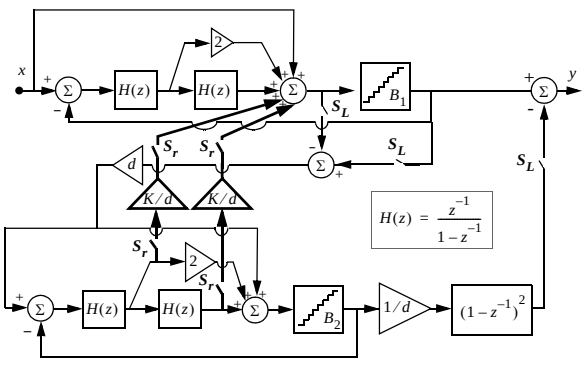

Fig. 1: Proposed reconfigurable ΣΔM topology.

integrators are required, thus making its Switched-Capacitor (SC) implementation easier.

The modulator includes a number of switches to configure the NTF according to the required performance. On the one hand, by connecting the switchable error feedback paths from the last to the first stage —with switches S_r and S_L in ON mode— the global resonation scheme is enabled. On the other hand, the order of the cascade is also reconfigurable. Both reconfiguration strategies (adaptive global resonation and NTF order) can be used independently, thus giving more flexibility to the ΣΔM to adapt its functionality to the required performance. In a practical application, those components that are not used can be turned off by using a power-down control in order to save power consumption.

In case resonation is enabled and considering a linear model for the embedded quantizers, it can be shown that the NTF of the proposed architecture is given by:

$$NTF(z) = \frac{-(1-z^{-1})^2 \cdot [1-(2-K)\cdot z^{-1}+z^{-2}]}{d} \quad (1)$$

where d stands for the inter-stage gain. Note that two of the NTF zeroes are a function of K, whose value can be optimally chosen to maximize the Signal-to-(Noise+Distortion) Ratio (*SNDR*).

This effect is illustrated in Fig.2 for an *OSR* of 4 and embedded quantizers with 4-bit resolution. The optimum values of K/d for an inter-stage gain of 1 and 4 are roughly 0.4 and 0.1, which can be easily implemented using capacitor ratios of 2/5 and 1/10, respectively. If there is no signal scaling along the cascade ($d = 1$), the resolution is increased in 11dB, whereas if $d = 4$, an increment of 23dB is achieved.

For the sake of completeness, Fig.3(a) shows the optimal location of the NTF zeroes in the unity-circle for oversampling ratios of 4, 8 and 16. The effect on the noise shaping is depicted in Fig.3(b) by representing the NTF for the different cases together with their corresponding signal BandWidths (*BW*s).

Note that an increase of d (to reduce the quantization noise) yields a reduction of the feedback coefficient K/d. In practice, this results in a smaller capacitor ratio, which makes the electrical implementation more difficult and prone to circuit non-idealities. However, the value of K/d can be easily implemented if the oversampling ratio is low enough because —as illustrated in Fig.3(a)— a reduction of the *OSR* means an increase of *K*. Therefore, the resonation provided by

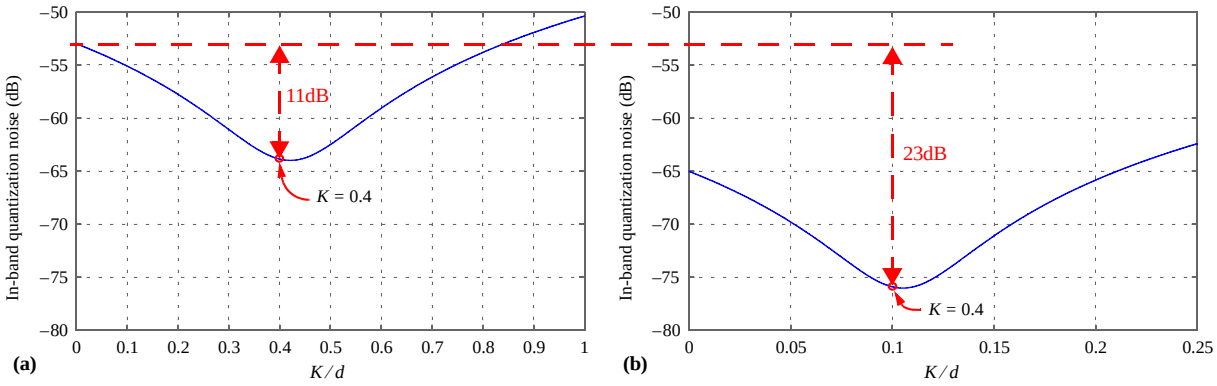

Fig. 2: Variation of the in-band quantization noise with K/d for: (a) $d = 1$, (b) $d = 4$ ($OSR = 4$ and $B_1 = B_2 = 4$).

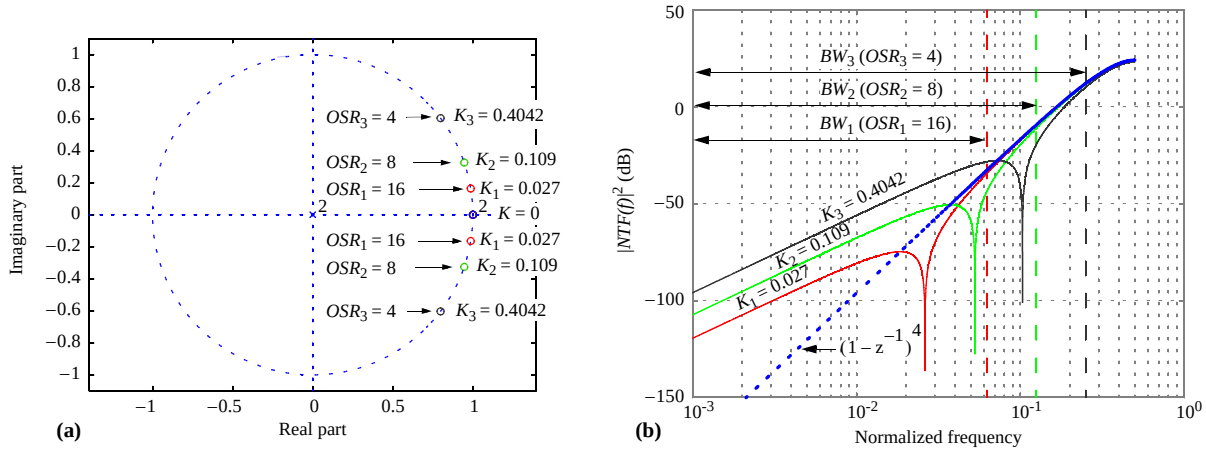

Fig. 3: Optimum distribution of NTF zeroes in the proposed resonation-based ΣΔM for different oversampling ratios: (a) Location of zeroes in the unit circle, (b) NTF vs. frequency ($d = 1$).

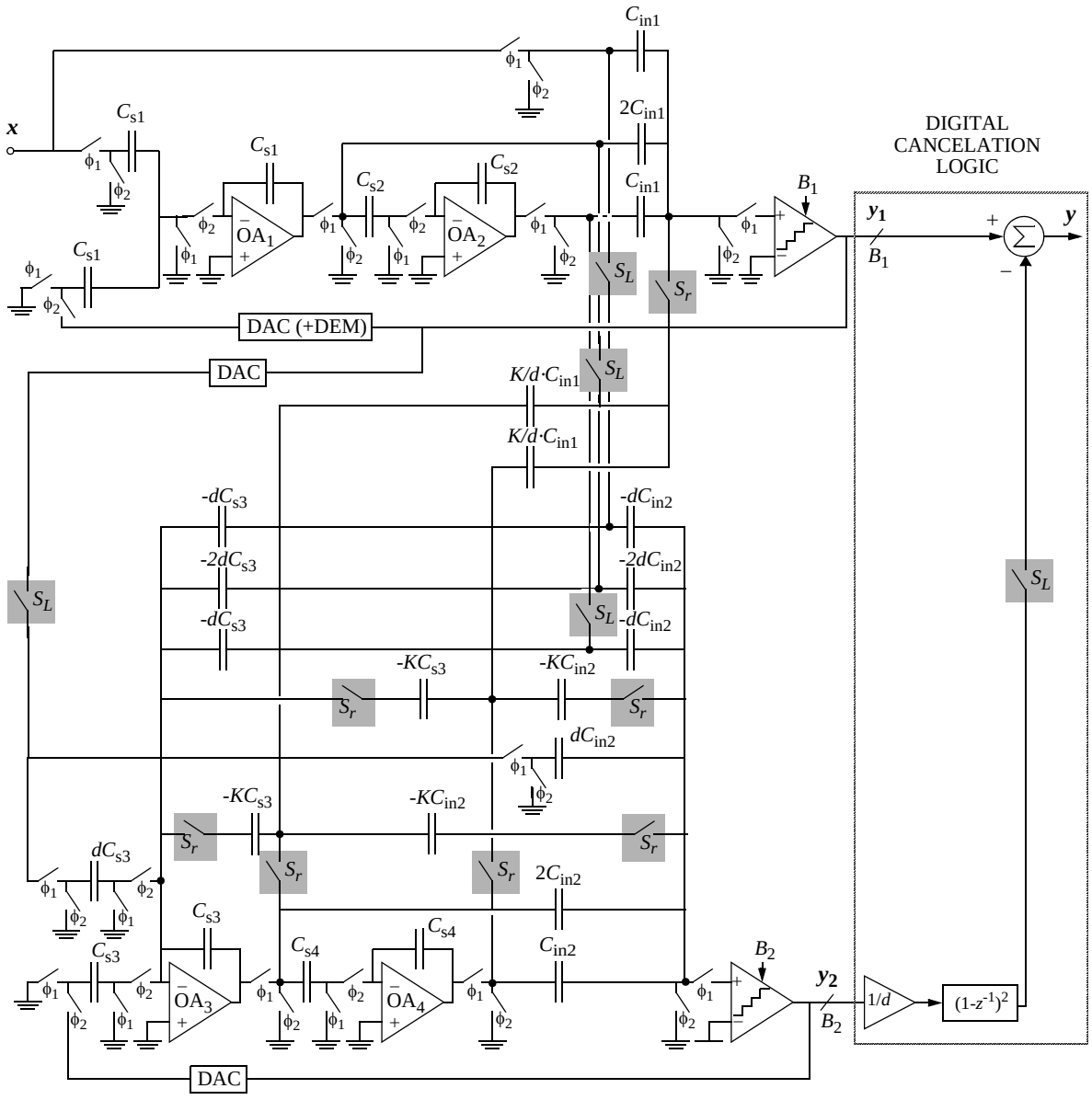

Fig. 4: SC schematic of the proposed reconfigurable ΣΔM (single-ended version).

the proposed architecture is specially suited for wide-band applications with low *OSR*.

Fig.4 shows the conceptual SC implementation of the modulator in Fig.1, in which the required analog additions are implemented by passive SC networks in order to save power. The required analog coefficients are implemented as capacitor ratios using capacitors C_{s1} to C_{s4}, C_{in1} and C_{in2}. Note that a number of capacitors in Fig.4 have negative values; in the actual fully differential implementation, the negative value would be implemented by swapping the corresponding capacitors in the positive and negative signal branches.

The use of passive SC analog additions involves a reduction of the full scale at the quantizer input and, consequently, a compression of the references and the quantizers voltage levels to be used [12]. For instance, if the distribution of the charge in the capacitors of the first-stage analog adder during phase ϕ_1 is considered, the resulting scaling factor is

$$\frac{C_{in1}}{4C_{in1} + 2K/d \cdot C_{in1} + C_{quant}} \qquad (2)$$

where C_{quant} stands for the input capacitance of the quantizer.

In order to get a robust modulator implementation it is desirable to have the same scaling regardless of the use of resonation. However, note from (2) that the denominator term $2K/d \cdot C_{in1}$ equals zero in case resonation is not employed, and thus the scaling factor varies from the one obtained with resonation. Let us assumed that $C_{in1} = 2\text{pF}$, $d = 4$, $K = 0.4$, a 4-bit quantizer and 10-fF input capacitance for the quantizer comparators; then the corresponding scaling factor would be 0.234. If resonation is not employed

($K = 0$), the compression would be 0.245. In this example, a good choice for the reference compression in both cases is 0.25, thus making easier the implementation of the resulting voltage levels. Besides, thanks to the location of the addition in the modulator chain, a small variation of the scaling factor —as the one in this example— will have almost no impact on the modulator resolution. Note that the same applies to the second-stage analog addition.

III. CASE STUDY

In order to show the reconfigurability of the proposed ΣΔM architecture, a case study is presented considering the specifications and standards listed in Table I. Table II shows the values of the modulator design parameters that are reconfigured for the different operation modes, namely: NTF order (L), resonation coefficient (K/d) and *OSR*. Note that different oversampling ratios —and their corresponding sampling frequencies (f_s)— are employed in order to cope with the required resolution of each signal bandwidth. Note that in those operation modes in which no resonation is used (GSM, UMTS and Wi-Max), the switches responsible for the last-stage error feedback (S_r in Fig.1) are disconnected. Additionally, in GSM mode only the first stage is working —with switches S_r and S_L disconnected— whereas all the integrators and comparators of the second stage are turned off.

Global resonation is used only in WLAN mode. In this case, the rounded optimal feedback coefficient is $K/d = 0.1$, resulting in a shift of two zeroes of the NTF from 0 to $0.8 \pm j0.6$. Note that thanks to this optimum distribution of the NTF zeroes —together with the employment of an inter-stage scaling $d = 4$—, the in-band noise is minimized as shown in Fig.2(b).

TABLE I.
SPECIFICATIONS FOR THE ΣΔM IN THE CASE STUDY

Standard	**GSM**	**UMTS[a]**	**Wi-Max**	**WLAN**
SNDR (bit)	14	12	8	10
BW (MHz)	0.2	4	20	20

a. Although the bandwidth of UMTS is 3.84 MHz, it has been expanded to 4MHz in order to easily implement the sampling frequency.

TABLE II.
RESONATION COEFF, MODULATOR ORDER, *OSR* AND *d*

Standard	**GSM**	**UMTS**	**Wi-Max[a]**	**WLAN**
Order (L)	2	4		
Inter-stage gain (d)	----	4		
K	0 (No resonation)			0.4
K/d	0 (No resonation)			0.1
OSR	100	10	4	
f_s (MHz)	40	80	160	

a. Note that resonation could also be employed in this case if a larger resolution is demanded.

IV. SIMULATION RESULTS

Several behavioral simulations have been performed using SIMSIDES, a Simulink-based time-domain simulator for ΣΔ modulators [13]. In all operation modes, 4-bit internal quantizers and a 1-V reference voltage were considered. Additionally, kT/C noise, sampled by 0.25-pF sampling capacitors, is introduced at the first integrator in all simulations. The embedded Digital-to-Analog Converters (DACs) are assumed linear, although dynamic element matching will be required in practice at least in the first stage of the cascade.

Fig.5 shows the modulator output spectra for all the operation modes. In GSM [Fig.5(a)], the in-band error is dominated by thermal noise, whereas in UMTS

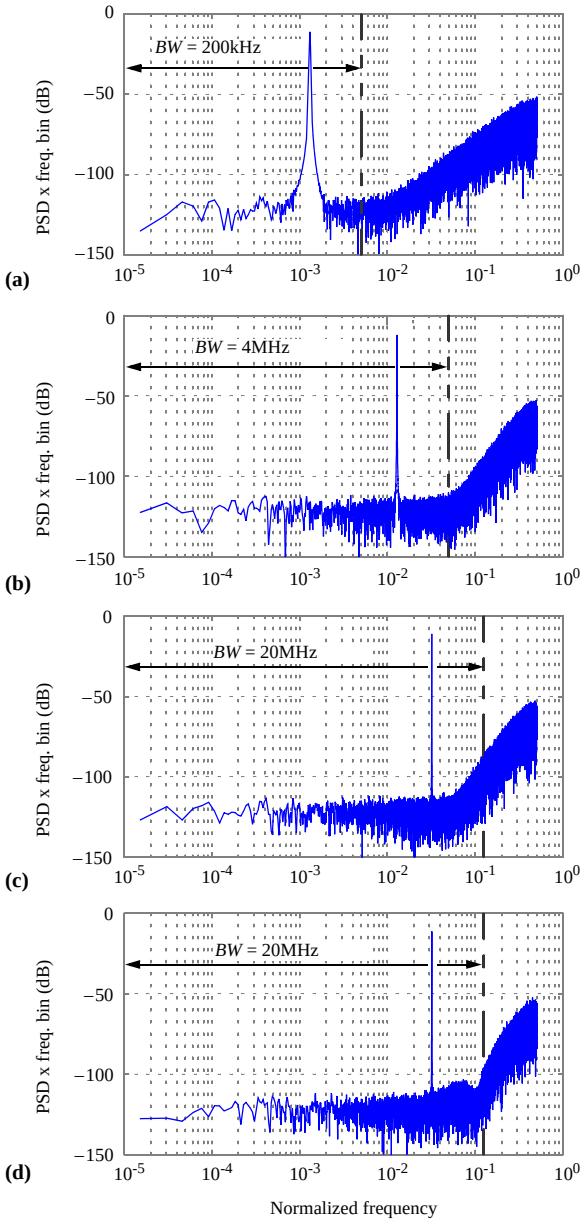

Fig. 5: Modulator spectra of the different modes: (a) GSM, (b) UMTS, (c) Wi-Max, (d) WLAN (-6dBFS input level, 64k-point FFTs).

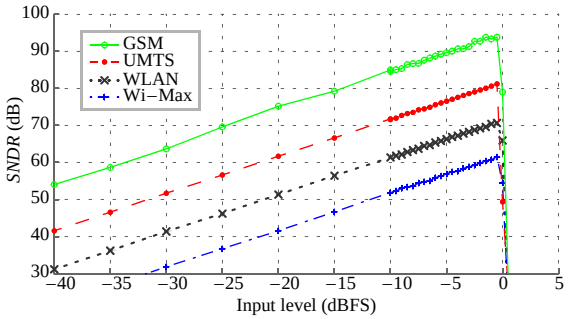

Fig. 6: Modulator *SNDR* versus input level (normalized to full scale).

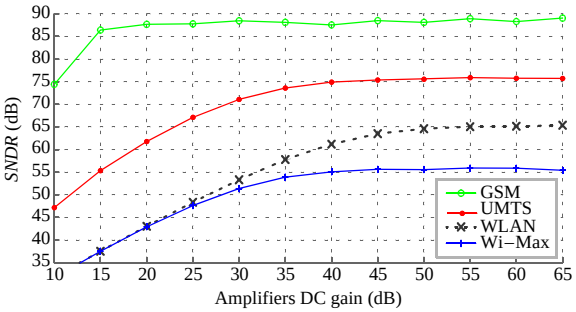

Fig. 8: *SNDR* vs. finite DC gain of the amplifiers (-6dBFS input level).

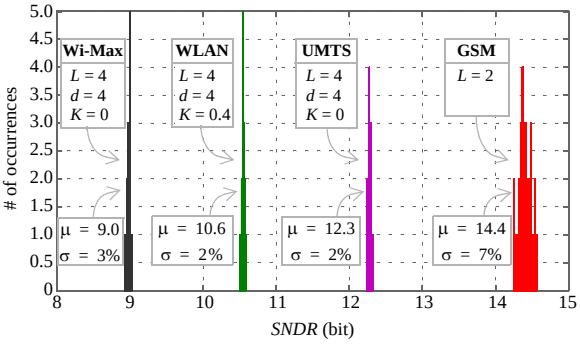

Fig. 7: *SNDR* variation considering a 0.1% capacitor mismatch (-6dBFS input level, 50-run Monte Carlo simulation).

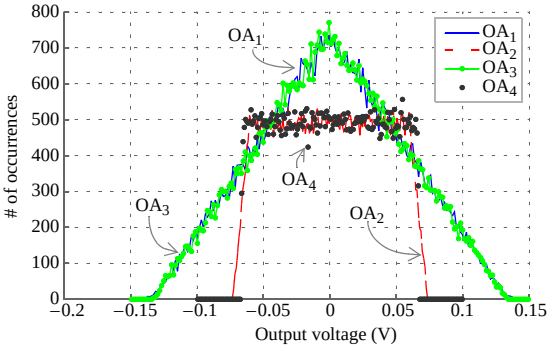

Fig. 9: Histogram of the integrators outputs.

[Fig.5(b)] the larger error term is not clearly defined between thermal or quantization noise. The effect of resonation can be clearly distinguished by comparing Fig.5(c) and (d), corresponding to Wi-Max and WLAN, respectively. Note that in WLAN, resonation reduces the in-band quantization error power as compared to Wi-Max. This is illustrated in Fig.6 where the *SNDR* is represented versus the input signal amplitude. Note that the effective resolution for WLAN is approximately 9dB larger than that for Wi-Max.

The sensitivity to noise leakages due to capacitor mismatch has been studied on the basis of Monte Carlo simulation. Fig.7 shows the *SNDR* at -6dBFS obtained for a 50-run Monte Carlo simulation considering a standard deviation of 0.1% in all capacitors. The mean [μ (bits)] and the standard deviation (σ) of the resulting effective modulator resolutions are also shown for each operation mode. Note that the use of resonation in the WLAN mode introduces no appreciable performance degradation when compared to the rest of operation modes.

Fig.8 shows the effect of the amplifiers finite DC gain on the modulator effective resolution for all the operation modes. Note that the impact of the amplifiers gain on the modulator performance is considerably lower in GSM when compared to the rest of standards. This is due to the topology used for the $\Sigma\Delta$M in the former case (single loop), which does not present the sensitivity to noise leakages inherent to cascade topologies (used in the remaining standards). In the case of UMTS and Wi-Max, there is no appreciable degradation for amplifiers gains above 40dB. This value raises to 50dB for WLAN, which is still not a demanding requirement in practice.

An appealing advantage that comes from the use of unity STFs is the subsequent reduction of the amplifiers output swing. This is illustrated in Fig.9 by plotting the histogram of the integrators outputs obtained from the operation of the proposed modulator in all operation modes. Note that the required output swing is only ± 0.15V for the 1st and 3rd operational amplifiers (OA_1 and OA_3), whereas it reduces to ± 0.10V for the 2nd and 4th ones (OA_2 and OA_4). This translates into an excellent linearity behavior for the proposed architecture.

The latter is illustrated in Fig.10 by plotting the effect of the amplifier gain non-linearity on the modulator *SNDR*. In this simulation, a finite gain of 55dB is considered for all amplifiers, while varying the 2nd-order non-linearity of the DC gain for the amplifiers in the first stage of the cascade. Note that the robustness of the proposed $\Sigma\Delta$M to non-linearities is quite high, even if resonation is used to increase the effective modulator resolution.

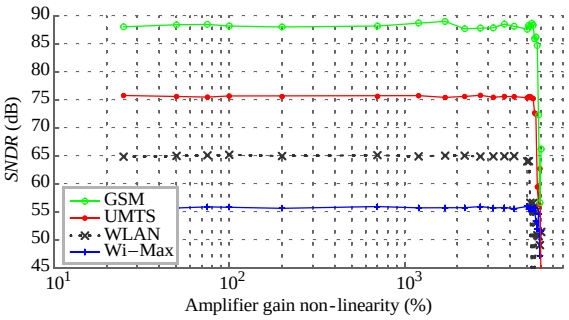

Fig. 10: *SNDR* vs. non-linearity of the amplifier gain (-6dBFS input level, 55-dB amplifier gain).

V. CONCLUSIONS

A new multi-functional cascade ΣΔM architecture has been presented. This architecture is capable to reconfigure the order of the quantization noise filtering and to resonate through switchable feedback inter-stage paths. Additionally, it achieves high linearity with reduced output swing requirements by using unity STFs in both cascaded stages. These characteristics make the proposed modulator very appropriate for the implementation of low-voltage multi-mode A/D conversion, where the resolution of wideband standards can be easily increased by means of adaptive global resonation. A case study covering GSM, UMTS, Wi-Max and WLAN standards has been discussed in order to show the capabilities of the proposed modulator to perform the A/D conversion in future 4G wireless multi-standard hand-held devices.

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