Semi-empirical model of MOST and passive devices focused on narrowband RF blocks

Rafaella Fiorelli[1], Fernando Silveira[2], Adoración Rueda[1] and Eduardo Peralías[1] [1] IMSE-CNM (CSIC) and Universidad de Sevilla, Seville, Spain.
[2] Facultad de Ingeniería, Universidad de la República, Montevideo, Uruguay,
e-mail: fiorelli@imse-cnm.csic.es

Abstract

This paper presents a semi-empirical modeling of MOST and passive elements to be used in narrowband radiofrequency blocks for nanometer technologies. This model is based on a small set of look-up tables (LUTs) obtained via electrical simulations. The MOST description is valid for all-inversion regions of MOST and the data is extracted as function of the g_m/I_D characteristic; for the passive devices the LUTs include a simplified model of the element and its principal parasitic at the working frequency f_0. These semi-empirical models are validated by designing a set of 2.4-GHz LNAs and 2.4-GHz and 5-GHz VCOs in three different MOST inversion regions.

Index Terms

Semi-empirical model, all-inversion region, narrowband, LC-VCO, CS-LNA.

I. Introduction

The modeling of active and passive components becomes more complex when nanometer technologies and radiofrequency signals are involved. However, RF analog designers need simpler models to quickly achieve the circuits' specifications. These two facts pose a compromise in the election of the model utilized in the design stage, since a non-accurate one would generate substantial differences in manual computation and simulated results, leading to useless designs.

We categorize three types of models to describe active and passive elements:

1) Empirical models: manifolds fitted from measurements or simply look-up tables (LUTs), whose parameters are non-physically based.

2) Analytical models: physical-based equations or topologies. They provide relations between basic electrical magnitudes (currents or voltages), whose parameters are obtained from fitting procedures using measured data.
3) Semi-empirical (or semi-analytical) models: are neither analytical nor empirical. We divide them into two sub-types:
   a) those analytical models whose parameters are in look-up tables (LUTs) and depend on primary electrical magnitudes.
   b) those empirical models whose data are obtained from analytical models, e.g. LUTs, obtained from electrical simulations.

In this work, we will show, how to follow these last two kind of descriptions with nanometrics CMOS process, to easily achieve, optimal and precise RF designs in early stages of design. In the case of MOST, empirical models are normally discarded when nanometer technologies are used because the measurements needed to do a correct description of all the parameters are time-consuming and a fabricated circuit is always compulsory.

MOST analytical models, in which are included physical equation-based models, have proved to be useful for CMOS micro and submicrometer technologies, as the number of parameters in the equations set is small and second-order effects are generally discarded. Among the most advanced models which allow precise designs in all-inversion regions of MOS transistor, are: BSIM [1], PSP [2], EKV [3], ACM [4] or HiSIM [5]. Nevertheless, analytical models for CMOS nanometer processes must mandatorily include second and higher order effects since, in this case, they are very noticeable. This modeling produces a extremely complex description with a huge number of parameters, as shown in [3] and [4]. The time needed to obtain their values through the fit of data is one of the reasons why MOST semi-empirical models are a very convenient intermediate choice, and we study them here.

Considering passive components, they can similarly be characterized either with empirical, analytical or semi-empirical models. The first one is discarded following the same justification as in MOST. Analytical ones are especially useful in multi-frequency systems. However obtaining simple and accurate formulas for the element and its parasitics are not always easy to achieve. Semi-empirical models as the one used in this work, are easy to obtain, but they are only useful for narrowband architectures. This work proposes very simple passive components' semi-

empirical models extracted from electrical simulations and saved as LUTs. Depending on the level of accuracy and the available technological information, the LUTs can be extracted using parameterized cells provided by the foundry libraries or the ones obtained with electromagnetic simulators (as ADS Momentum, ASITIC [6] or VPCD of Cadence [7]). In order to speed-up the modeling, we use here the former method. Library cells supplied by the foundry are simulated at the working frequency to obtain their equivalent complex impedance.

This paper is organized as follows. Sections II and III provide the basics of MOST and passive elements modeling as well as the results of implementing it in an RF 90nm CMOS technology (similar behaviors have been observed in technologies bulk CMOS between 350nm and 65nm). Section IV verifies the model by means of design and electrical simulations of two kind of RF circuits: CS-LNAs at 2.4 GHz and LC-VCOs at 2.4 GHz and 5 GHz. Finally the conclusions arrive.

II. MOST SEMI-EMPIRICAL MODEL DESCRIPTION

A MOST model generally describes the following transistor characteristics as a function of the quiescent drain current I_D and/or the terminal voltages V_G and V_D: 1) transconductance g_m; 2) conductance g_{ds}; 3) intrinsic (and extrinsic) capacitances; 4) noise parameters. We use the g_m/I_D ratio as the fundamental base for describing the MOST parameters [8], [9] since g_m/I_D gives a direct indication of the inversion region and its variation is constrained to a very small range, efficiently covered with a grid of some tens of values of g_m/I_D (e.g. from 1 V^{-1} to 30 V^{-1} in a nanometer bulk MOS). For our 90nm technology, strong inversion is well below of g_m/I_D =10V^{-1}, weak inversion is well above of g_m/I_D =20V^{-1} and moderate inversion is in the middle of them. The model presented here considers that: 1) the MOST has a quasistatic behavior (transition frequency f_T above ten times the working frequency f_0 [10]); 2) only the quasistatic capacitances C_{ij} with ij=$\{gs, gd, gb, bs, bd\}$ are included; 3) the channel length is the minimum of the process to reach the highest f_T; and 4) V_B=V_S=0.

Our model, whose topology is shown in Fig. 1.(a), comprises the following relations derived from electrical simulations on parametric cells modeled by the foundry with precise advanced analytical models:

A. Normalized current $i = I_D/(W/L)$ as function of g_m/I_D.

B. g_{ds}/I_D as function of g_m/I_D and V_{DS}.

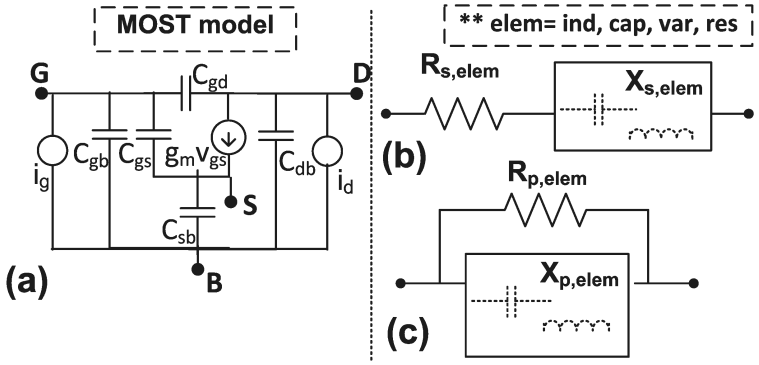

Figure 1. (a) MOST model. (b) Serial and (c) parallel network model of the passive elements (inductors, capacitors, varactors and resistors).

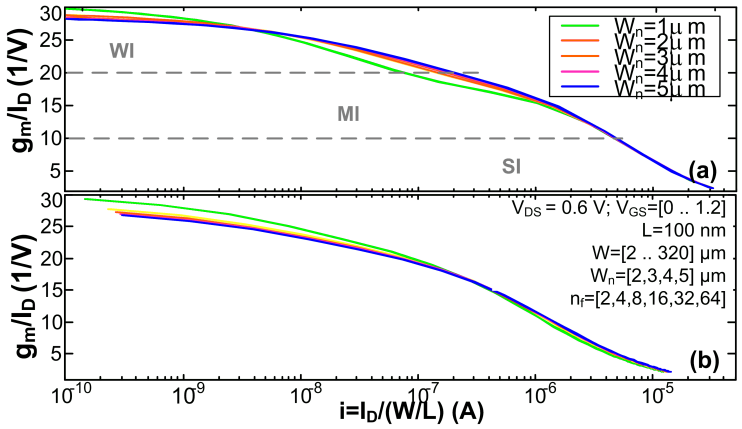

Figure 2. (a) nMOS and (b) pMOS g_m/I_D versus i for a wide set of widths.

C. Area-normalized capacitances $C_{ij}^{'}$ versus g_m/I_D.

D. Overdrive voltage V_{OD}=$V_G - V_T$ versus g_m/I_D.

E. Thermal noise parameters as function of g_m/I_D and V_{DS}; and flicker noise parameter versus g_m/I_D, at f_0.

The spread with W of previous characteristics (versus g_m/I_D) is slight and in a first approximation it can be neglected if narrow devices are not used. Except for g_{ds}/I_D and the thermal noise parameters, these features are also weakly dependent of V_{DS} and this variability can be initially discarded.

Flicker parameter is also function of frequency, but this variation is not included in the LUTs because the model proposed here is for a narrow band on f_0; hence only the simulated data at

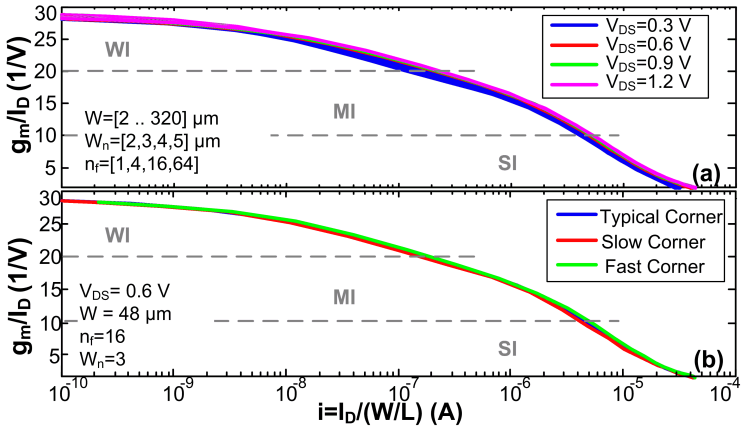

Figure 3. nMOST g_m/I_D versus i (a) for four V_{DS} voltages and (b) for typical, fast and slow corners.

that frequency is collected.

A. g_m/I_D characteristic

The g_m/I_D ratio defines the inversion region and has a biunivocal relation with i [11]. For our RF CMOS 90nm process the behavior of g_m/I_D vs. i for a minimum channel length nMOS is visualized in Fig. 2, with W={2, .. ,320} μm (sweeping finger width, W_n, and number of fingers, n_f). The plot shows that for W_n >1 μm the spread is very small.

The g_m/I_D ratio has also small variations with the drain-source voltage, V_{DS}, and the process corners, as observed in Fig. 3. Neither V_{DS} variations or process variations (for typical, fast and slow corners) modify considerably the g_m/I_D curve, and hence the circuit characteristic in which this transistor is embedded.

The independence of g_m/I_D with W, V_{DS} and process corners reinforce the idea of utilizing this ratio as the independent variable of the MOST LUTs. Also this fact simplifies the extraction as only one transistor or a small number of them (with different W and V_{DS}) suffice to collect this LUT.

B. Output conductance g_{ds} and g_{ds}/I_D ratio

Output conductance g_{ds} dramatically increases in nanometer processes due to the shortening of MOST channel length, as g_{ds} is, in a first approximation, inversely proportional to the transistor length L [10]. To normalize this information, the g_{ds}/I_D ratio is studied here [8]. Figure 4 shows

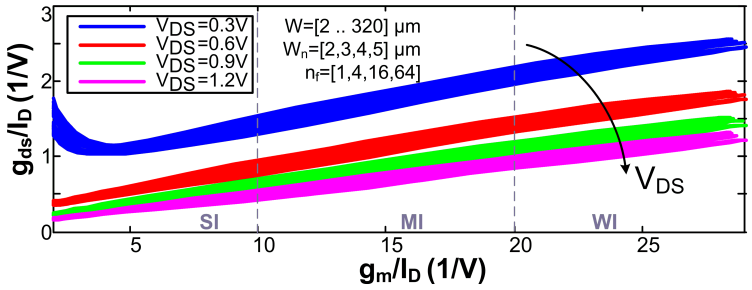

Figure 4. nMOS g_{ds}/I_D versus g_m/I_D. For each V_{DS} the width is swept in the complete range of values available.

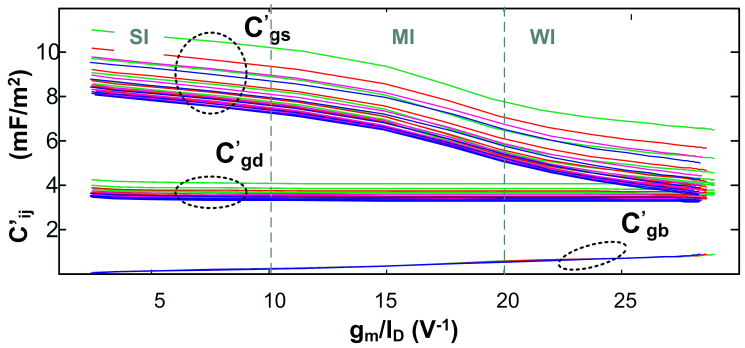

Figure 5. nMOS intrinsic capacitances: (a) $C_{gs}^{'}$, (b) $C_{gd}^{'}$, (c) $C_{gb}^{'}$ versus g_m/I_D for W_f >1 μm.

the behavior of g_{ds}/I_D versus g_m/I_D when W and V_{DS} vary jointly. The g_{ds}/I_D range is small, moving from 0 to 2.5 V^{-1} in a quasi-linear behavior. The variations with V_{DS} are not negligible.

C. MOST extrinsic and intrinsic capacitances

Radiofrequency design requires the inclusion of transistor capacitances in its modeling, grouped as intrinsic and extrinsic ones. They influence not only on the computation of the MOST transition frequency f_T but also on the input and output MOST impedances.

For a quasistatic MOST behavior ($f_0 << f_T$), it is enough to include the following capacitances: C_{gs}, C_{gd}, C_{gb}, C_{bs} and C_{bd}. The extrinsic part of these capacitances are modeled with the known expressions of Tsividis model [10], and their parameters are estimated from technological data and layout considerations. The intrinsic part is obtained from electrical simulations. These capacitances change with the inversion level [10] and with the transistor size. The hypothesis done in this work is that the intrinsic capacitances are proportional to the gate area (WL) because

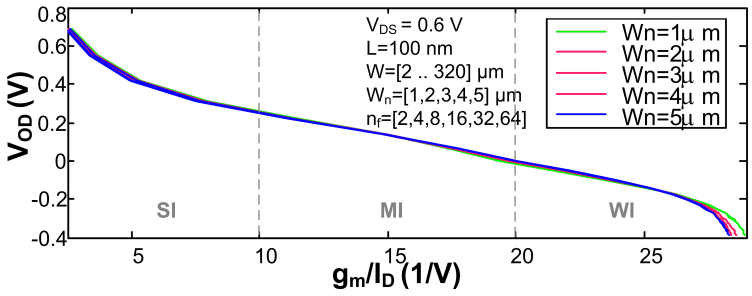

Figure 6. nMOST overdrive voltage versus g_m/I_D varying W, for V_T=0.41 V

they are proportional to the oxide capacitance C_{ox} which is itself proportional to WL [10]. Using that hypothesis, the LUT is composed by the normalized capacitances C'_{ij} versus g_m/I_D.

To study how C'_{ij} behave, the plots of nMOS C'_{gs}, C'_{gd} and C'_{gb} versus g_m/I_D are seen in Fig. 5, for a wide set of W. Their maximum absolute spread are, respectively, around 1 mF/m^2, 0.4 mF/m^2 and less than 0.02 mF/m^2. Only for C'_{gs} the error is appreciable for weak inversion, where C'_{gs} rounds 4 mF/m^2 and the relative error is around 20%. As we have observed, this variation is acceptable for the studied circuits, hence we collect the normalized capacitance LUTs only versus g_m/I_D, discarding the effects of W and V_{DS}.

D. Overdrive voltage versus g_m/I_D

The overdrive voltage V_{OD}, hence voltage V_{GS}respect to the threshold voltage V_T, are functions only of the normalized current [3], [4], and hence of the g_m/I_D accordingly to our assumptions of Section II-A. Analogously as we saw in that section, it slightly varies with the MOST width, as observed in Fig. 6.

E. Noise modeling in MOS transistors

The MOST noise sources considered in this model are presented in Fig. 1.(a), and are the drain noise (the sum of white noise and flicker noise) and induced gate noise [10], which are modeled with semi-analytical models. Their power spectral density (psd) are, for white noise, $\overline{i_w^2} = 4k_BT\frac{\gamma}{\alpha}g_m$; for flicker noise $\overline{i_{1/f}^2} = \frac{K_F g_m^2}{C'_{ox}WL}\frac{1}{f}$ and for induced gate noise $\overline{i_g^2} = \frac{16}{5}\pi^2 k_BT\alpha\delta\frac{C_{gs}^2}{g_m}f^2$ [12], where the parameters are γ, α, δ and K_F. When working with short-channel devices γ and α vary with the inversion region, To show this graphically, these parameters (as well as γ/α)

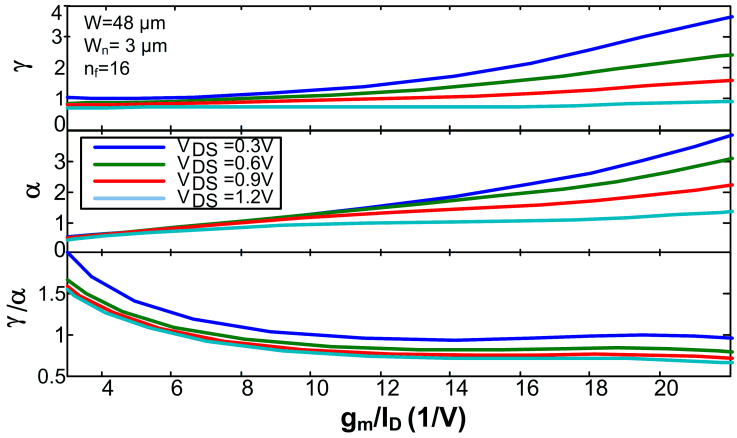

Figure 7. Noise parameters: γ, α and γ/α for a nMOS of W=48 μ and L=100 nm.

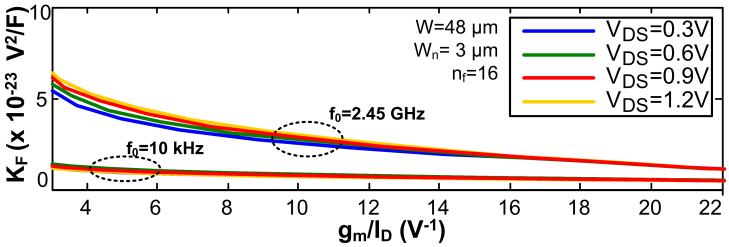

Figure 8. Parameter K_F for two f_0 and four V_{DS} voltages.

are plotted in Fig. 7. In strong inversion γ and α are low, but not always near the generally used values of $\gamma = 2/3$ and $\alpha = 0.6$. When moving to weak inversion, both parameters suffer a dramatic raise. This increment generates circuit noise computation errors if the MOST is biased in MI and WI. Nonetheless, when the γ/α ratio is present, it is maintained relatively constant and less errors appear.

For the flicker noise psd, the K_F parameter is modeled against g_m/I_D and f_0, As Fig 8 presents, its value changes with the working frequency and the different inversion regions considered, which could not be negligible in certain designs. As seen, K_F decreases when moving to weak inversion and the estimation of K_F increases for high frequencies.

Finally, due to the very small effect of the induced gate noise, compared with other MOST noise psd, the parameter δ is considered constant and equal to $\delta = 4/3$.

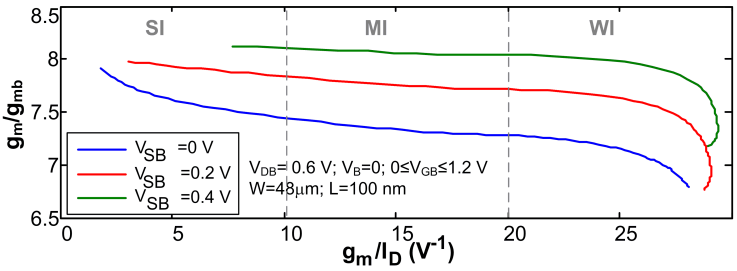

Figure 9. g_m/g_{mb} ratio for a nMOS of W=48 μ and L=100 nm.

F. Bulk substrate effect

This can be considered a second order effect because g_{mb} is much smaller than g_m; in fact this relation can be modeled as a constant value for all-inversion regions, as seen in Fig. 9. Observe that even when $V_S = V_B = 0$, g_{mb} is not null.

III. Passive component semi-empirical models

We use very simple semi-empirical models of passive components, extracted from cells provided by the foundry. As seen in Fig.1.(b) and (c), a resistance and a reactance, in series or parallel, extracted electrically, form the model. The extraction of the model depends on the topological location of the component; for example, if the device has an AC grounded terminal or is fully differential. In noise modeling, only the thermal contribution of the resistive part of the passive component is considered ($v^2 = 4k_BTR$).

A. Inductor modeling

The extracted inductor model consists of an equivalent ideal inductor with a parasitic resistor, for each f_0. The inductor has a complex series impedance $Z_{ind} = R_{s,ind} + j|X_{s,ind}| = R_{p,ind}//j|X_{p,ind}|$ where $R_{s,ind}$ and $R_{p,ind}$ are the parasitic series and parallel resistances and $X_{s,ind}$ and $X_{p,ind}$ are the series and parallel reactances, respectively. Its quality factor is $Q_{ind} = |X_{s,ind}|/R_{s,ind} = R_{p,ind}/|X_{p,ind}|$. If the inductor quality factor $Q_{ind} \geq 4$, both reactances are approximately equal, $X_{s,ind} = X_{p,ind} = X_{ind}$; when divided by the angular frequency $\omega_0 = 2\pi f_0$, the equivalent inductance $L_{ind} = |X_{ind}|/\omega_0$ is obtained.

In these conditions our inductors' semi-empirical model consists of the relations of Q_{ind}^{max} versus L_{ind} for each f_0, where Q_{ind}^{max} is the maximum quality factor for each feasible inductor

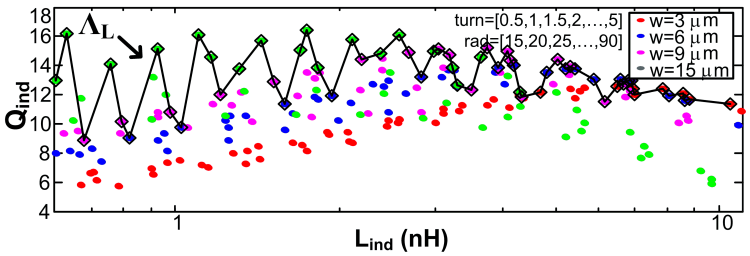

Figure 10. Inductor quality factor Q_{ind} for f_0=2.4 GHz. The maximum inductor quality factors are marked with a black line.

value of the technology. The characterization of a set of technology inductors has two steps. The first step is to run the AC analysis for a large set of inductors, varying their physical magnitudes (turns, coil widths and/or radius), to obtain a complete collection of modeled devices characteristics, e.g. Q_{ind}, L_{ind}, as it is shown in the scatter plot of Fig. 10 for our 90nm process. The minimum quality factor Q_{ind} of the set of selected inductors is 5, to be far from the self resonance frequency of the device. The second step is to collect the inductor LUT, Λ_L, where for each inductance value, we get the highest inductor quality factor (black line of Fig. 10) and the geometry of its implementation. From Q_{ind}^{max} and L_{ind}, $R_{s,ind}^{min}$ and $R_{p,ind}^{max}$ are deduced. Only inductors in Λ_L are considered in our RF designs.

B. Capacitor and varactor modeling

The model for capacitors and varactors is a complex parallel impedance $Z_{cap} = R_{p,cap}// - j|X_{p,cap}| = R_{s,cap} - j|X_{s,cap}|$ where $R_{s,cap}$ and $R_{p,cap}$ are the serial and parallel parasitic resistances and $X_{s,cap}$ and $X_{p,cap}$ its series and parallel reactances. Its quality factor is $Q_{cap} = |X_{s,cap}|/R_{s,cap} = R_{p,cap}/|X_{p,cap}|$. With $Q_{cap} \geq 4$ parallel and serial capacitances could be considered equal and the equivalent capacitance is $C_{cap} = 1/(\omega_0|X_{cap}|)$.

As well as the inductors, the first step in the characterization is to run an AC analysis for a considerable number of devices (vary their width w and length l) to collect their characteristics, as seen in the scatter plot of Fig. 11. The second step is to collect the capacitor LUT, Λ_C, where for each feasible capacitance value we extract the maximum quality factor Q_{cap}^{max} (black lines of Fig. 11) and capacitor size. From Q_{cap}^{max} and C_{cap}, $R_{s,cap}^{min}$ and $R_{p,cap}^{max}$ are deduced. In this 90nm process, as gathered from Fig. 11, MiM capacitors have very high quality factors, above 50 for C_{cap} below 2 pF, meaning that parallel (serial) parasitic resistances are very high (slow).

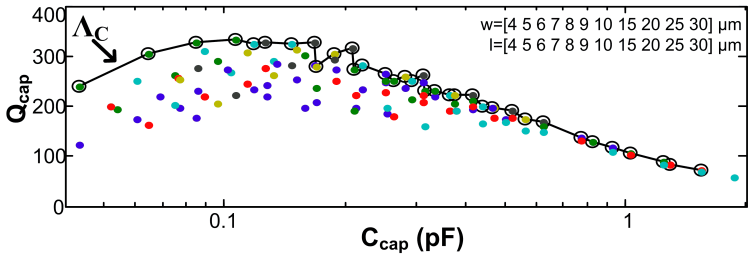

Figure 11. MiM capacitors quality factors, varying w and l for f_0=2.4 GHz.

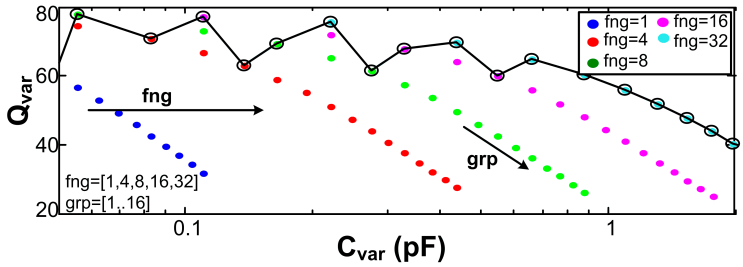

Figure 12. Accumulation varactors quality factors, for f_0=2.4 GHz

Varactors are generally based on semiconductor devices and have much lower quality factor than MiM capacitors. In this work we use accumulation varactors, whose quality factors can be comparable with the ones of high-Q on-chip inductors. As the equivalent capacitance of varactors strongly depends on the signal amplitudes, it is not always possible to use AC analysis to characterize them. For these devices, we need a large-signal analysis, and in this case we utilize the PSS analysis of SpectreRF. It enables us to calculate the impedance Z_{var} seen between the terminals gate-drain/source at f_0, i.e. $Z_{var} = \underline{V}(f_0)/\underline{I}(f_0)$, where $\underline{V}$ and $\underline{\mathrm{I}}$ are the phasors in f_0 of v_{var} and i_{var} of Fig. 12. This way we obtain the quality factor Q_{var} and capacitance C_{var} at the working frequency. Being V_{tune} the tuning voltage (at the drain-source terminal), V_G^{DC} the DC voltage and V_G^{RF} the amplitude voltage at the gate terminal. In this study we fix V_{tune}=0.5 V, V_G^{RF}= 0.4 V and V_G^{DC}=0.5 V. The varactors studied have a fixed finger size of W/L=1.6 μm/400 nm, while the number of fingers fng and the number of rows of these fingers grp can be sweep. Applying the same steps to obtain the capacitors LUTs we generate Fig. 12 and the varactor LUT, Λ_{Var}.

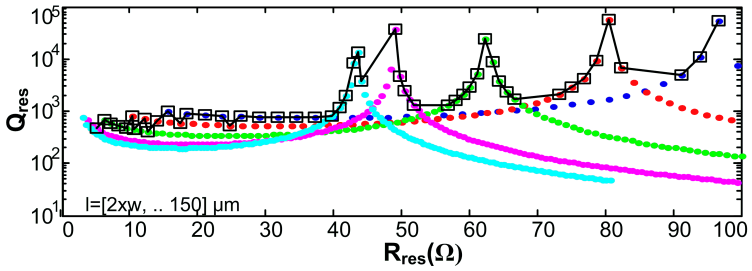

Figure 13. P+ Poly resistor characteristics: R_{res} vs Q_{res} for f_0=2.4 GHz.

C. Resistor modeling

In this paper, only resistors with low resistances values are studied as they are typically used for adjusting RF circuits input/output impedances [13]. We only discuss the characteristics of the RF characterized P+ Poly resistors with silicide, which are appropriate when low resistance values are needed in RF. The model presented here is used only when the resistor is in an RF path.

As well as inductors and capacitors, integrated resistors have associated parasitics, and therefore, we could model it accordingly with an AC analysis. Depending on the resistor type and size, its effective parasitic in AC could be capacitive or inductive. As the monolithic resistors studied have low resistance values, it is more convenient to model them as a resistor R_{res} in series with a series reactance $X_{s,res}$, with its corresponding quality factor Q_{res}, defined as $Q_{res} = R_{res}/|X_{s,res}|$.

The resistance of the P+ Poly resistors with silicide is set fixing their width w and length l. In this work, the width is swept from 2 μm to 10 μm despite it can be further reduced to less than 0.5 μm. It is done in order to position at least 6 contacts in each resistor's terminal to reduce the equivalent contact resistance. The first step of the characterization is to extract the device characteristics R_{res} and Q_{res}, as it is shown in the scatter plot of Fig. 13. The second step is to collect the LUT Λ_R, where for each resistance value it is found the highest quality factor Q_{res}^{max}, and the geometric sizing of each implementation. These values are highlighted in Fig. 13 with square symbols on black line.

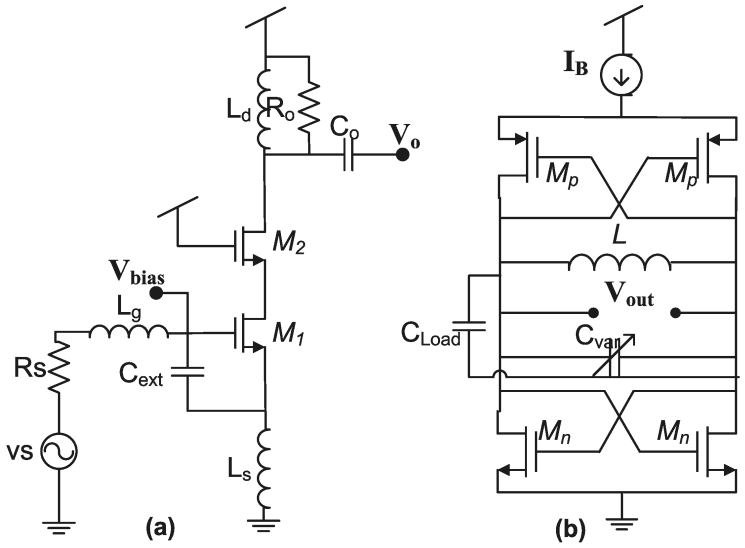

Figure 14. Schematics of (a) CS-LNA and (b) LC-VCO used to verify the semi-empirical model.

Table I

COMPARISON BETWEEN COMPUTATIONAL ROUTINES AND SPECTRERF SIMULATIONS.

Design	g_m/I_D	I_D	W	C_{ext}	L_s	L_g	G (dB)		NF (dB)	
CS-LNA	(1/V)	(mA)	(μm)	(fF)	(nH)	(nH)	Calc.	Sim.	Calc.	Sim.
LNA1	5	0.7	4.9	290	2.6	11	6.6	5.7	3.4	4.3
LNA2	13	0.7	28.3	370	1.5	8.7	12.2	11.8	2.1	2.5
LNA3	20	0.7	320	50	0.9	9.6	11.7	10.4	2.9	3.0
Design	g_m/I_D	L_{ind}	I_D	W_n	W_p	C_{var}	f_{osc} (GHz)		$\mathcal{L}$ (dBc/Hz)	
LC-VCO	(1/V)	(nH)	(mA)	(μm)	(μm)	(fF)	Calc.	Sim.	Calc.	Sim.
VCO1	7	4.1	0.75	7.0	22	86/870	5.0/2.45	5.09/2.45	-114/-118.5	-114/-120.5
VCO2	10	4.6	0.38	8	27/733	43	5.0/2.45	5.25/2.48	-110.7/-115	-110.1/-116.7
VCO3	16	1.5	0.6	60	196	60/2130	5.0/2.45	5.9/2.55	-111.9/-116.3	-109.3/-116.8

IV. MODEL VERIFICATION VIA CS-LNA AND LC-VCO DESIGNS.

We verify our semi-empirical model by means of comparing computed characteristics with a Matlab program with their SpectreRF electrical simulations over two circuits: 1) a 2.4-GHz common-source low noise amplifier (CS-LNA), and 2) a 2.4-GHz and 5-GHz LC tank voltage controlled oscillator (LC-VCO).

A. CS-LNA

The CS-LNA considered to verify this model is presented in Fig. 14.(a). The description used to make the comparison is similar to the one presented in [14], but considering that the MOST model covers all-inversion regions. The elements modeled are the gate and source inductors L_s and L_g, the external capacitor C_{ext} and the MOST M_1 and M_2 (both considered with equal dimensions). An ideal output network is adjusted for each design to obtain maximum power transference to the resistive load R_L. LNA input impedance is fixed equal to the input source resistance R_S. Due to the high quality factor of the capacitors, they are considered ideal, but its election is restricted over Λ_C. It is not the case of the inductors, whose parasitic resistances are included in the modeling. The bulk effect presented in the cascode MOST M_2 is neglected as this transistor affects much less than the MOST amplifier M_1. K_F is considered constant as this noise affects very little this design due to the frequencies involved.

Three designs, biased in three different inversion regions and with a low current of 0.7 mA, were chosen to perform the comparison, as listed in Table I. Noise figure, NF, and power gain, G, are the data to be compared. As shown, the relative errors in NF and G are below 1 dB and 1.3 dB, respectively.

B. LC-VCO

The LC-tank cross-coupled differential VCO utilized in this work is visualized in Fig. 14.(b). The modeled elements are the nMOS and pMOS transistors, the tank inductor and the tank varactor; the last two evaluated at 2.4 Ghz and 5 Ghz. The description used to model this design is given in [9]. K_F is considered constant because the phase noise is modeled in the $1/f^2$ region.

In Table I we present two sets of VCOs (for f_{osc}=2.45 GHz and 5 GHz) biased in three different inversion regions (nMOS and pMOS transistors have the same g_m/I_D) using three different inductor values. Load capacitance C_{Load} is fixed at 100 fF while minimum varactor capacitance is set to 40 fF. To do the model validation we choose the phase noise $\mathcal{L}$ and oscillation frequency f_{osc} as the VCO characteristics to be studied.

For f_{osc}=2.45 GHz, the error in $\mathcal{L}$ is below 2 dB and the oscillation frequency relative error is below 5%. When considering f_{osc}=5 GHz and $g_m/I_D = 16$, the error in f_{osc} and $\mathcal{L}$ increase up to 18% and 2.5 dB because the f_T of the pMOS reaches 3 times f_{osc} and non-quasistatic capacitances affect the design.

V. Conclusions

This paper presents a set of semi-empirical models used for RF analog designs in all-inversion regions. The behavior of MOST characteristics is studied as function of the g_m/I_D ratio, as i, g_{ds}/I_D, C'_{ij}, V_{OD} and noise parameters. An analysis of basic passive components as inductors, capacitors and resistors is also developed, presenting a simple model to be used in RF designs. Semi-empirical modeling has been validated by designing three CS-LNAs and six LC-VCOs, comparing the computed data using the proposed semi-empirical models with the electrical simulations. The resulting agreement among them verifies our semi-empirical modeling is a good tool for RF analog design.

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