RTD based Logic Circuits Using Generalized Threshold Gates[1]

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***Abstract* – Many logic circuit applications of Resonant Tunneling Diodes are based on the MOnostable-BIstable Logic Element (MOBILE). Threshold logic is a computational model widely used in the design of MOBILE circuits, i.e. these circuits are built from threshold gates (TGs). The MOBILE realization of generalized threshold gates is being investigated. Multi-Threshold Threshold Gates (MTTGs) have been proposed which further increase the functionality of the original TGs. Recently, we have proposed a novel MOBILE circuit topology obtained by fundamental properties of threshold functions. This paper describes the design of *n*-bit adders using these novel MOBILE circuit topologies. A comparison with designs based on TGs and MTTGs is carried out showing advantages in terms of speed and power delay product and device counts.**

***Index Terms* - Resonant Tunneling Diodes, MOBILE, Threshold gate, nanopipelining.**

I. INTRODUCTION

Resonant tunnelling diodes (RTDs) are very fast non linear circuit elements which exhibit a negative differential resistance (NDR) region in their current-voltage characteristics (Figure 1a) which can be exploited to significantly increase the functionality implemented by a single gate. Circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [1]. The MOBILE (Figure 1a) is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage (V_{bias}). When V_{bias} is low, both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{bias} to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state). Output is high if the driver RTD is the one which switches and it is low if the load switches. Assuming equal current densities for both RTDs, peak currents are proportional to RTD areas, λ_1 and λ_2, for load and driver respectively. Thus, $\lambda_1 < \lambda_2$ the load switches (the output V_{out} goes to low or "0") and if otherwise $\lambda_2 < \lambda_1$ the driver switches (the output V_{out} goes to high or "1"). Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration for an inverter MOBILE shown in Figure 1b, the peak current of the driver RTD can be modulated using the external input signal V_{in}. During a critical period when V_{bias} rises, the voltage at the output node V_{out} goes to one of the two stable states (low or high), corresponding to "0" and "1" in binary logic. RTD areas are selected such that the value of the output depends on whether the external input signal V_{in} is "1" or "0". For $V_{bias} = 1$, the output node maintains its value even if the input changes. That is, this circuit structure is self-latching allowing to implement pipeline at the gate level without any area overhead associated to the addition of the latches which allows very high throughoutput.

The operating principle of MOBILE is extremely well suited to implement the arithmetic operation on which Threshold Gates [2] (TGs) are based. The circuit topology in Figure 1b has been extended to systematically implement TGs [3][4] and have been experimentally demonstrated [4][5]. TGs are a generalization of conventional Boolean gates, able to implement also more complex functions which is atractive from the point of logic design:

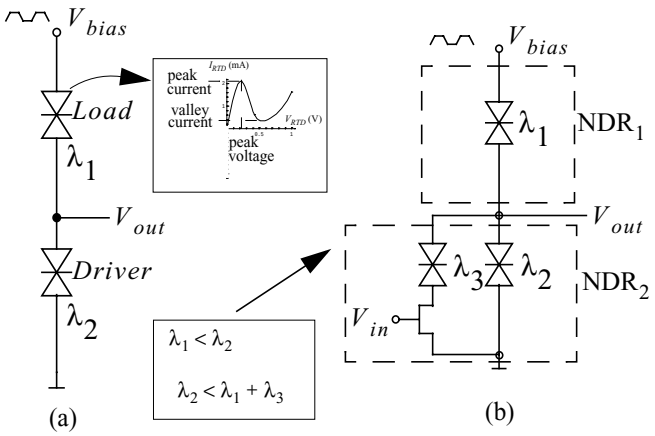

Figure 1.-a) Basic MOBILE, (b) MOBILE inverter.

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less gates and interconections. More recently, generalized threshold gates, also suitable to be realized with MOBILE RTD structures, are being investigated [6], [7], [8], [9]

In this paper we design, evaluate and compare 8-bit nanopipelined adders implemented with different threshold-based MOBILE logic styles. The rest of the paper is organized as follows. Section II describes and compares several threshold gate based MOBILE styles. Architectures of 8-bit adders using these gates are described, simulated and compared in Section III. In the conclusions the results obtained are discussed.

II. GENERALIZED THRESHOLD GATE MOBILE

For the sake of clarity, let us consider a two-input function, the EXOR, $f(x_2, x_1) = x_1 \oplus x_2$, to illustrate the relationship between generalized threshold logic and MOBILE circuit topologies, as well as to introduce the different topologies. This function is not a threshold function however, a number of MOBILE implementations are possible, if we generalize the threshold logic concepts.

A TG [2] is defined as a logic gate with n binary input variables, x_i, $(i = 1, \ldots, n)$, one binary output y, and for which there is a set of $(n + 1)$ real numbers: threshold T, and weights $w_1, w_2, \ldots, w_n$, such that its input-output relationship is defined as $y = 1$ *iff* $\sum_{i=1}^{n} w_i x_i \geq T$, and $y = 0$ otherwise.

Non threshold functions require a network of TGs to be implemented. Figure 2 depicts the TG networks realizing the two-input EXOR (Figure 2a). Bias signals to operate cascaded MOBILE-type circuits [4] are also shown (Figure 2b). A four phase (evaluation, hold, reset and wait) overlapping clocking scheme is used. Second stage evaluates (rising edge of V_{bias2}) while the first stage is in the hold phase (V_{bias1} high). For a number of logic levels greater than three, four bias signals are required. In one clock period all the gates are activated. Data can be processed at a frequency determined by the operation speed of four chained MOBILE gates.

Figure 3 depicts its realization as a Multi-Threshold Threshold Gate (MTTG) [6]. MTTGs are a generalization of the conventional TGs in which there are K thresholds, $T_1,\ldots T_K$, rather than the usual single threshold, T. $K + 1$ serie connected RTDs are required instead of the two of the basic MOBILE. The output of a two-input two-threshold MTTG is 1 for $T_1 \leq w_1x_1 + w_2x_2 < T_2$ and 0 for $w_1x_1 + w_2x_2 < T_1$ and $T_2 \leq w_1x_1 + w_2x_2$. Clearly, for $w_1 = w_2 = 1$, $T_1 = 1$, and $T_2 = 2$, this corresponds to the two-input EXOR function.

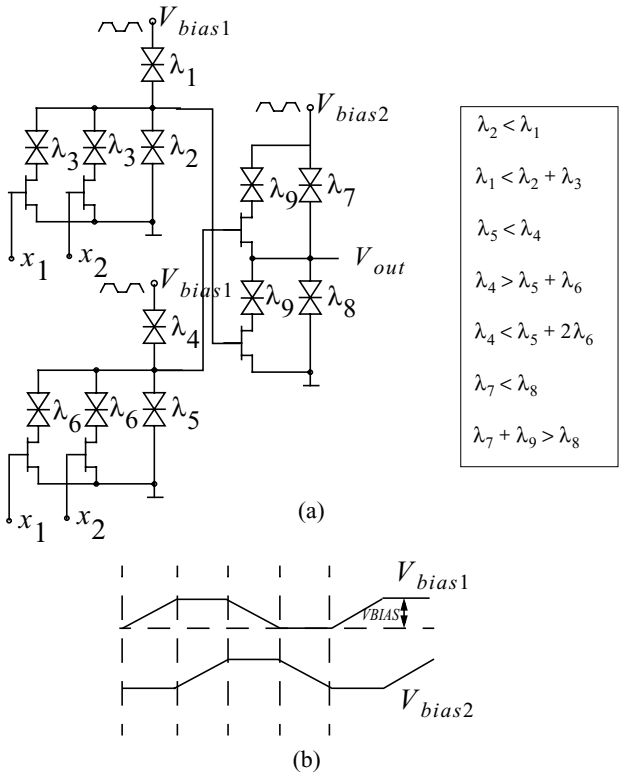

Figure 2.-(a) 2-input EXOR realized with a networks of TGs, (b) Bias scheme for nanopipelining

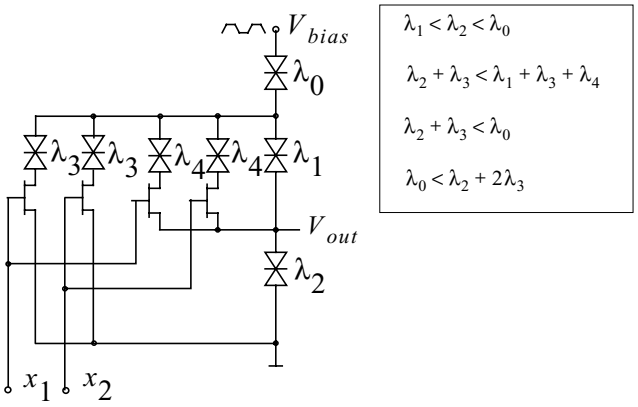

Figure 3.-2-input EXOR realized as an MTTG.

Figure 4 depicts a realization reported in [7] and which can be explained as a TG over an extended input set (GTG1). The two-input EXOR is realized as the TG with the extended set of input variables, $\{y_1, y_2, y_3\}$, given by $\{x_1, x_2, x_1 \wedge x_2\}$, $w_1 = w_2 = 1$, $w_3 = -2$, and threshold at 1.

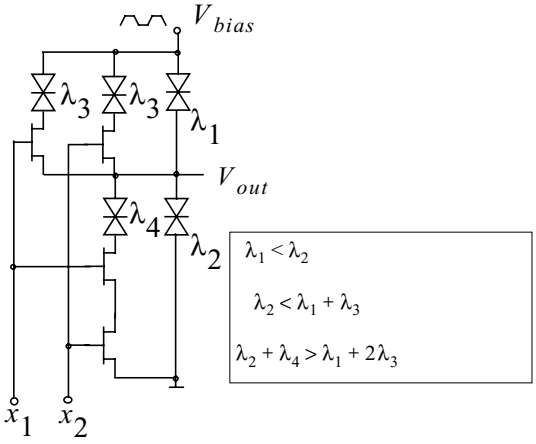

Figure 4.- 2-input EXOR from [7] (GTG1).

Figure 5 shows a realization using the logic style proposed in [8] (GTG2). This realization is obtained since the 2-input EXOR can be explained as a a TG over the extended set of input variables given by $\{x_1 \vee x_2, x_1 \wedge x_2\}$, $w_1 = 2$, $w_2 = -2$ and threshold at 1. Note that the two upper input branches in Figure 4 have been combined.

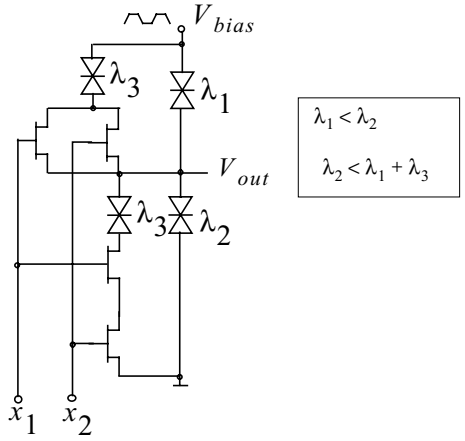

Figure 5.- 2-input EXOR from [8] (GTG2)

From the performance point of view, MOBILE TGs with only negative weights (all input branches in parallel with driver RTD) are superior since transistors associated to positive weights are larger to compensate reduced gate to source voltages, which increases capacitances. Thus, it would be desirable to obtain representations for the target functions with only negative weights. In addition, having all branches in parallel could enable additional combinations. We are able to obtain such a representation by applying a basic property of threshold functions which states that given a threshold function $f(x_n \ldots x_1)$, with weights w_i, $1 \le i \le n$, and threshold T, the function $f(x_n \ldots \bar{x}_j \ldots x_1)$ is also a threshold function with weights $w'_i = w_i$, $i \neq j$, $w'_j = -w_j$ and $T' = T - w_j$. For our EXOR example, this means that it can be represented as a TG over the set of input variables, $\{y_1, y_2\}$, given by $\{\overline{x_1 \vee x_2}, x_1 \wedge x_2\}$, $w_1 = w_2 = -2$ and threshold at -1 (applying the stated property to the represetation supporting GTG2). In addition, it can be described as a TG with a single input variable, given by $\{y_1\}$, $\{\overline{(x_1 \vee x_2)} \vee (x_1 \wedge x_2)\}$, $w_1 = -2$ and threshold at -1. Figure 6 depicts the circuit realization obtained from this model (GTG3) [9]. Note that areas of driver and load RTDs are interchanged with respect to GTG2 and that two inverters are required. Pipelined operation of cascaded GTG3 with the inverters which do not exist in previously reported MOBILE topologies has been validated through extensive simulations of several complex examples.

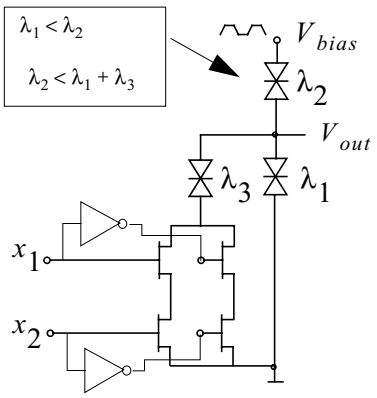

Figure 6.- 2-input EXOR from [9] (GTG3).

In order to compare the circuit architectures we have carried out simulations of three stage chains of the 2-input exor gates in a non commercial university InP technology in which RTD and transistors can be co-integrated. For this RTD, V_p is 0.21V, the peak current density 21KA/cm^2, the peak to valley current ratio is about 6.25 at room temperature and the capacitance is 4fF/μm^2. The transistor is a depletion HFET with threshold voltage -0.2V and minimum gate-length 0.6μm. Minimum gate-length transistors have been used. The sizes of the transistors have been selected to optimize the operating frequency for clocked V_{bias} between 0V and 0.7V (high voltage level VBIAS= 0.7V). In all the simulations, models for RTDs and transistors experimentally validated have been used [10]. In order to accept as correct one simulation, the three gate outputs are checked.Table I summarizes performance in terms of frequency and power-delay product obtained through simulations. Devices counts are reported too. Inverters required by the topology proposed in this paper have been included in the simulations.

Table I: Simulation results for 2-input exor. PDP = (P@F_{max})/F_{max}

Style	F_{max} (GHz)	PDP/ $PDP_{proposed}$	nº Devices
TGs	2.65	6.75	18
MTTG	1.75	3.25	11
GTG1	0.83	5.5	9
GTG2	1.14	3.25	8
GTG3 (including inverters)	4	1	11

In order to explore the application of the different described threshold based MOBILEs to logic design, we have designed *n*-bit adders using TGs, MTTGs and GTG3 exhibiting the best performance among the generalized TGs.

III. DESIGN OF N-BIT ADDERS

Figure 7, 8 and 9 show the logic diagram of nanopipelined carry propagation *n*-bit adders.

Figure 7 depicts the logic diagram of the TG nanopipelined *n*-bit carry-propagation adder. The main difference between the TG adder proposed in [4] and the presented here consists on the use of only negative weights in most of its gates, which has advantages in terms of speed. power and robutness.

Figure 8 depicts the logic diagram of the MTTG nanopipelined *n*-bit carry-propagation adder. Note that it uses modified full adders in which complemented inputs are processed in some stages. Each of them consist on athree input-minority and a three-input EXNOR in two levels. The avoidance of using a three-input EXOR gate, as in the reported *n*-bit adder scheme [11], is due to its really poor frequency.

The third design to be analized is the GTG3 nanopipelined *n*-bit carry-propagation adder shown in Figure 9. In this case the 3-input EXOR required for the FA is also implemented in two levels. Although when using a single gate, the frequency does not degradate as much as in the MTTG design.

Note that all the *n*-bits adders proposed require a two-level network for the full adder . This means the latency at the same operation frequency is the same for the three adders. Note that aditional buffers and inverters are required in the architectures to support pipeline.

Eight-bit adders have been designed to operate up to 1.33GHz using each of the architectures. Minimization of power has been the design target. Nanopipelined architectures for multipliers and divisors recently reported [12] can take advantage of these advanced proposed adders.

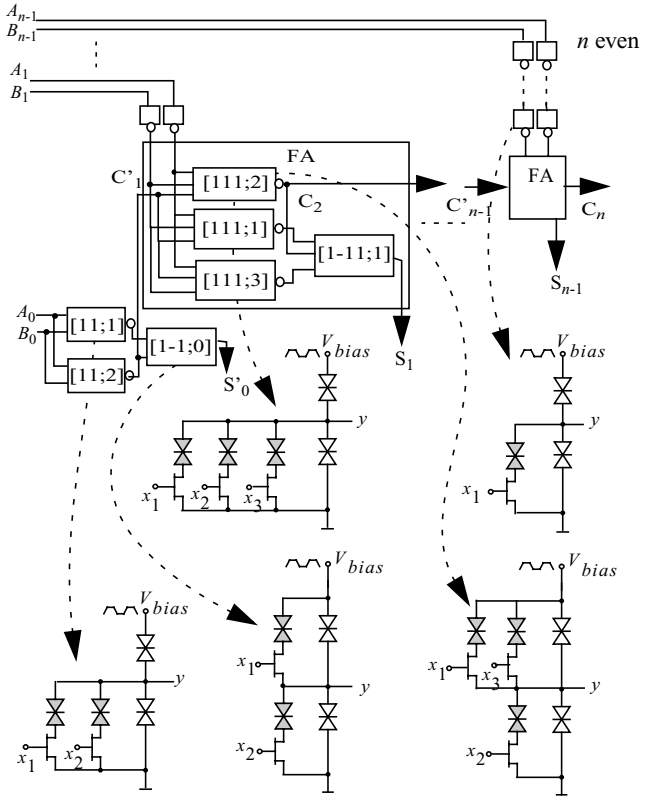

Figure 7.- TG nanopipelined *n*-bit adder.

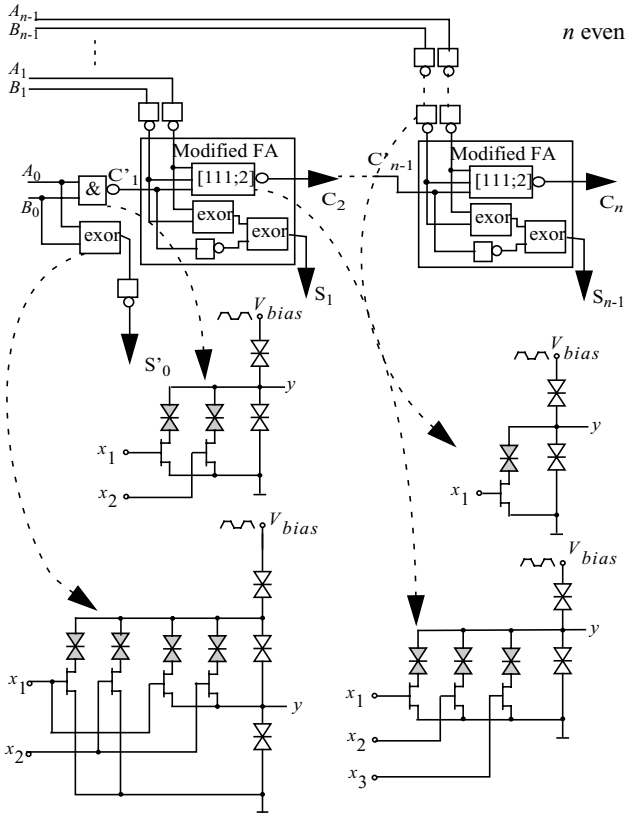

Figure 8.- MTTG/TG nanopipelined *n*-bit adder.

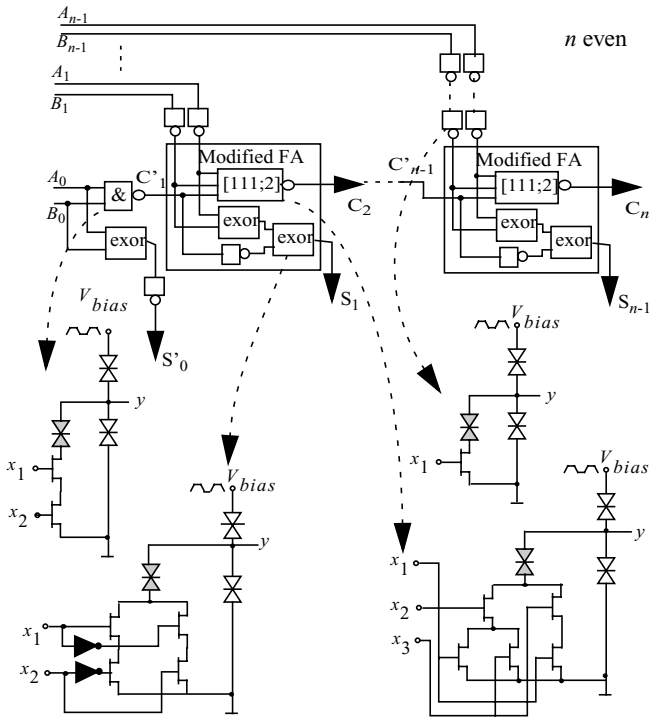

Figure 9.-GTG3 nanopipelined *n*-bit adder.

Table II summarizes a comparison between the three designs. For 8 bit adders operating at 1.33 GHz the design based in MTTGs has 14% more devices and consumes 35% more power than the GTG3, on other hand the design based in TGs has 11% more devices and consumes 3% more power than GTG3. The best result of speed corresponds to the GTG3 which has almost twice the maximum frequency exhibited by the TG adder design. Furthermore the power-delay product at maximum frequency is better in GTG3 design.

Table II. Comparison between 8-bit adders.

	Device Count	F_{max}(*G*Hz)	$P_{@Fmax}$(*m*W)	$P_{@1.33GHz}$(*m*W)	$PDP_{@Fmax}$(*p*J)
MTTG	599	1.89	16.82	15.43	8.90
TG	584	1.67	11.90	11.82	7.13
GTG3	605	3.13	15.20	11.47	4.86

IV. CONCLUSIONS

In this paper different designs of nanopipelined *8*-bit adder based on RTDs and HFET devices has been described. An extensive analysis of gates based on Threshold Logic concept has concluded with the choice of the best designs in terms of novelty, speed, power consumption and number of devices for the adder implementation. The selected gates are the TGs, MTTGs and GTG3. A comparative analysis has been carried between them. The proposed design with GTGs has demonstrated several advantages in comparison with TGs and MTTGs: higher speed, lower number of devices, and lower power consumption at the same operation frequency.

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