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TRANSMISSION ELECTRON MICROSCOPY OF SEMICONDUCTOR MATERIALS AND DEVICES

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Abstract

This paper surveys the application of transmission electron microscopy (TEM) to semiconductor materials and device technology. A broad spectrum of TEM studies requires the preparation of either plan-view or vertical sections; these sections are made using mechanical abrasion, chemical etching or ion milling or a combination of these procedures. A survey is then given of applications of TEM to four classes of studies of semiconductor materials and devices: the configuration of device features, crystallographic defects, lattice and atomic resolution imaging, and the analysis of phase and chemical composition.

Keywords:
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Introduction

Transmission electron microscopy (TEM) studies on semiconducting materials and devices are made with two types of sample configurations: plan-view sections parallel to the sample surface and vertical sections orthogonal to the sample surface (Fig. 1). Vertical sections are usually used for studies requiring information on depth distribution of features such as defects or device layers, while plan-view sections are particularly useful for studies of homogeneously distributed features of bulk materials and of interface structure.

A more precise description of the types of studies requiring vertical and plan-view sections can be made by first recognizing four major categories that comprise the field of TEM studies of electronic materials. One is the study of the configuration of device features of layers; these studies are usually made in conjunction with a process development or device failure analysis program. Studies of feature configuration such as step coverage, dielectric-semiconductor interface texture, shorts, etching and

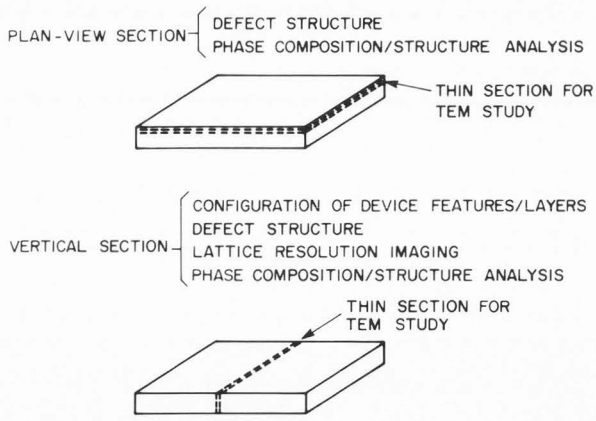


FIGURE 1

1. Two types of sample configurations used for TEM study, indicating the types of semiconductor materials and device studies usually made with each sample.

mask misalignment errors are usually made by TEM examination of thin cross-sections through device structures rather than examination of plan-view sections. A second category is the study of defect structures, such as these produced during crystal growth, implantation, oxidation or other thermal treatment. Bulk defects are usually studied with plan-view sections, while defects associated with an interface or surface require a cross-section for examination because of the changing character of these defects with depth. Lattice or atomic resolution imaging is a third category of study, and requires cross-section samples since these studies are usually made at an interface which runs parallel to the surface. The final category is phase composition and structure analysis, made with x-ray emission spectroscopy (XES) and electron energy loss spectroscopy (EELS), and electron diffraction, respectively; both types of samples are used for these studies.

The next section of this paper covers instrumental aspects of TEM that relate to electronic materials studies, and consists of three parts: sample preparation, structural and chemical analysis, and lattice imaging. The application of TEM to the four classes of semiconductor technology materials problems is described in the third section.

Instrumental

Sample Preparation

An essential difference between cross-section TEM studies of semiconductor devices and studies of bulk materials is, in the former case, the concentration of essential features in the top 1 − 2μm of a 250 − 510μm sample. Cross-section sample preparation methods have to address this problem. Both chemical and ion beam etching have been used to prepare thin (<100nm) sections for TEM study. Chemical etching is generally more material-selective and can be used for etching of a single phase material such as a silicon or GaAs substrate during preparation of a plan-view sample, while the preparation of a cross-section device sample by chemical etching alone often leaves regions of markedly different thickness, depending on the selectivity. Methods for preparing TEM samples of electronic materials and devices are listed in Table I and described below in greater detail.

Cross-section samples are usually prepared by a combination of mechanical abrasion and ion milling with argon.[10,25] Ion milling is typically performed with a 15° angle of incidence of the ion beam to a rotating sample, at 5kV and 0.5mA/gun. Lower power settings are used to prevent dissociation of III-V materials, and in addition liquid nitrogen sample cooling is often used for preparation of InP samples. The 1-2μm layer containing device features can be brought to an electron-transparent region of the sample by milling the sample until a hole forms, close to the device region (see Fig. 2). The wedge-shaped sample at the edge of a hole usually creates a region of 50 − 100μm that is thin enough for most TEM studies. The voltage can be lowered to 2kV during the last stage of ion milling in order to help remove surface damage.[34] A large number of samples can be ion milled at one time by following a procedure similar to that described in Section 2.3.3 of Reference 25, and shown in Fig. 3, thus avoiding the "slow turn-around time" reputation which sometimes characterizes TEM laboratories.

A novel method for preparing cross-section samples quickly, but at random sites across a surface, involves deposition of colloidal spheres on the surface followed by ion etching.[6] The spheres are electrostatically bonded to the surface. When polystyrene latex spheres are used, the differential etch rates between the spheres and a Si/Ge superlattice substrate is 1:6 in a CCl_4 ion beam, and by choosing small diameter spheres, several hundred thin cross-section samples can be prepared from one surface within one-half hour.[7]

A useful chemical etch for silicon is a 3:3:5 mixture of acetic acid, HF and HNO_3.[3] A number of different etches are reported for III-V compounds: InP, GaAs, InGaAsP and GaAlAs are etched in a solution of Br_2 in methanol. InP (but not InGaAsP) can be etched in a 1:1 solution of HCl and H_3PO_4,[33] 1:10 HF in HBr, or HF alone.[46] GaAs can be etched in 1:10 NH_4OH in H_2O_2.[31] Although anodic thinning (anodic oxidation followed by oxide strip) has been

Table I

TEM Sample Preparation Methods

Semiconductor	Sample: Materials	Sample: Devices	Configuration: Plan View	Configuration: Cross Section	Method
Si	√	√	√	√	lap, ion mill i) lap 240-400-500-3μm grit ii) ion mill
Si	√	√	√		
GaAs	√	√	√	√	lap, chem. polish i) lap ii) (Si) 3:3:5 HOAc: HF: HNO_3 (GaAs) 0.5% Br_2/MeOH
GaAs	√	√	√	√	lap, chem. polish, ion mill i) lap ii) polish 2% Br_2/MeOH iii) ion mill
III-V	√	√	√	√	chemical thinning [4] i) 2% Br_2MeOH ii) 0.5% Br_2MeOH or selective etch (plan view)
III-V	√		√	√	anodization [47] i) form 700nm oxide ii) strip oxide iii) repeat
III-V, Si	√	√		√	lithographic [6] i) deposit colloidal masks ii) ion etch

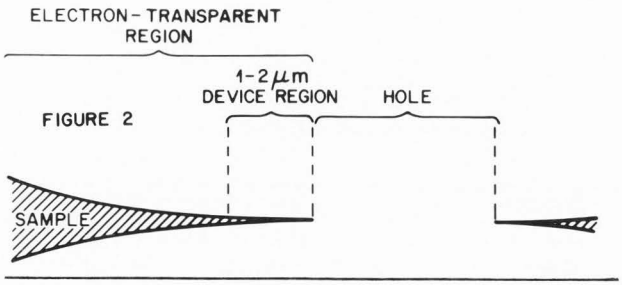


FIGURE 2

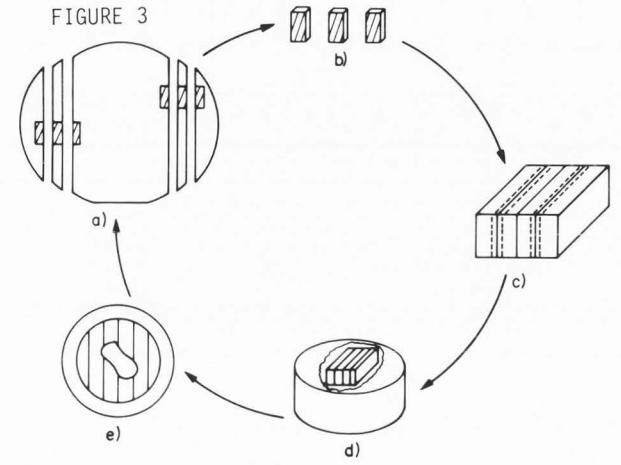


FIGURE 3

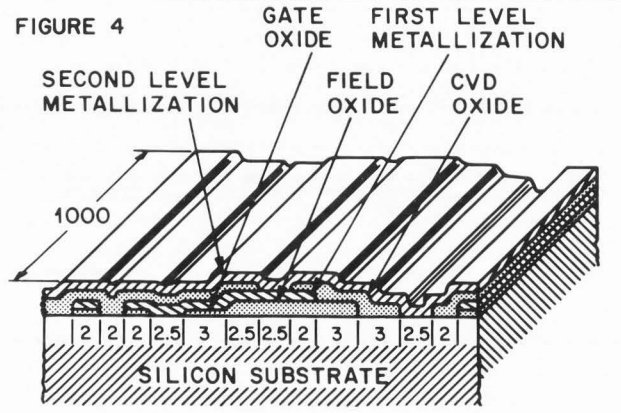


FIGURE 4

Figures

2. Schematic section through a TEM cross-section sample. The electron transparent region often extends a distance of 50μm or more.

3. Steps in preparation of vertical sections of device chips. Wafer is cleaved through chips (a) forming 1.5mm × 3.0mm pieces (b). These are epoxy bonded (c), polished to a thickness of about 40μm (d), cut and bonded to a 3.0mm-diameter Mo ring, and ion milled until a hole appears (e).

4. Schematic of a TEM test pattern for silicon NMOS device technology showing a 29μm repeat unit. All dimensions are in microns.

proposed as a sample preparation technique for GaAs, InP and Ge,[47] its use has not been widespread.

The brittle nature of InP and GaAs makes these materials unusually difficult to handle. Bonding a molybdenum grid to a sample for reinforcement helps to solve this problem.[4] Silicon, being less brittle, can be conveniently handled with a 3.0 mm-diameter molybdenum ring.[25]

For some TEM studies the location of the cross-section slice in the original device sample is not particularly critical. Studies of the oxide/silicon interface, the bulk defect structure of epitaxial layers, and the grain structure of aluminum are three examples of studies that do not usually require the precise location of the cross-section on the original device, since these features are present in almost any cross-section sample made at random. Other studies, though, require the capture of specific morphological features (such as a metallization-substrate contact or polysilicon passing over a field oxide edge) in an electron-transparent region of the sample. This is generally difficult to accomplish and adds enormously to the time needed to prepare a proper sample, since a number of cross-sections, made in the "wrong" place, have to be discarded before a proper sample is made. This problem is avoided by use of a "TEM test pattern" as described in Fig. 4.

The assumption basic to the use of a TEM test pattern is that all appearances of a particular morphological feature on a device wafer are identical. For example, all contacts of a top-level metallization to the substrate (in a given wafer) are expected to have the same characteristics and any problem such as the presence of an interfacial oxide, substrate defects, or an over-etched window would be exhibited by all contacts on that wafer. This assumption is not always valid, since crystallographic anisotrophy as well as processing differences which show up radically across a wafer can produce changes in the appearance of a given feature; however, for most studies the assumption is valid.

The TEM test pattern is designed to include all morphologically distinct features of a particular technology. Each feature appears (in one dimension) over a very short distance, say 1-2μm. Within a distance usually less than 30μm (29μm in Fig. 4) all features have appeared once; this "unit cell" is repeated a number of times over a total distance of 1-2mm. In the orthogonal distance each feature is extended to a distance of 1-2mm. It is a relatively simple matter to cleave or cut a section (parallel to the "short" direction of the unit cell) that contain a number of repeat units, and prepare a sample that is suitable for TEM study from this section. Since an electron transparent region (at the edge of a hole) usually extends a distance of more than 50μm, at least one repeat unit is captured within this region and TEM studies of all distinct features can be made within this repeat unit.

Table II summarizes the major problems which occur during sample preparation. The first four problems were discussed above. The last problem (small size) is particularly troublesome with laser samples which usually measure 200μm × 20μm or smaller. Such small samples are made part of a more easily handleable "dummy sample" by surrounding the sample with shims of the same material and similar thickness, and epoxy bonding the assemble to appear as one unit.

Structural and Chemical Analysis

A number of structural parameters (lattice parameter, strain, film thickness, orientation, crystal symmetry) as well as information on chemical composition, can be determined by using various configurations and accessories of the modern TEM instrument. Since none of these applications offers restrictions or advantages which are specific to semiconductor materials, only a few general comments are made regarding them.

Electron Diffraction

Conventional electron diffraction, which uses a parallel electron beam normal to the specimen surface (Fig. 5a), has been used for many years, primarily for identification of unknown phases. When a structural phase extends over a large area, cell parameter measurements can be easily made with an accuracy of 1%. The smallest area which can be studied in this way is limited to 0.5μm by lens spherical aberration and aperture design. Smaller regions, such as formed by metal-semiconductor interdiffusion and reaction, or small grains within a polycrystalline metal layer, require use of a convergent beam.

Convergent beam electron diffraction was introduced many years ago[19] and its modern use has been described.[39,48] When a convergent electron beam is used for sample illumination, the diffraction spots become broadened into discs at the back focal plan of the objective lens (Fig. 5b). Each disc contains an image of the field irradiated by the beam, which can be made as small as the beam diameter at the point of intersection with the sample (<10nm). The array of diffraction discs can include discs from higher order Laue zones, thus giving information on the three-dimensional structure of the crystal. In addition to providing identification of unknown phases, convergent beam diffraction also provides information on specimen orientation, strain field, lattice parameter changes and crystal symmetry.

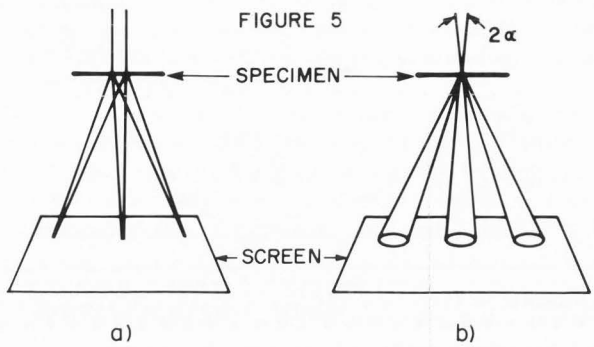
Chemical Analysis

Electron beam interaction with a sample volume can produce inner shell ionization yielding, in turn, electron transitions resulting in x-ray emission. The process whereby an incident beam transfers energy to an inner shell ionization has been used as the basis for the analytical procedure of electron energy loss spectroscopy (EELS) and has been described by Joy and Newbury[16] and others (of pp. 91-116 of reference 39). EELS is particularly useful for analysis of light elements.[15] Experimental measurements of the

Table II

TEM Sample Preparation Problems & Solutions

Problem	Type of Sample	Solution
brittleness	III-V Si	Mo reinforcement grid Mo reinforcement ring
indium drop formation during ion milling	InP	low T, slow mill
difficulty in locating desired device feature	VLSI circuits	use TEM test pattern
slow "turn-around" time	vertical sections	multiple-sample preparation
small size	laser (200 × 200 × 10μm)	imbed in "frame"



5. Illustration of conventional (selected area) electron diffraction (a) and convergent beam electron diffraction (b).

sensitivity limit for detection of nitrogen in a silicon matrix give a concentration limit of about 0.1 atom %. At a minimum detectable mass limit of 2.5×10^6 atoms (carbon in a silicon matrix[23]) and a sample of 100nm thickness, a beam diameter of 800nm is required. Thus, as is always the case with chemical microanalysis, there is a trade-off between sensitivity and spatial resolution.

Two major problems for the application of EELS to chemical microanalysis of semiconductor materials are the need for very thin samples (to avoid multiple scattering events) and chemical interference from absorbed gases. For example, it is difficult to analyze for the presence of oxygen or carbon in InP when both surfaces of the TEM sample are covered with contaminating layers that contain these elements.

Analysis of x-ray emission spectra serves as the basis for x-ray emission spectroscopy (XES) and is frequently used for microanalysis in a TEM instrument. The sensitivity limit for detection of nitrogen under typical operating conditions is about 2×10^4 atoms and a minimum mass fraction of 0.6 at % (ref. 48, p. 83). With a 100nm-thick sample, a beam diameter of 30nm is required for detection of nitrogen at these limits. This analytical method is discussed in ref. 48, pp. 55-90 and in numerous places

in the book by Hren, Goldstein and Joy (see reference 23).

Lattice and Atomic Structure Imaging

High resolution images can be obtained which reveal the lattice planes or atomic structure of crystalline materials. The (220) and (111) planes of GaAs, InP, and silicon can be imaged if the line-to-line resolution of the instrument is better than 1.9Å. Careful study on the proper specimens can also display the open atomic channels in these structures, revealing the atomic structure. The principles of lattice parameter and atomic structure imaging of semiconductor materials are the same as for non-semiconductor materials, and are described in references 48 and 41 and in other literature.

Semiconductor Material Studies

As described above, TEM studies of semiconductor materials and devices can be grouped into four major categories: studies of the configuration of device features or layers, studies of defect structure, lattice or atomic resolution imaging, and phase or chemical composition analyses. These are not mutually exclusive; lattice imaging studies, for example, can be used to reveal information on the presence of atomic disorder or extended crystallographic defects. Many studies in the first and fourth categories are made in conjunction with exploratory development or process monitor programs, and as such do not reach the published literature.

Configuration of Device Features

The development of VLSI circuits with dimensions of 1μm and below means that light microscopy has an increasingly minor role, and even scanning electron microscopy (on bulk samples) becomes severely limited as a tool for obtaining information on the morphology of device features. Most of the applications of TEM to problems of device feature morphology are centered around questions about layer thickness, step-coverage, and shapes of etched features and junctions. These questions require spatial resolution better than 0.1μm, and most problems can be successfully analyzed with a resolution limit of 0.5 nm.

An early study of silicon microcircuits by TEM was published by Ham, et al. in 1977.[10] They described the preparation of both plan-view and cross-section samples, and the desirability of having a circuit region of "high periodicity" (anticipating the need for a TEM test pattern) for the latter. This paper showed the presence of silicon "horns" at corners of thermally oxidized silicon, and noted that these sharp corners had previously escaped detection in SEM studies.

A large number of examples of TEM studies of MOS VLSI circuits is found in the book by Marcus and Sheng.[25] These studies were made on circuit wafers containing TEM test patterns, and demonstrate the application of TEM analysis for determining the morphology of oxides, metallization, vertical contacts between layers, and other features formed by VLSI processing. All mask sets used to fabricate devices and experimental wafers in these studies contained TEM test patterns in four locations, and it was only through the use of test patterns that useful information could be fed back to processors and experimentalists within 2 – 3 days.

TEM studies also have been made of the shapes of oxide walls,[24,38] the configuration of the polysilicon/oxide interface,[3,13,26] and the morphology and grain structure of various metallizations.[18,28,45]

Most TEM/STEM studies of integrated circuits have been based on silicon technology, and studies of devices based on III-V materials are expected to grow as III-V integrated circuit technology assumes greater importance.

Defects

A number of exciting studies have been made by using TEM to characterize defects in silicon and in III-V materials and devices. Early work on TEM analysis of dark line defects (DLDs) in GaAlAs/GaAs double heterostructure lasers[32] was followed by a number of additional publications on that material, and more recent TEM studies of InGaAsP/InP lasers reflect a current interest in longer wavelength laser technology. Dislocation slip was found to occur in optically degraded InGaAsP laser material.[22] Further studies showed that dislocation slip motion parallel to a laser stripe causes rapid degradation, while slow dislocation climb (10^{-11} cm sec^{-1}) is less important as a degradation mechanisms in stressed quarternary lasers.[14,44] Slip dislocations are thought to originate from the stress induced by metallization contact to the p-layer.[14] Dark spot defects (DSDs) formed in stressed lasers were found to increase in number with increasing laser degradation, and analysis showed that they consisted of platelike precipitation and dislocations.[46] Similar studies showed that other "dark defects" originated from a misfit strain and mechanical damage introduced during epitaxial growth.[44] TEM studies have also been applied to the problem of understanding the high threshold on these lasers and has revealed a layer of atomic disorder at the mesa sidewall/epi regrowth interface that explains high threshold and other data on laser leakage.[8]

A major source of raw data for implantation model studies is TEM analysis of implanted material. These structural studies are often made in conjunction with Rutherford backscattering analysis, which gives information on the chemical profile and lattice disorder in the implanted region.

Implantation of ions into semiconductor crystals produce damage sites. As the ion dose rate is increased, TEM micrographs show that the damaged regions created by the individual implanted ions overlap, eventually creating an amorphous layer.[35] For silicon at liquid helium temperature a crystalline to

amorphize transition occurs at a threshold implantation energy of 12 eV/atom. Further increases in the dose or a rise in the substrate temperature result in regions essentially free or low in defects due to the annealing out of the radiation-induced damage.[29] Substantially further increases in dose cause additional defects to appear.

While many TEM studies have been made in the 1970's of the damage structure introduced in silicon as a function of dose, energy, ion species, and anneal time and temperature, recent work on silicon has looked at more complex questions involving implantation through oxide layers[37] and implanted layers treated by rapid thermal anneal (RTA).[36] A very short (10 − 20 sec) RTA treatment at 1100°C is considerably more successful in annealing away implantation damage than a 30-minute furnace anneal.[9] These RTA experiments demonstrate the ability to perform anneal on implanted semiconductors under conditions that produce very little bulk diffusion, particularly when the semiconductor is pre-amorphized.[9]

TEM studies of implantation-induced defects in III-V materials are not as extensive as work with silicon. SiH_2^+ implantation into InP at a dose of 10^{14} ions/cm^2 produce an amorphous layer when the substrate is at room temperature, but not when the InP is held at 200°C; different kinds of structural defects are then formed when the samples are subsequently furnace annealed at 650°C.[5] The surface amorphous layer of GaAs implanted with Zn^+ or Se^+ can be converted to polycrystalline material, single crystal material with defects, or defect-free material by laser annealing, depending on the laser energy used and the corresponding depth of penetration of the laser melted region.[12] Redistribution of Cr in Cr-doped GaAs following boron implantation was shown to occur by the gettering action of a layer of GaAs containing Ga and As interstitials displaced by the implantation; the interstitials coalesce into small cluster sites, rendering them immobile during anneal.[21]

Considerable attention has been given lately to attempts to grow single crystal material over amorphous surfaces. A recent paper describes TEM methods for characterizing the overgrowth of silicon on oxidized silicon, using an opening in the SiO_2 for seeding the overgrowth during silicon deposition.[27] This study showed that a faulted layer of crystalline silicon can form, and that the faults are likely the result of strain resulting from differential thermal contraction during cooling.

Lattice and Atomic Resolution Imaging

Most of the TEM lattice imaging studies of semiconductors have been of heterojunction interfaces with silicon. Amorphous SiO_2 over single crystal silicon contains 30Å inclusions of β-cristobalite near the interface with a fixed crystallographic relationship to the substrate in spite of an intervening layer of amorphous oxide.[34] Thermally oxidized phosphorus-doped polysilicon shows enhanced oxidation at grain boundaries when oxidation is carried out in wet O_2 at 800°C, and high resolution TEM shows these regions to be crystalline with a fringe periodicity of 0.67nm.[3] Higher temperature oxidation shows no oxidation enhancement at grain boundaries.[3,26]

Lattice image studies of epitaxially deposited silicon over sapphire show that the interface is fault-free.[34] The absence of misfit dislocations, in view of the large lattice mismatch between the two layers, is ascribed in part to reconstruction of the top oxygen layer of the sapphire. These results are in slight disagreement with earlier lattice resolution image studies[2] which showed a transition region of three to five lattice plan thickness which accommodated the misfit.

High resolution studies of AlGaAs/GaAs superlattices show uninterrupted lattice planes crossing the interfaces.[30] Vacancy and interstitial defects resulting from As^+ implant into silicon are revealed in atomic resolution TEM studies.[20] In these studies, models of defects are used to generate computed images which are then compared with experimentally obtained images. The interface between the heavily irradiated amorphous phase and the single crystal silicon lattice is closely shown in atomic resolution images from another study;[29] also demonstrated in this study are regions of small (~10Å wide) amorphous cascades in the host lattice, and inclusions of crystalline regions in an amorphous matrix.

Phase and Chemical Composition

High resolution images of cross sections through superlattices can reveal a distinction between the layers when the atomic composition or structure factors are sufficiently different. Thus, the phases of a AlAs-GaAs superlattice[17] or a $Al_{.2}Ga_{.8}As$-AlAs superlattice[40] are distinguishable while the layers could not be clearly distinguished in an earlier study where the phases were more closely matched in atomic composition.[30] A superlattice consisting of amorphous Ge and Si layers (repeat distance 27Å) is imaged in another recent study;[1] the TEM sample was prepared by a novel method described earlier in this paper.

The STEM has recently been applied to the study of the phase and chemical composition of the spinodally decomposed InGaAsP quarternary layer, which is the active region of long wavelength InP lasers. The quasi-periodic contrast seen in TEM images is consistent with spinodial decomposition into regions which differ by 10^{-3} in their lattice parameter.[42,43] A slightly earlier work studied the compositional variations across phase boundaries using x-ray emission spectroscopy and found corresponding variations in the Ga to As ratio.[11]

Summary

This paper reviews the application of transmission electron microscopy to the study of semiconductor materials and devices. Techniques for preparing cross-section samples of devices were

described, including use of a special test pattern chip on semiconductor device wafers which greatly facilitates the application of TEM methods to semiconductor processing problems. Significant features were described of the specific application of electron diffraction, chemical analysis, and lattice and atomic structure imaging to semiconductor materials.

A survey was then given of the application of TEM methods to four classes of studies, the configuration of device features, crystallographic defects, lattice and atomic resolution imaging, and phase and chemical compositional analyses. It is likely that the future application of TEM methods will see growth in all four categories. The push toward smaller dimensions creates a new class of processing materials in silicon technology, and the development of optoelectronic integrated circuit technology based on III-V compound semiconductors is only just beginning. Improvements in instrument resolution and in the modeling and understanding of electron imaging are expected to encourage the application of TEM methods to the study of defect structures and to the use of lattice and atomic resolution imaging.

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Discussion with Reviewers

D. B. Williams: Heating in excess of 200C can easily be introduced during ion beam thinning and in combination with the introduction of vacancies and interstitials could result in substantial diffusion occurring during the specimen thinning process. Do you have any evidence that such effects occur and how do you minimize it? Is there any way to distinguish ion-beam thinning defects from other (deliberately introduced) defects?

T. J. Shaffner: What types of damage can occur during sample preparation and how can it be detected and avoided?

Author: The main artifacts produced by the ion milling of semiconductors materials are the effects of the disproportionation of some III-V compounds such as the formation of liquid indium drops on InP caused by the preferential loss of phosphorus, and the formation of a thin amorphous layer on surfaces such as silicon (Ray Carpenter, Arizona State University, private communication). Indium drop formation can be avoided by lowering the sample temperature and using a lower beam power, and the silicon amorphous layers can be etched off the sample. Temperature rise is not a major problem. Experimental measurements showed temperature rises of less than 50°C in one case (Zhdanov GS, Vertsner VN. (1966). The heating of objects under an electron beam, Radiotekhn Elektron, 1901-1904) and less than 150°C in another experiment (Barber DJ. (1970). Thin foils of non-metals made for electron microscopy by sputter-etching, J. Mat. Sci. 5 1-8.).

T. J. Shaffner: What factors influence how many mounts one should prepare and how many micrographs can be considered with confidence to represent the material or device?

Author: If a device feature on a silicon chip is to be studied and a TEM test pattern is available, then only one sample is needed (the rate of success at producing a TEM sample of silicon with an experienced operator is nearly 100%). If one wishes to study either a silicon device feature or feature of silicon material (defects, for example) that is known to be non-uniformly distributed through a wafer, then representative TEM samples must be made from different areas. The situation with III-V materials and devices is more complicated because of the more brittle nature of these materials, and some redundancy is needed to cover the loss of samples due to breakage.

T. J. Shaffner: How important is high voltage (>300 keV) in the lattice imaging mode? While resolution can be improved, specimen damage must be kept at a minimum. What is the current status of high voltage transmission electron microscopy? How useful do you think these machines will be in the near future?

Author: The main advantages to high voltage TEM operation are i) greater transparency and the ability to use thicker samples for study, ii) improved resolution, and iii) less absorption effects such as contamination, temperature rise, and background noise in EELS and XES spectra. The main disadvantage is displacement damage resulting from "knock-on". Values reported for the energy threshold for displacement damage in silicon vary from 145 to 173 keV (Cosslett VE (1980). Radiation damage by electrons with special reference to the knock-on process, Inst. Phys. Conf. Ser. No. 52 1980 chapter 5 277-282). This damage can be a severe problem at beam energies above 300keV, depending on the nature of the problem under study.