Fast and Area Efficient Multi-Input Muller C-Element Based on MOS-NDR

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***Abstract*—A new multi-input Muller C-element based on a MOS-NDR device is proposed in this contribution. This design overcomes some drawbacks of previously proposed structures. A comparison in terms of area, delay and power consumption over another efficient CMOS Muller C-element circuit has been performed, resulting that our structure improves this performance.**

I. INTRODUCTION

Resonant tunnelling diodes (RTDs) are considered today as one of the most mature types of quantum-effect devices, already operating at room temperature, and being promising candidates for future nanoscale integration. RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics, which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies [1]. Most of the reported working circuits have been fabricated in III-V materials while Si-based tunnelling diodes compatible to standard CMOS fabs are currently an area of active research [2].

Circuit ideas coming from RTD-based designs can be interesting even in an "all CMOS" environment. To prove this, we have selected an application which can be very efficiently implemented by using one RTD and we have substituted it by a MOS circuit able to emulate its NDR characteristic. So, a novel multi-input Muller C-element circuit is proposed and analysed in this paper, concluding that the CMOS implementation of the original RTD-based idea for its realization is more efficient than other conventional C-element structures.

The paper is organised as follows: in Section II, the MOS-NDR device is described. The operation principle of the Muller C-element circuit is studied in Section III. Section IV describes the proposed structure. A comparative area, delay and power consumption analysis between two 0.13µm Muller C-elements, the MOS-NDR-based and one previously reported, is presented in Section V. Finally, some key conclusions are given in Section VI.

II. THE MOS-NDR STRUCTURE

Figure 1*a* shows the structure of the MOS-NDR device integrated in the Muller C-element circuit. It consists of two NMOS and two PMOS transistors [3].

The current-voltage characteristic of the MOS-NDR device is shown in Figure 1*b*. The first positive differential resistance (PDR) and the NDR zones of the *I-V* characteristic is

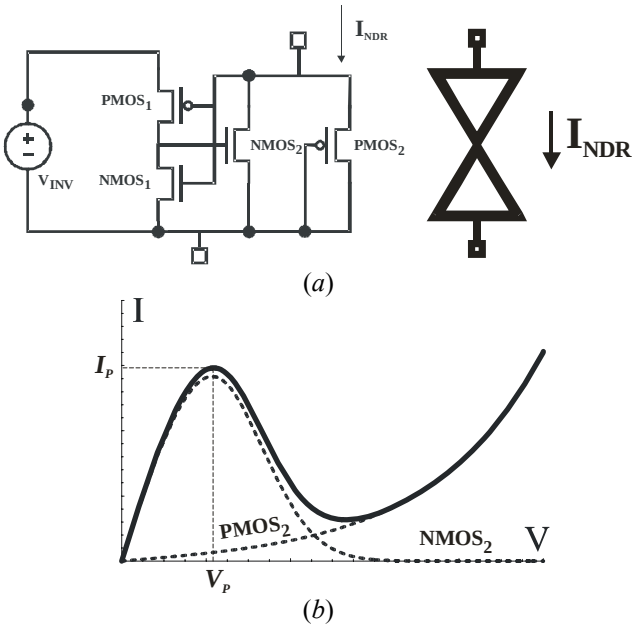

Figure 1. (*a*) MOS-NDR circuit diagram and equivalent symbol. (*b*) I-V characteristic of the MOS-NDR device. Dashed lines represent the current contribution of transistor $NMOS_2$ and $PMOS_2$.

obtained through the current of a NMOS transistor ($NMOS_2$) whose gate-to-source voltage is modulated by the output voltage of the CMOS inverter made up by $NMOS_1$ and $PMOS_1$ and biased by V_{INV}. This inverter is biased with the voltage source V_{INV}. The second PDR region comes from the contribution of $PMOS_2$ transistor. Both currents have been shown as dashed lines in Figure 1*b*.

The peak voltage (V_p) and current (I_p) of the *I*-*V* characteristic in Fig. 1 can be modified by setting up properly the sizes of the transistor. In this way, I_p is increased with the width of $NMOS_2$. Assuming that all transistors have the same gate length, the position of V_p is controlled by the ratio between the widths of $NMOS_1$ and $PMOS_1$. In this way, higher values of V_p are obtained by decreasing the ratio $W_{NMOS,1} / W_{PMOS,1}$.

III. Operation Princicple of the Muller C-element

A Muller C-element is a circuit widely used in the design of self-timing circuits to perform the functions "*and*" of events (transitions 1→0 or 0 → 1). Its output is made equal to the value of the inputs after all of them reach the same value; on the contrary, the output remains the same. The equation which defines a Muller C-element of N inputs is given by $Q=\{x_1 \cdot x_2 \cdot \ldots \cdot x_N\}+\{x_1+ x_2+\ldots+ x_N\} \cdot q$, where x_i, (i=1,…, N) are the primary input, Q the next state variable, and q the present state variable.

The NDR devices latching properties can be exploited to reduce the complexity of the design, since a Muller C-element may only require one NDR and as many active elements (NMOS transistors in this case) as inputs signal [4]. Figures 2*a* and 2*b* show the circuit diagram of a basic Muller C-element of two inputs along with its operation principle, respectively. When both transistors are biased such that their total current is smaller than the valley current of the NDR, output voltage "L_1" is obtained. When the total current through the input stage is larger than the peak current of the NDR, solution corresponds to "H_1". Finally, when the current through the transistors is between the peak and the valley currents, output levels "L_2" or "H_2" could be obtained.

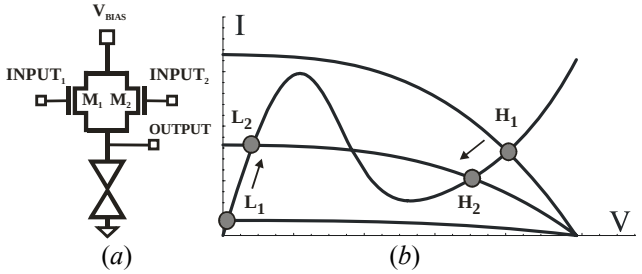

Figure 2. (*a*) Basic Muller C-element circuit diagram (*b*) Operation principle of a basic Muller C-element, depicting all feasible solutions of the output voltage.

Solution "L_2" corresponds to a situation in which originally the output was "L_1" and one input changes its state. Similarly, "H_2" comes from an original situation in which solution "H_1" was active. Solutions "H_1" and "H_2" are associated to a high level of the output, whereas "L_1" and "L_2" corresponds to a low level.

Implementing an N-input Muller C-element would require the only addition of input transistors until N of them are in parallel. Unfortunately, this structure is not efficient for a large number of inputs. In such situation, the difference between the total current through the input stage when N-1 inputs are '1' and the case in which all inputs are '1' would be so small that the circuit could not be able to switch to the appropriate state.

In this paper, we exploit ideas from the RTD-based design domain to obtain a MOS multi-input Muller C-element which compares very favorably with a well known design.

IV. The Proposed Muller C-element Structure

Figure 3 depicts the block diagram of our circuit, which have been divided into two parts in terms of their functionality. They have been denoted as "Preprocessing" and "Core".

A. Preprocessing

This block receives the N-input set and generates two intermediate signals, s_1 and s_2, that overcome the multi-input drawback of the basic Muller C-element structure described at the end of the previous Section.

Signal s_1 is '0' when all inputs are equal to '1', and '1' for the other combinations of logic levels of the input set (i.e. an N-input NAND gate). The circuit corresponding to signal s_1 is depicted in Figure 4*a*. In this case, the N-inputs set is connected to N PMOS transistors. The NMOS transistor gate-to-source voltage is fixed to a constant voltage V_{NMOS}.

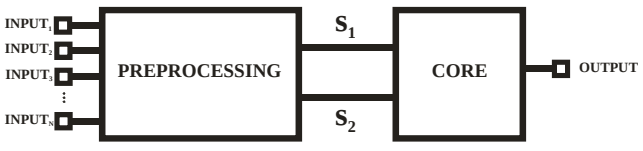

Figure 3. Block diagram of the proposed Muller C-element.

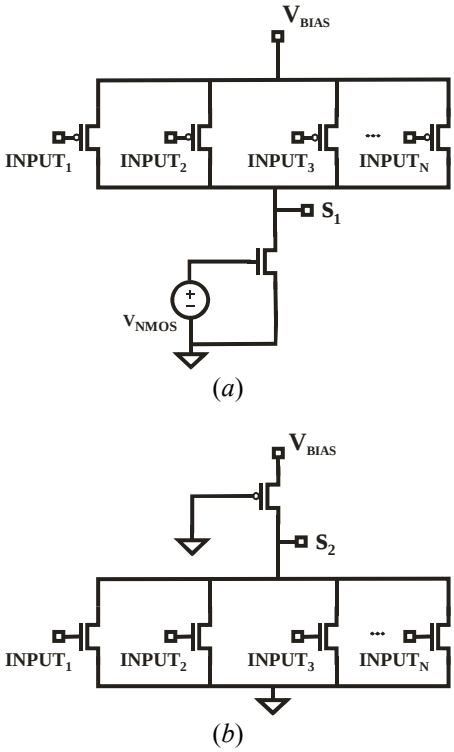

Figure 4. (*a*) Signal s_1 preprocessing circuit. (*b*) Signal s_2 preprocessing circuit.

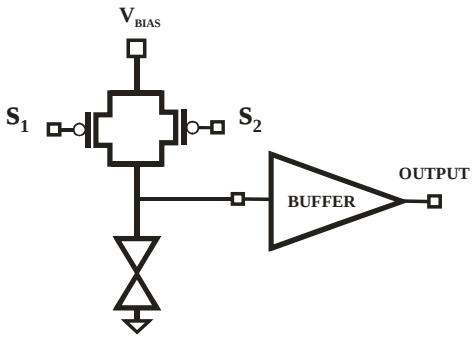

Figure 5. Circuit diagram of the Core part of the Muller C-element circuit.

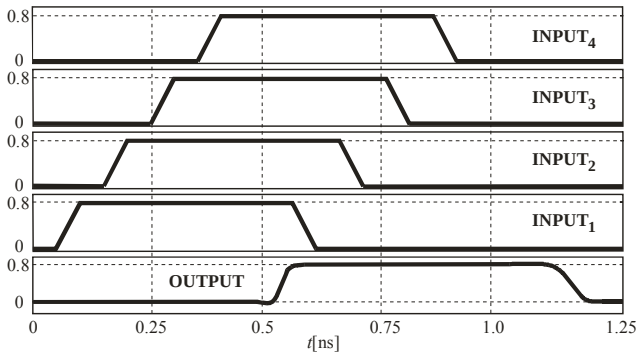

Figure 6. Waveforms of the input set and the output for the proposed 4-input Muller C-element.

Signal s_2 is generated as follows: when all inputs are set to '0', s_2 is '1', and otherwise s_2 is '0' (i.e. an *N*-input NOR gate). Figure 4*b* shows the circuit from which signal s_2 comes from. It consists of the parallel connection of *N* NMOS transistor, and a PMOS transistor with its gate connected to ground.

B. Core

Figure 5 shows the circuit diagram for the "CORE" block. It consists of two PMOS transistor and one MOS-NDR device. This part of the structure directly receives signals s_1 and s_2 from the preprocessing block. Those signals directly feed the gate of both PMOS transistors. The operation principle of this circuit is similar to the one described in Section III for a two-input Muller C-element. A buffer consisting of two CMOS inverters has been added in order to regenerate the final output signal.

C. A case example: the 4-input Muller C-element

In order to show the operation of our structure, a 4-input Muller C-element is analyzed. An input set of four pulse trains have been used. Minimum and maximum input voltages are $0V$ and $0.8V$ respectively. Each signal has 1ns of period and the delay between each one is 100ps. We have the same value for V_{bias}, V_{INV} and V_{NMOS}, $0.8V$.

Figure 6 shows the waveforms of the input set and the output. When the last input signal ($INPUT_4$ in the Figure) switches from '0' to '1', the output commutes to '1' state as well. Similarly, when $INPUT_4$ goes down to '0', the output switches to the low state.

V. SIMULATION RESULTS

In this Section, simulation results using the Cadence® Toolset and transistors from the UMC 130nm design kit have obtained.

Since the Power-Delay Product has a small demand on the chip area consumption, it is difficult to be used in applications with the stringent chip area consumption. The performance of the proposed structure has been measured in terms of the Power-Delay-Area Product (*P-PDA*). The *P-PDA* enhances the significance of the chip area consumption besides the power consumption and the delay time [5]. It is defined as,

$$P - PDA = P_{AV} \cdot D_{AV} \cdot A \qquad [1]$$

where P_{AV} is the average power consumption, D_{AV} is the average delay (defined as the mean between the rise and fall delay) and A is the total area of the circuit. Since the gate length of all transistors is the same, we have defined the *normalized P-PDA* ($P\text{-}PDA_N$) as,

$$P - PDA_N = P_{AV} \cdot D_{AV} \cdot \sum_i w_i \qquad [2]$$

where $\Sigma_i w_i$ is the sum of all transistors widths.

Simulations have been performed through a set of inputs consisting of pulse trains of 50ps of rise and fall times, 1ns of period and a range between $0V$ and $0.8V$. Bias voltage has been set to $0.8V$. Results are presented in TABLE II for the 2, 4, 8, 16 and 32-input structures.

TABLE I. PROPOSED STRUCTURE

	Power-Delay-Area				
	2 inputs	***4 inputs***	***8 inputs***	***16 inputs***	***32 inputs***
P_{AV} (μW)	350.77	376.14	405.57	459.91	516.09
D_{AV} (ps)	263	268	296	327	396
$\Sigma_i w_i$ (μm)	28.08	39.08	66.40	102.00	182.00
$P\text{-}PDA_N$ (pJ·μm)	2.59	3.94	7.97	15.34	37.15

In order to check the efficiency of our structure, we have compared it with the multi-input Muller C-element circuit proposed by Wuu and Vrudhula [6]. To make comparisons as fair as possible, we have simulated them by using transistors from the 130nm UMC design kit. Simulation results are given in the following table, marking the value of the *P-PDA* for which this structure is more efficient than our proposed circuit.

TABLE II. WUU-VRUDHULA STRUCTURE

	Power-Delay-Area				
	2 inputs	***4 inputs***	***8 inputs***	***16 inputs***	***32 inputs***
P_{AV} (μW)	14.01	18.10	73.05	260.27	416.62
D_{AV} (ps)	289	294	442	471	514
$\Sigma_i w_i$ (μm)	8.16	11.28	48.60	119.16	280.16
$P\text{-}PDA_N$ (pJ·μm)	0.03	0.06	1.57	14.61	59.99

Delay in our structure is always inferior to the traditional one, being the opposite the behavior of the power. However, our structure is more efficient than the previous one in terms of the $P\text{-}PDA_N$ for N>16, as shown in Figure 7, where this $P\text{-}PDA_N$ has been represented versus N. Moreover, the ratio between the PDA_N of both structures increases for larger values of the number of inputs, as shown in TABLE III.

TABLE III. $P\text{-}PDA_N$ RATIO

$P\text{-}PDA_{N,Wuu\text{-}Vrudhula}$ / $P\text{-}PDA_{N,Prop}$				
2 inputs	***4 inputs***	***8 inputs***	***16 inputs***	***32 inputs***
0.01	0.02	0.20	0.92	1.61

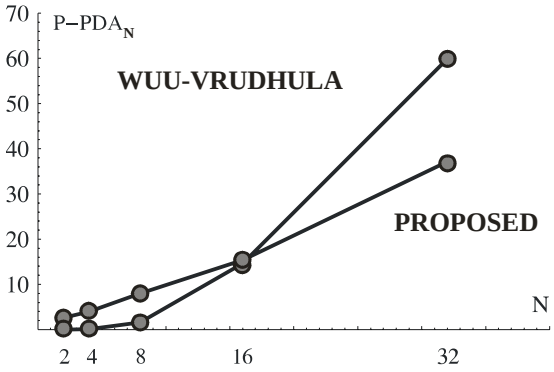

Figure 7. Power-Delay-Area product (normalized) vs. N

VI. CONCLUSIONS

A new multi-input Muller C-element circuit has been presented which takes advantages of the self-latching properties of NDR devices. It has been demonstrated to improve the power-delay-area product performance over a well known structure when the number of inputs increases.

ACKNOWLEDGMENT

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