

# Insect-Vision Inspired Collision Warning Vision Processor for Automobiles

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## Abstract

Vision is expected to play important roles for car safety enhancement. Imaging systems can be used to enlarging the vision field of the driver. For instance capturing and displaying views of hidden areas around the car which the driver can analyze for safer decision-making. Vision systems go a step further. They can autonomously analyze the visual information, identify dangerous situations and prompt the delivery of warning signals. For instance in case of road lane departure, if an overtaking car is in the blind spot, if an object is approaching within collision course, etc. Processing capabilities are also needed for applications viewing the car interior such as “intelligent airbag systems” that base deployment decisions on passenger features.

On-line processing of visual information for car safety involves multiple sensors and views, huge amount of data per view and large frame rates. The associated computational load may be prohibitive for conventional processing architectures. Dedicated systems with embedded local processing capabilities may be needed to confront the challenges. This paper describes a dedicated sensory-processing architecture for collision warning which is inspired by insect vision. Particularly, the paper relies on the exploitation of the knowledge about the behavior of *Locusta migratoria* to develop dedicated chips and systems which are integrated into model cars as well as into a commercial car (Volvo XC90) and tested to deliver collision warnings in real traffic scenarios.

## 1. Introduction

**M**aking cars safer is one of the major challenges of the automotive industry. Future cars might be ideally expected to “behave” following laws similar to those formulated by Isaac Assimov for robots. Namely: (1) a car should not injure a human being, or, through inaction, allow a human being damage; (2) a car must obey orders given by human beings, except that these orders are in conflict with the first law, and; (3) a car must protect its own existence as long as such protection does not conflict with neither the first nor the

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second law. The challenge of increased safety requires different innovations among which the enhancement of *car smartness* is of primary importance. A smart car should primarily be able of *sensing* its state: engine parameters, cinematic parameters, passengers typology and movements, position relative to the road, obstacles, ... But just sensing is not enough; smart cars must also be capable of *processing* the acquired data to either giving information to the driver or eventually taking control [1], [2].

Out of the many sensor types, it is generally understood that *optical sensors* (devices to acquire images) and *vision systems* (systems to acquire, process and extract the information from image flows) will be key ingredients in *passive* and *active* safety systems of future cars [3], [4]. Safety-system roadmaps envisage the use of many vision devices per car; some of them looking at *outside* the vehicle and others looking at the *inside*. Inside vision sensors will be used to monitor sizes, positions and movements of passengers and hence to control airbag deployment in case of crash [5]. They will also be employed to analyze the driver status; for instance, to detect drowsiness [6]. Furthermore, car architects may take advantage of the availability of vision devices to realize not-safety-related tasks such as human-computer-interface. Regarding outside sensors they will serve, among other tasks, to keep the car within road lanes, to calculate proper speed and distance of the car relative to others and to detect either objects or cars approaching on a *collision course*.

Figure 1 compiles potential applications of vision for cars. Vision will be used in combination with other sensor systems (radar [7], lidar, etc.) to support the development of future *advanced driver assistance systems (ADAS)* capable of taking full control of the car engine, brake and steering in order to avoid accidents [8]. However the endeavor to incorporate vision to cars is demanding. Apart from the typically long automotive design cycles (several years) the development of vision for automobiles is slowed down by the challenges which confront the analysis of rapidly changing image flows in *real-time*. On the one hand these challenges are due to the *huge amount of data* which

images contain. On the other hand, they are motivated by the complex ways in which the safety-relevant information is encoded into *spatial* (intra-frame variations) and *temporal* (inter-frame variations) of the image sequences. To begin with, large computational and memory resources may be needed for real-time completion of even conceptually simple tasks. To overcome these problems new architectural solutions are advisable.

This paper presents a *bio-inspired* vision system for detection of collisions threats in automotive applications [10]. The rationale for adopting a bio-inspired architectural approach relies on the observation that the visual detection of motion is essential to survival in many animal species. Motion tells animals about predators and preys, about its own movements and that of others around it. Particularly, *Locusta Migratoria* (from now on *Locust*) [11] is exceptionally good at detecting and

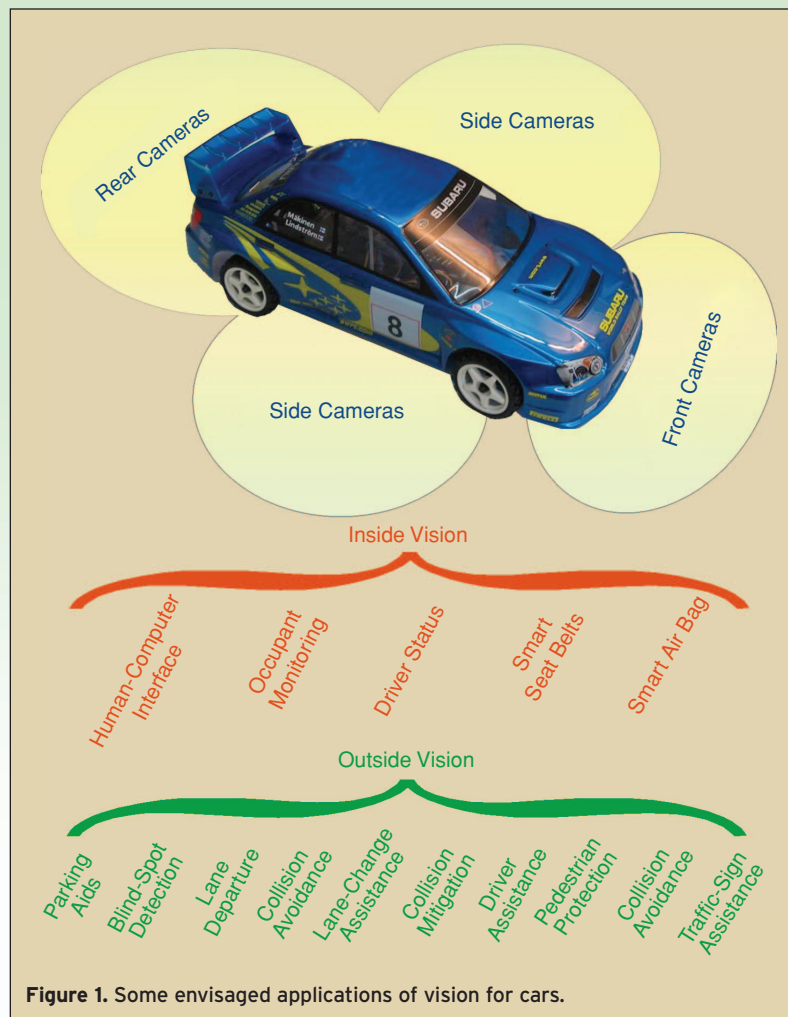


Figure 1. Some envisaged applications of vision for cars.

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reacting to the visual motion of an object approaching on a collision course. Indeed, some of the largest neurons in the Locust brain are dedicated to this task. We exploit the knowledge of the neural circuitry underlying this ability to construct artificial vision systems capable to deliver collision-warning alarms for cars.

Besides new paradigms, building efficient vision systems for automotive applications requires careful choice of the *hardware* architecture. Two basic possibilities arise:

- Using separate sensors and processors, relying either on CCD or on CMOS for the sensors [4].
- Building dedicated CMOS solutions which merge the sensing and the processing parts [9].

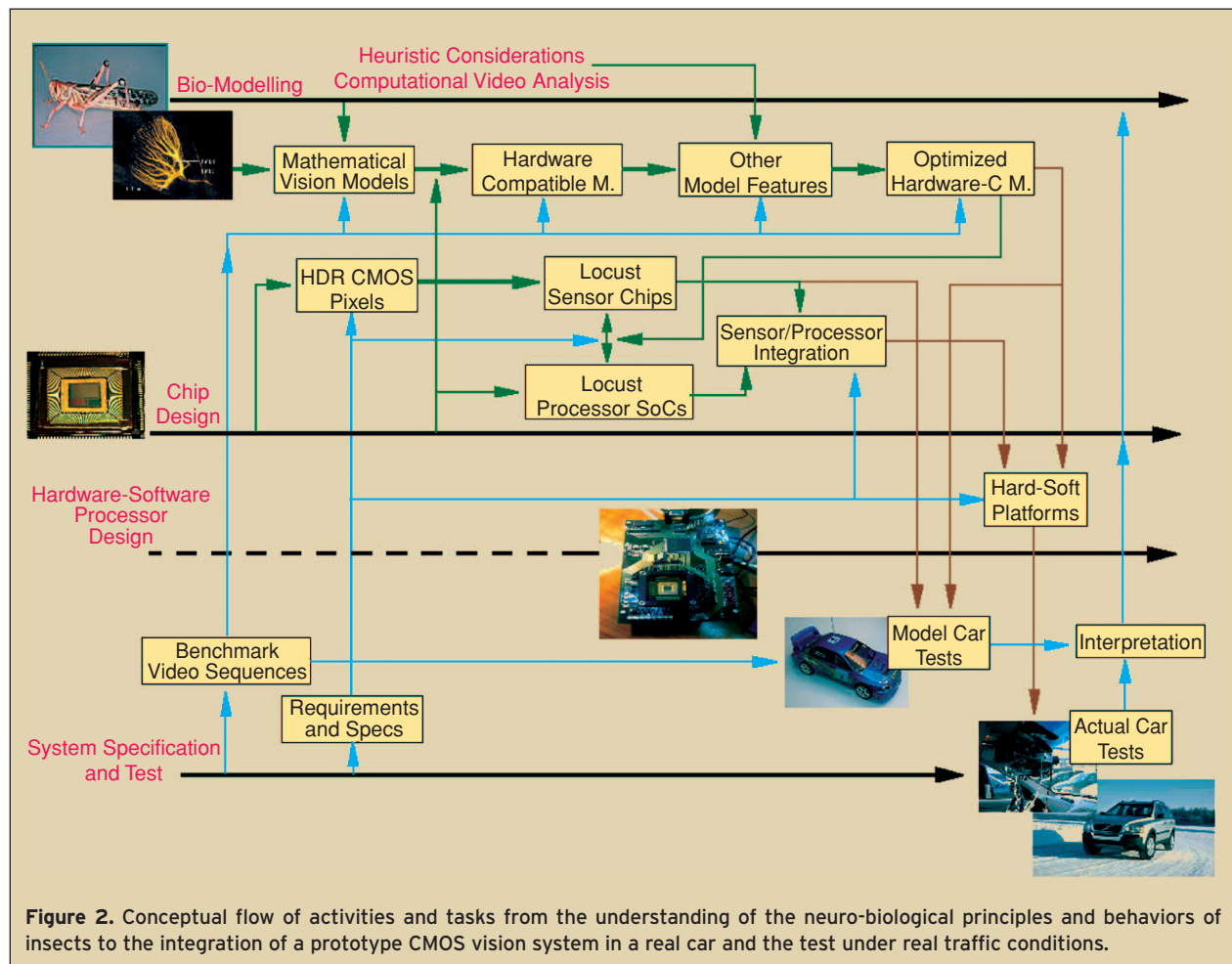
The main advantage of the second alternative is that dedicated *readout* circuitry, dedicated *error correction* circuitry and dedicated *processing* circuitry can be embedded *on-chip* together with the sensing circuitry. Such embedding can happen either pixel-by-pixel (*in-pixel* circuitry), or at chip level (off-pixel circuitry), or as a combination of both. Thus, for instance, *in-pixel* processing circuitry can be used to obtain high-speed through *parallel processing* in tasks where many data are involved such

as spatial filtering, image feature extraction, motion estimation, ... [12]. Then, off-pixel embedded digital processors can be used for control and high-level processing tasks involving a reduced data set [13].

Sensory-processing embedding is crucial for some customized processing architectures [14]. Furthermore, it can be used to speed up the computations needed to *adapt* the sensor response to changing conditions in the environment; i.e., to make the sensor section capable of acquiring images with *High Dynamic Range* (HDR). This latter feature is crucial since car vision sensors must be able to “see” under a very wide range of lighting and weather conditions.

Figure 2 shows a conceptual block diagram of the tasks involved in the development of a bio-inspired, custom CMOS vision system to be mounted at cars for collision-warning. The final goal encompasses the coordinated completion of *multi-disciplinary* activities of quite diverse nature, namely:

- To model the underlying biological behaviors by mathematical descriptions.
- To refine the bio-models upon a representation realizable through electronic circuits.



**Figure 2.** Conceptual flow of activities and tasks from the understanding of the neuro-biological principles and behaviors of insects to the integration of a prototype CMOS vision system in a real car and the test under real traffic conditions.

- To optimize the structure and parameters of such representation using benchmark real traffic sequences specified by car builders.
- To conceive and design dedicated CMOS chips capable of: 1) acquiring HDR images; 2) implementing the bio-inspired processing algorithm; 3) fulfilling the robustness and reliability requirements of automotive.
- To conceive and design hardware/software platform to: 1) host the dedicated chips; 2) interact with the car electronics through the available buses; 3) fulfilling automotive requirements.
- To integrate the hardware/software system into cars and to perform testing in benchmark collision scenarios.

As Figure 2 shows, the abilities and features of Locust must be supplemented with other features for proper operation. Also, practical considerations and experience dictate the convenience of using model cars as well as commercial cars for testing purposes.

## 2. The Underlying Biological Models

Natural vision systems have been improved through millennia of evolution and are more robust, compact and efficient than artificial counterparts. Many insects rely on vision for cruise control, navigation and collision avoidance [11], [15]–[21]. They are also able to perform these tasks within wide range of lighting condition. Why not to take advantage of the knowledge about these systems?

Figure 3 shows the concept of a system based on the “*Lobula Giant Movement Detector*” (LGMD) neural structure which is found in the visual system of the Locust [11], [21]. This structure fires an alarm if some collision threat is detected, thus giving rise to an evasive maneuver. An emulated-LGMD module is at the core of the system in Figure 3 and has been complemented for enlarged functionality with two other modules [22], namely:

- A Topological Feature Estimator (TpFE), whose purpose is to make an early classification of the approaching object that generates the alarm.
- An Attention Focusing Algorithm (AFA), aimed to optimize the use of the computing resources by restricting the processing to the zones of the frame that present more activity at a given instant.

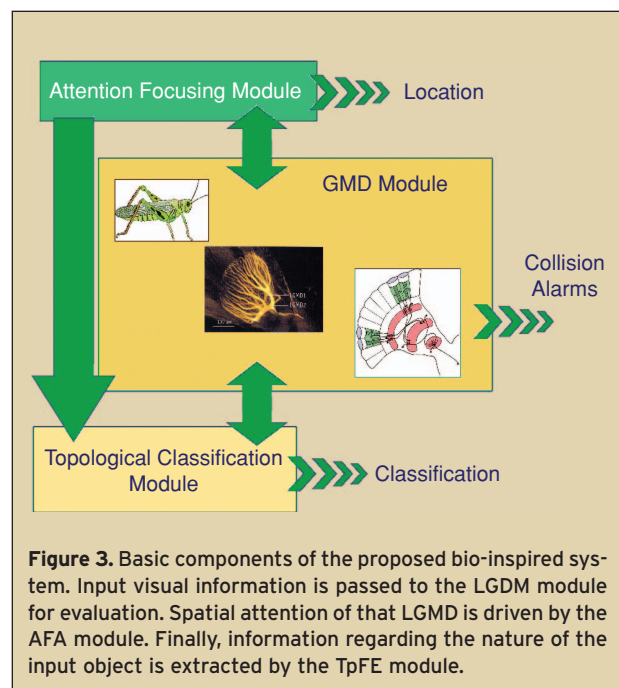
Deployment of warning signals in the presence of looming objects on a collision course is the basic role of the LGMD module. The TpFE and AFA modules are meant to provide further information about the environment and hence to: optimize the use of computer resources, to discriminate between real and spurious alarms, and to allow prompt appropriate evasive maneuvers.

Several works have addressed the use of insect visions for vehicles. Based on *Elementary Motion Detector* (EMD)

units, the work in [23] presents a bio-inspired analog VLSI chip that detects collisions up to 500msec before they occur. EMD units provide input to several directionally-sensitive neural structures which are found in insects like the flies. The idea is to design an array of EMD disposed in a radial way, from the centre of the array to the borders. This is the neural structure thought to be used in the landing mechanism of the fly. On the one hand, an approaching object would generate response in almost all the EMD’s, given that its edges would all move outwards in the radial sense. On the other hand, an object that approaches in non-collision course, or a translating object, would generate response in only a part of them. Simple steering and collision avoidance mechanisms based on fly EMDs have also been investigated in [24] using robot platforms. However system integration of these approaches into real cars is still in its earlier stages.

### A. LGMD Behaviour and Emulation

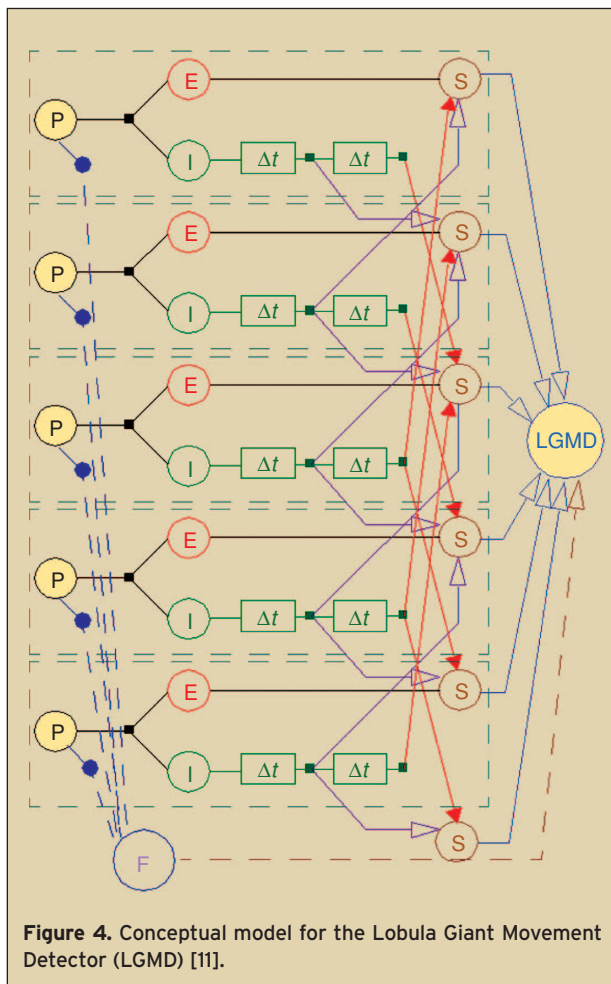
The LGMD neural structure, devised upon experimentation with Locusts [21], consists of 4 retino-topical layers of mutually interacting neurons, see Figure 4. Layer 1 represents the input to the neuronal circuit where P-units perform a high-pass temporal filter of the scene by subtracting the value of the luminance in a previous instant,  $\Delta t$ , from the current local value. Outputs from the P-units are simultaneously fed into an excitatory neuron E and an inhibitory neuron I. These two neurons constitute the second Layer. Layer 3 contains an excitatory neuron S, which collects excitatory inputs from E neurons within its retino-topic unit and inhibitory activity from I neurons



**Figure 3.** Basic components of the proposed bio-inspired system. Input visual information is passed to the LGMD module for evaluation. Spatial attention of that LGMD is driven by the AFA module. Finally, information regarding the nature of the input object is extracted by the TpFE module.

located within a finite neighborhood—called area of influence. Inhibitory activity spreads laterally with delays  $\Delta t$  and  $2\Delta t$  before entering the S units, thus providing a mechanism for spatio-temporal computation. Finally, excitatory activity of all S neurons converges into a single neuron, the already mentioned LGMD, in Layer 4, where it is accumulated. This biological model also suggests the existence of a global inhibition mechanism, F neuron, which is fired whenever the number of activated photoreceptors exceeds a given threshold within a time interval.

Mathematically, the behavior of each neuron can be defined by a spatio-temporal differential equation which rules the evolution of a *state variable*—called membrane potential in a biological language. Neuron activity and hence the information that is transmitted to other neurons in the structure occurs in different forms but always as a function of such state variable. In the original formulation, neurons belong to one of the following classes, namely: *Linear Threshold Cells (LT)*, or *Integrate and Fire Cells (IF)*. In both cases, the membrane potential  $v(t)$  is defined by a discrete time equation,



$$v_i(t+1) = P_i \cdot v_i(t) + g_i^{Exc} \cdot \sum_{j=1}^{N_{Exc}} w_{ij} \cdot a_j(t - \delta_{ij}) - g_i^{Inh} \cdot \sum_{k=1}^{N_{Inh}} w_{ik} \cdot a_k(t - \delta_{ik}) \quad (1)$$

where  $p_i$  is the persistence of the membrane potential,  $g_i^{Exc}$  and  $g_i^{Inh}$  are the gains of the excitatory and inhibitory channels respectively,  $w_{ik}$  is the strength of the synaptic connection from neuron  $k$  to neuron  $i$ , and  $\delta_{ik}$  is the delay associated to this connection.

Neuron activity  $a_i$  for Linear Threshold Cells is defined as:

$$a_i(t) = \begin{cases} v_i(t) & v_i(t) \geq \theta \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

Regarding Integrate and Fire neurons, the activity is the generation of a discrete-amplitude spike whenever the membrane potential exceeds the threshold.

$$a_i(t) = \begin{cases} \beta & v_i(t) \geq \theta \\ 0 & \text{otherwise} \end{cases} \quad (3)$$

Besides, when a spike is produced, the membrane potential is hyper-polarized such that  $v_i(t+1) \rightarrow v_i(t+1) - \alpha$ , being  $\alpha$  the amplitude of the hyper-polarization.

Table 1 shows the equations governing the original bio-model.

### B. Computational LGMD Model

The bio-model of Figure 4 captures correctly the reactions of the Locust to looming objects in collision course and is a starting point to build a car collision warning system. However, towards this end, its *structure* and its *parameters* must be modified to reach the following targets:

- Fit the frame rate to the distance resolution required by safety regulations. For instance, for 25 Fps the distance resolution will be 1 meter assuming 90 km/h speed.
- Make the model realizable by electronic circuits. Particularly, implementation becomes largely simplified if all model operations are realized through arithmetic operations between matrices.
- Select the model structure and parameters to guarantee robust operation within the range of illumination conditions, temperature and spreading of the underlying circuit parameters. Illumination range goes well from  $0.3 \text{ cd/m}^2$  to  $30000 \text{ cd/m}^2$ ; temperature range goes from  $40^\circ\text{C}$  to  $110^\circ\text{C}$ ; and for circuit parameters spreading typically  $6\sigma$  design [25].
- Guarantee correct model operation for a complete set of benchmark collision scenarios and traffic video sequences. These sequences were delivered by Volvo Car Corporation [26]. Figure 5 shows exemplary sample frames for some of them. The accuracy



**Figure 5.** Exemplary sample frames from selected test sequences. (a) Highway driving. (b) Roundabout. (c) Collision with test balloon car. (d) Pedestrian crossing in front of the car.

of the model response for each scenario/benchmark was qualified by expert human observers.

- Suppress spurious threats by the incorporation of features different from those observed in the biological beings.

The modification procedure follows a heuristic search where hypothesis are validated by simulations with detailed electrical macro-models. To build such models, non-ideal electronic effects such as memory leakage, mismatching, non-linearity in the operators, offsets, electronic noise, etc. must be analyzed and described by equations. The result of this heuristic

model tuning is the so-called *Simplified NoM (Noise Optimized Model)* shown in Figure 6. Main differences with the original model are:

- The model parameters and state variables are tuned such that everything can be satisfactorily executed with 6-bits equivalent accuracy. Moreover, input image was decided to be  $100 \times 150$  pixels.
- In the competition between inhibition and excitation, the inhibitory pathway contains information about the current spiking rate.
- The LGMD threshold is made adaptive instead of constant.

**Table 1.**  
Original model.

Cell	State equation and output equation.
P	$P_{ij}(t+1) = 0.4 \cdot P_{ij}(t) + L_{ij}(t) - L_{ij}(t-1)$ $P_{ij}^*(t+1); \text{ Integrate and Fire with } \beta = 1 \quad \alpha = 0.5 \quad \theta = 0.3$
E	$E_{ij}(t+1) = 0.1 \cdot E_{ij}(t) + 0.6 \cdot P_{ij}^*(t)$ $E_{ij}^*(t+1); \text{ Linear Threshold with } \theta = 0$
I	$I_{ij}(t+1) = 0.8 \cdot I_{ij}(t) + 0.2 \cdot P_{ij}^*(t)$ $I_{ij}^*(t+1); \text{ Linear Threshold with } \theta = 0$
S	$S_{ij}(t+1) = 0.4 \cdot S_{ij}(t) + E_{ij}^*(t+1) - 0.4 \left[ \sum_{Nr1} I_{kl}^*(t-1) + 0.8 \cdot \sum_{Nr2} I_{kl}^*(t-1) + 0.5 \cdot \sum_{Nr3} I_{kl}^*(t-2) \right]$ $S_{ij}^*(t+1); \text{ Integrate and Fire with } \beta = 1 \quad \alpha = 0.5 \quad \theta = 0.5$ <p>where:</p> <p><math>Nr_1</math> are the four nearest neighbors (top, bottom, right, left)</p> <p><math>Nr_2</math> are the four nearest neighbors in <math>45^\circ</math> (top-right, top-left, ...)</p> <p><math>Nr_3</math> are the four second-level nearest neighbors (top, bottom, right, left)</p>
F	$F(t+1) = 0.1 \cdot F(t) + 0.008 \cdot \sum_{i=1}^N \sum_{j=1}^M P_{ij}^*(t)$ $F^*(t+1); \text{ Linear Threshold with } \theta = 0.15$
LGMD	$y(t+1) = 0.4 \cdot y(t) - 5 \cdot F^*(t-1) + 0.08 \cdot \sum_{i=1}^N \sum_{j=1}^M S_{ij}^*(t)$ $y(t+1); \text{ Integrate and Fire with } \beta = 1 \quad \alpha = 0.25 \quad \theta = 0.5$

■ Threat scenarios are classified according to the firing rate of a neuron which receives information from the LGMD and the Threshold cell. Mathematically the model defines an ON-OFF cell which computes the local contrast  $C(i, j, t)$  as:

$$C(i, j, t) = |L(i, j, t) - L(i, j, t - 1)| \quad (4)$$

with luminance values in the range [0:63].

The inhibition is produced as a spatial low-pass filtered version of the contrast, then:

$$I(i, j, t) = K \otimes C(i, j, t) \quad (5)$$

where  $K$  is a typical  $3 \times 3$  low-pass kernel and  $\otimes$  denotes convolution.

Excitation from the ON-OFF cells  $C(i, j, t)$ , and inhibition  $I(i, j, t)$  are combined into the Summing Units to produce a net excitation  $S(i, j, t)$ :

$$S(i, j, t) = \max\{C(i, j, t) - w(t) \cdot I(i, j, t - 1), 0\} \quad (6)$$

where  $w(t)$  are empirical, firing rate dependent, weights which are defined below.

The net excitation enters the LGMD neuron to generate a membrane potential  $e(t)$ :

$$e(t) = \sum_{i=1}^{100} \sum_{j=1}^{150} \frac{S(i, j, t)}{150} \quad (7)$$

whereas the LGMD output  $E(t)$  is computed as:

$$E(t) = \vec{u} \circ [e(t), E(t - 1), E(t - 2)]^t \quad (8)$$

where  $\circ$  denotes the dot product, and  $\vec{u} = (1/24) \cdot [20, 3, 1]$ , which was found by using genetic algorithms and different test videos provided by Volvo Car Corporation. By definition  $E(t)$  is zero for the first 15 frames ( $t = 1, 2, \dots, 15$ ).

The threshold computation involves a second LGMD variable  $v(t)$  which results from:

$$v(t) = \vec{u} \circ [e(t), v(t - 1), v(t - 2)]^t \quad (9)$$

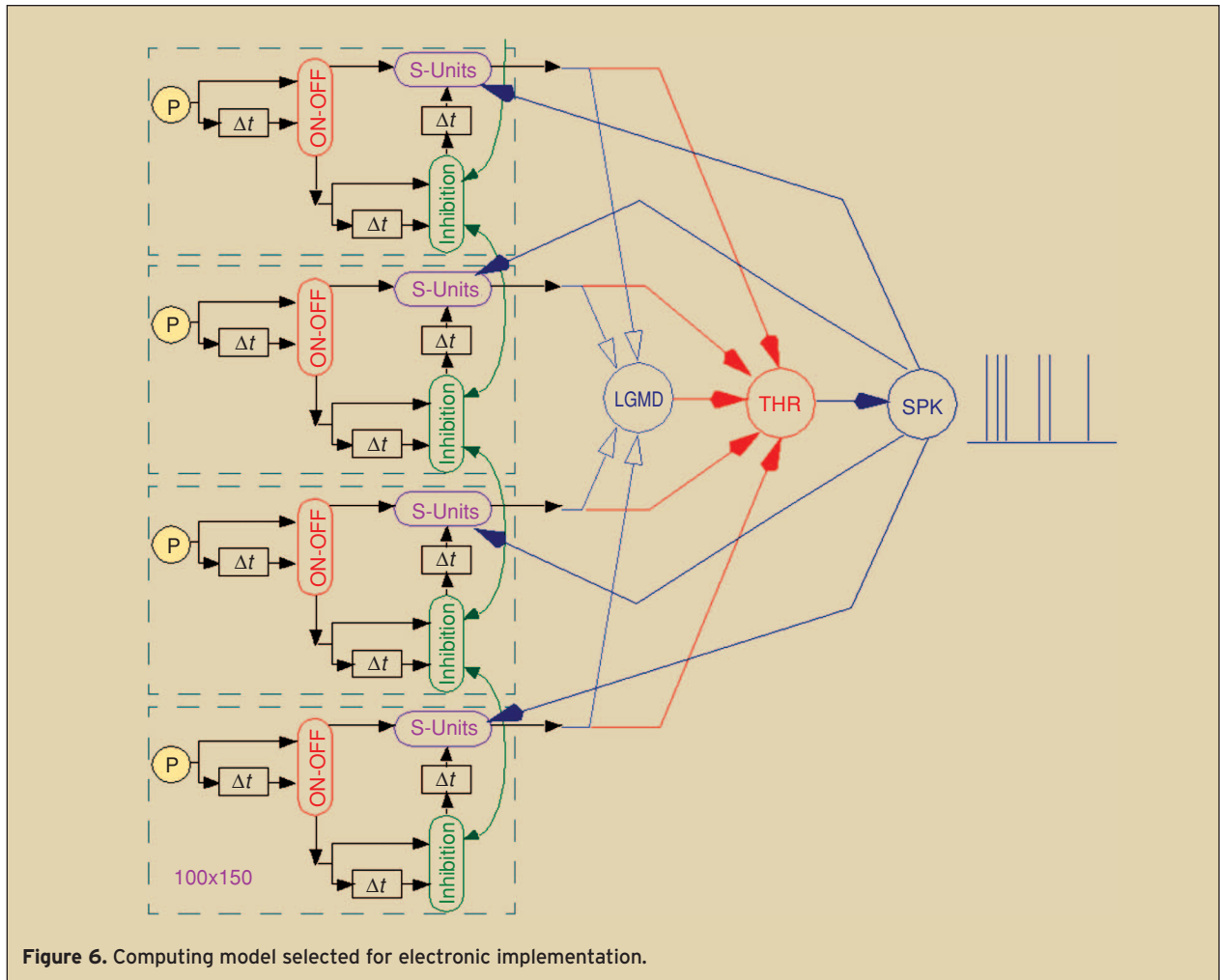


Figure 6. Computing model selected for electronic implementation.

which is also zero for frames 1 to 15, and that is employed to calculate a raw threshold  $V(t)$  as:

$$V(t) = \vec{V} \circ [v(t-5), v(t-10), v(t-14)]^t \quad (10)$$

where the parameters in  $\vec{V}$  are  $\vec{V} = (1/7) \cdot [1, 3, 3]$ , and were found in the same genetic algorithm used for  $\vec{u}$ .

Finally, the threshold cell output is the *effective threshold*  $W(t)$  which is computed as:

$$W(t) = \max\{V(t), 50\} + 15 \quad (11)$$

Threshold and LGDM output values are passed to the firing neuron (SPK in Figure 6) which fires an spike in frame  $t_j$  if

$$E(t_j) \geq W(t_j) \quad (12)$$

Besides, if a spike has been produced, the LGMD suffers a hyper-polarization which makes  $[E(t_j - 1), E(t_j - 2), E(t_j - 3)] = 0$ . Observe that while the LGMD states are reset after firing spikes, the threshold cell, which is governed by a similar state equation, does not. Note also that in cases where activity variation is low, LGMD and threshold cell outputs tend to the same value and therefore no spikes will be produced.

Finally, the model incorporates an accumulator which contains the number of spikes produced in the last five frames. The state of this accumulator,  $n(t)$ , is used to define the response of the model (*State*) and to modify the strength of the inhibitory pathway  $w(t)$  in (6) as indicated in Table 2.

### C. Attention Focusing Algorithm (AFE)

Heuristics search shows that, typically, all relevant information is contained within reduced regions of the last model layers. This happens for instance when an object is approaching and the excitation is not generated by a turning movement or camera vibration—see Figure 7. In these situations focusing on the region of interest reduces the amount of information to be processed and improves the model efficiency.

Inputs to the AFE module are taken from the S-layer because there the background and other non significant pieces of information have been already removed. The AFE divides the input frame by defining an *attention grid* formed by groups of cells, some of which are enabled and other disabled. Each group defines an *attention-cell*. Cells within an enabled attention-cell are active and con-

tribute to the model computation. On the contrary, cells within a disabled attention-cell remain silent and their outputs do not contribute to the LGMD potential.

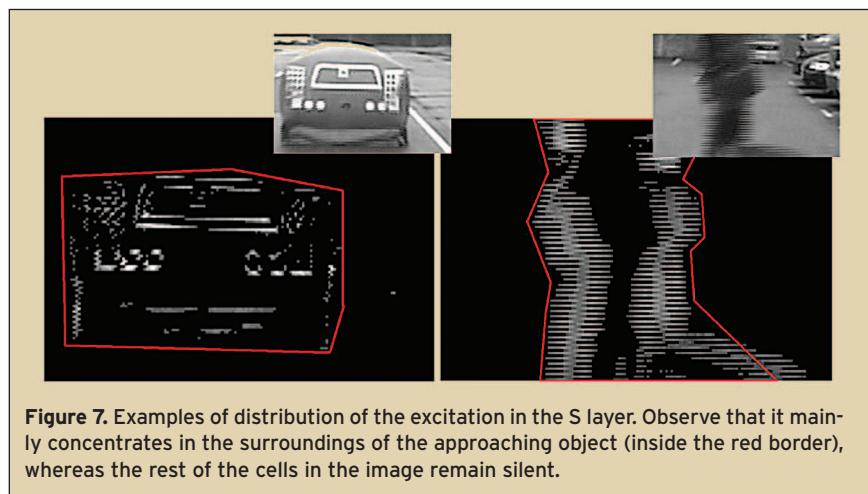
At the beginning, the attention grid is, by default, a chess board pattern and the following modules are used to control the activation of attention cells:

- *Attention*: this module decides which attention cells exhibit enough activity to activate their neighbors (activating cell). It also disables the ones in which there was not enough activity in the previous frame, transferring their activation to the nearest disabled attention cell that belongs to the default activation grid.
- *Activate*: this module is called by the Attention one, and activates the attention cells that surround the current activating cell. It returns the number of cells it has actually activated, since it depends on the location of the central cell, and the previous state of activation of its surrounding attention cells.
- *Disable*: this module is also called by the Attention one, and its duty is to switch off the same number of attention cells that Activate has activated. The goal is to maintain constant the amount of information to be extracted from the array of the S-cells. The rule is to switch off the attention cells that are furthest to the current activating cell.

Experience reveals that the best default attention grids are the ones that uniformly distribute the attention over the frame when there is no particular source of excitation.

**Table 2.**  
 $w(t)$  and model output as a function of the spiking rate.

$n(t)$	1	2	3	4	5
$w(t)$	0.75	1.0	1.25	1.5	1.5
State	No danger		Attention	Danger	Extreme Danger



**Figure 7.** Examples of distribution of the excitation in the S layer. Observe that it mainly concentrates in the surroundings of the approaching object (inside the red border), whereas the rest of the cells in the image remain silent.



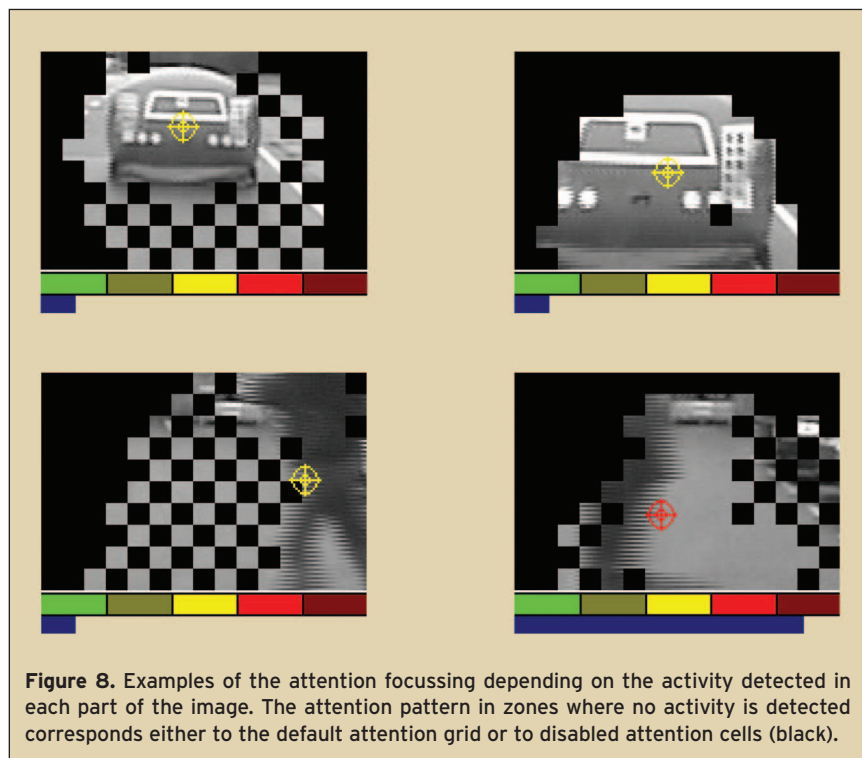
Examples of the concentration of the attention can be observed in Figure 8. The circle pointer indicates the centre of mass of the excitation in the S-layer. Green color means neither danger nor activity; yellow means activity but no danger; and red activity an alarm.

#### D. Topological Feature Estimator (TpFE)

The way how the LGMD potential is calculated involves losing information about the shape of the object originating the alarm. However, this information is pertinent in many cases. For instance, a sharp turning of the car makes the background to move rapidly, spreads the activity out across the entire S-layer and may produce false alarms. Similar situations happen when the car is approaching a horizontal road line, if a bulge of the road shakes the camera, etc. The TpFE module overcomes these problems by making an early classification of the approaching objects. In addition to making the system more accurate, such classification helps when taking countermeasures with better fitting in the type of the approaching object (whether it is a pedestrian, a car, etc.).

Using the information contained in the S-layer, shapes are classified into four different classes corresponding respectively to:

- vertical-shaped object such as traffic lights, persons ... —vertical-shaped class
- road line or road stripe—horizontal-shaped class
- turning movements—spatially global class
- an approaching car—squared-shaped class.



**Figure 8.** Examples of the attention focussing depending on the activity detected in each part of the image. The attention pattern in zones where no activity is detected corresponds either to the default attention grid or to disabled attention cells (black).

Classification requires, first, calculating a *vertical* vector (obtained by adding up column entries, row-by-row) and a *horizontal* vector (obtained by adding up row entries, column-by-column), respectively. Usually, the first entries of the vertical vector are discarded to filter out the spurious activity caused by the movement of the horizon. Then two statistical descriptors  $\delta_V(t)$  and  $\delta_H(t)$  are built using the mean value  $\mu$  and the variance  $\sigma$  of these vectors, namely:

$$\begin{aligned}\delta_V(t) &= \mu_V(t) - \sigma_V(t) \\ \delta_H(t) &= \mu_H(t) - \sigma_H(t)\end{aligned}\quad (13)$$

The dominant components of the shape are evaluated by comparing the values of these descriptors with a priori defined values for each of the classes being considered. Figure 9 shows examples of object classification by the TpFE module.

#### 3. From the Locust to the Car: LOCUST CMOS Chips

The correct operation of the collision-warning system when mounted on real cars requires proper image acquisition at the photosensor layer. This is challenging due to:

- The necessity to handle wide illumination ranges.
- The stringent automotive requirements regarding temperature range, vibrations, EMI, ...
- The necessity to guarantee correct operation under wide tolerance margins of the underlying technological parameters.

While the last two challenges apply to both the sensor and the processor, the first is specific for the front-end [29].

Different approaches for High Dynamic Range (HDR) image sensors have been reported such as *logarithmic compression, dual and multiple sampling, programmable gain, intelligent control of exposure, ...*, etc. Some of the most relevant early ideas are found in [30]–[37]. Overviews are presented in [38] and then in [39], [40]. Practical circuit implementations can be found at *IEEE Solid-State Circuits* archive. One may rely on available HDR sensors and combine them with standard digital processors to implement the collision warning models.

Alternatively, the design of the front-end sensory part and that of the processing part can be affronted as linked components of a single *sensory-processing*

design problem. Still different architectural solutions apply, namely:

- Using a fully retino-topic architecture where a significant part of the processing is completed in fully parallel manner through dedicated in-pixel analog and mixed-signal circuitry
- Keeping only a few mixed-signal functions in-pixel and shifting all the remaining to be handled by dedicated digital processors.

To untie the gordian knot of this architectural choice the following question should be answered: where to place the border between the parallel mixed-signal circuitry and the serial digital processing circuitry? This question arises when one confronts the design of any on-chip sensory-processing system [13]. Its answer involves issues regarding the application (for instance whether complete images or only image features must be downloaded from the sensor); considerations on the computing paradigm to adopt [14]; and issues regarding feasibility of the available technologies and circuit primitives [41].

In the case of automotive applications the decision about where to place the border between the analog and the digital domain is largely conditioned by data storage issues. Particularly by those related to short-term storage of intermediate data. Analog storage provides compact solutions for neural and bio-inspired VLSI systems [42] and has been demonstrated through both academic [12], [43], [44] and industrial [13] CMOS VLSI chips. However, in automotive applications leakage currents and reliability considerations pose difficult challenges to the practical usage of analog storage. They can be addressed by using a refreshing scheme consisting of AD and DA converters in a loop [42], but this increases the pixel size and severely penalizes the pixel count and hence the spatial resolution of the sensor.

#### A. HDR CMOS Pixel

Figure 10 shows a concept of a HDR pixel which combines the principles of *companding* pixels with those of pixels based on the control of the *integration time*. Companding in this pixel is not determined by inaccurate device features as it happens with logarithmic compression based on the I-V characteristics of MOS transistors in weak inversion. Instead, companding is controlled by timing. The principle is similar to that of integration pixels. The photogenerated current is integrated in a capacitor producing a decay of the voltage. Assuming that both the photogenerated current and the pixel capacitance remain constant during the operation, the decay happens to be linear and determined by the result of the multiplication of this current and the integration time,

$$V_{ph}(t) = V_{RST} - \frac{I_{ph}}{C_{pix}} \cdot t \quad (14)$$

In integration pixels this voltage defines the pixel output. In the pixel of Figure 10 this voltage signal is employed to set the time interval during which a reference signal is first tracked and finally sampled. This latter signal is either stored on a capacitor, Figure 10(a), or on a digital register, Figure 10(b).

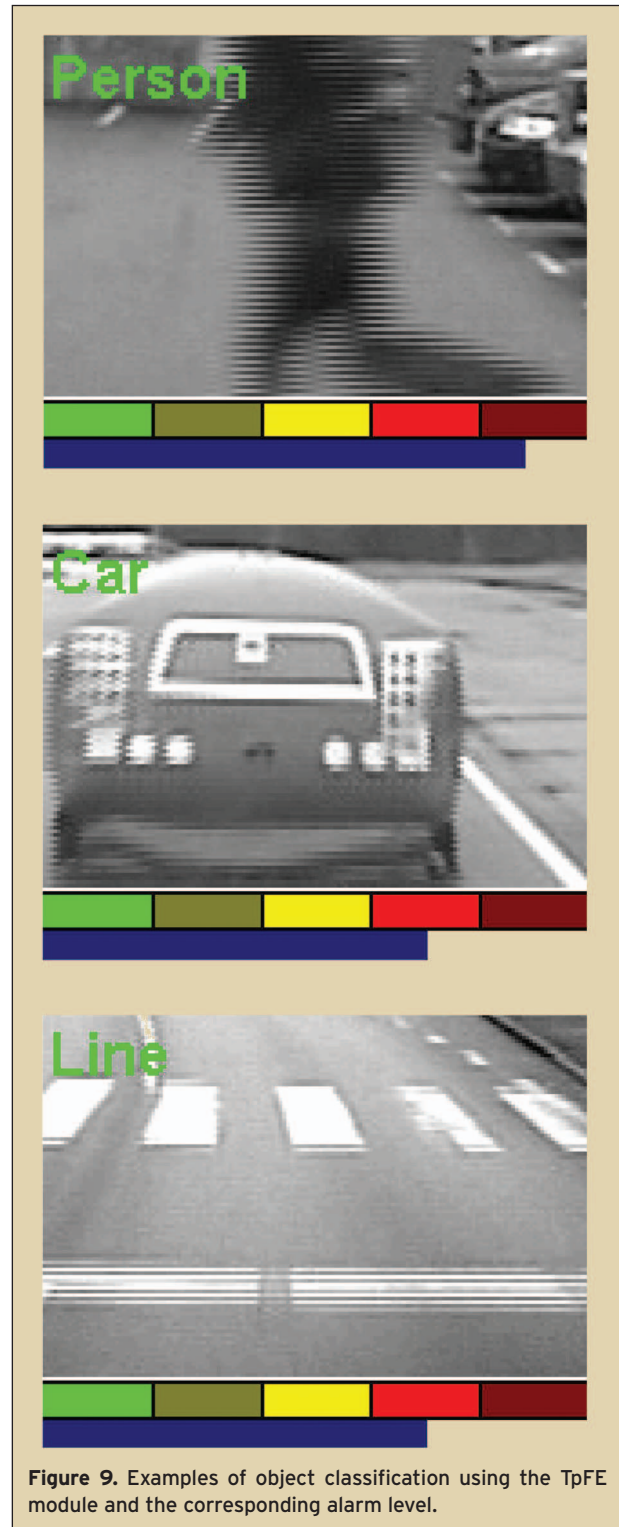


Figure 9. Examples of object classification using the TpFE module and the corresponding alarm level.

The mixed-signal choice of Figure 10(b) has the main advantages of precluding the analog memorization errors and the Fixed Pattern Noise artifact (FPN [39]) caused by the mismatch of the analog buffer which delivers  $V_{pix}$  across the photosensor array. In this pixel, an analog signal  $V_{REF}(t)$  is compared with the photo-generated voltage  $V_{ph}(t)$ , and a  $N$ -bit digital signal  $V_{IO}[N-1:0]$  is continuously sampled by the  $N$ -bit register on the pixel. While  $V_{ph}(t) \leq V_{REF}(t)$ , the comparator disables the write-enable signal in the memory and the pixel output tracks the time evolution of the digital signal. When  $V_{ph}(t) = V_{REF}(t)$  the current value of the digital signal is stored as the pixel output.

In the case of linearly increasing reference signals (as shown in Figure 10(c)), the I-V compression curve is given by:

$$V_{pix}(I_{ph}) = \frac{V_{RST}}{1 + \frac{I_{ph}}{I_{Sat}}} \quad (15)$$

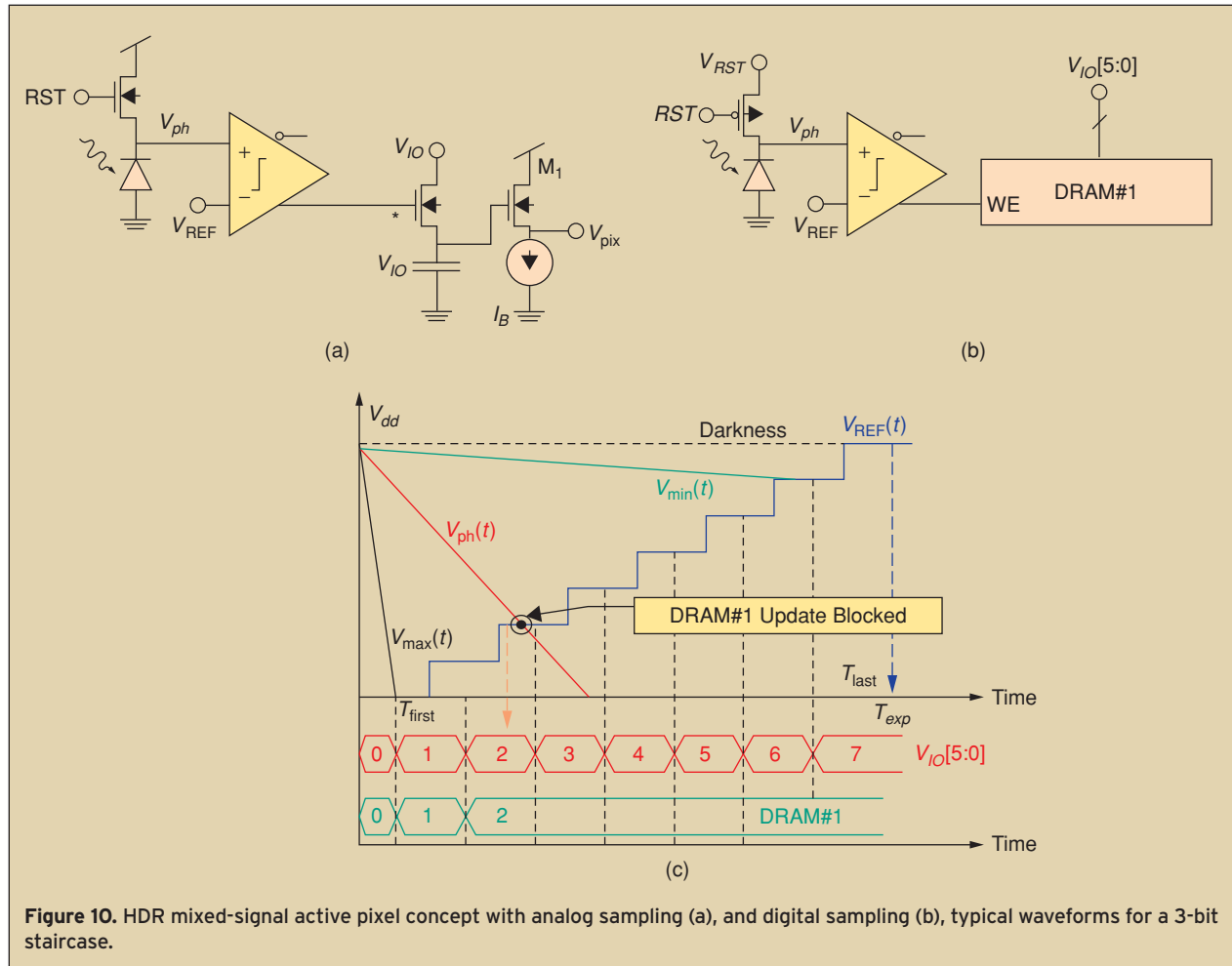
Which is obtained by assuming that  $V_{REF}(t) = V_{RST} \cdot t/T_{EXP}$ , and where  $I_{Sat}$  denotes the value of the photogenerated current which produces a voltage drop

$V_{RST}$  within a time interval  $T_{EXP}$ , or, in other words, the photogenerated current which produces the saturation of the pixel in integration mode for this exposure.

This companding approach enhances the dynamic range by precluding brightest pixels to saturate. Conventional integration pixels exhibit a dynamic range given by

$$DR_{LIN} = 20 \text{Log} \left( \frac{FS}{V_N} \right) \quad (16)$$

where  $FS = V_{RST} - V_N$  is the maximum attainable (detectable) voltage drop across the integration capacitance, and  $V_N$  is the minimum voltage drop that can be detected (usually this is referred to the noise value, since it is assumed that a signal is detectable if its SNR is one). This is also the value of the dynamic range at the integration capacitor of the HDR pixel. However, the dynamic range of the photogenerated current is larger due to the action of companding. Maximum photogenerated current produces a voltage drop  $V_{RST} - V_N$  in a short time, whereas the minimum photogenerated current produces a voltage drop  $V_N$  in a time interval  $T_{EXP}$ . After some calculations one obtains:



**Figure 10.** HDR mixed-signal active pixel concept with analog sampling (a), and digital sampling (b), typical waveforms for a 3-bit staircase.

$$DR_{HDR} = 20\text{Log} \left( \frac{\max(I_{ph})}{\min(I_{ph})} \right) \cong 40\text{Log} \left( \frac{FS}{V_N} \right) \quad (17)$$

It is seen that the DR of the photocurrent is two-orders-of-magnitude larger than that of the integrated voltage.

Seeking for simpler design, the reference signal is replaced by a digitally-generated staircase followed by a Digital to Analog Converter (DAC). If the converter satisfies  $V_{LSB} > V_N$ , and it is properly programmed to cover the maximum attainable voltage drop at the photodiode capacitance, then the dynamic range results:

$$DR_{HDR} = 20\text{Log} \left[ \frac{1 - 2^{-(N+1)}}{2^{-(2N+1)}} \left( 1 - 2^{-N} - 2^{-(N+1)} \right) \right] \quad (18)$$

The global operation is illustrated by the transfer curve of Figure 11(a), where the code  $2^N - 1$  corresponds to a

photogenerated current of 18pA. The figure also shows the curve corresponding to linear integration. It is seen that the HDR pixel produces non-saturated outputs at higher luminances. Besides, different transfer curves can be obtained by properly programming the reference signal  $V_{REF}(t)$  and  $V_{IO}[N-1:0]$  as it is illustrated by the 3-D family of measured curves shown at the figure inset. Hence a feedback signal can be applied to adapt the pixel response to the global (inter-frame) illumination conditions. Under the assumption that  $V_{LSB} > V_N$ , equation (18) shows that the DR can be controlled as a function of the number of bits in the DAC. It provides some degree of freedom to cover different specifications, but has counterparts. Particularly it has a direct impact on the number of memories on the pixel which are devoted to  $V_{IO}[N-1:0]$  storage, and hence on the spatial resolution of the sensor.

Figure 11(b) illustrates the operation of a CMOS imager prototype with a 6-bit DAC ( $DR_{HDR} = 78$  dB

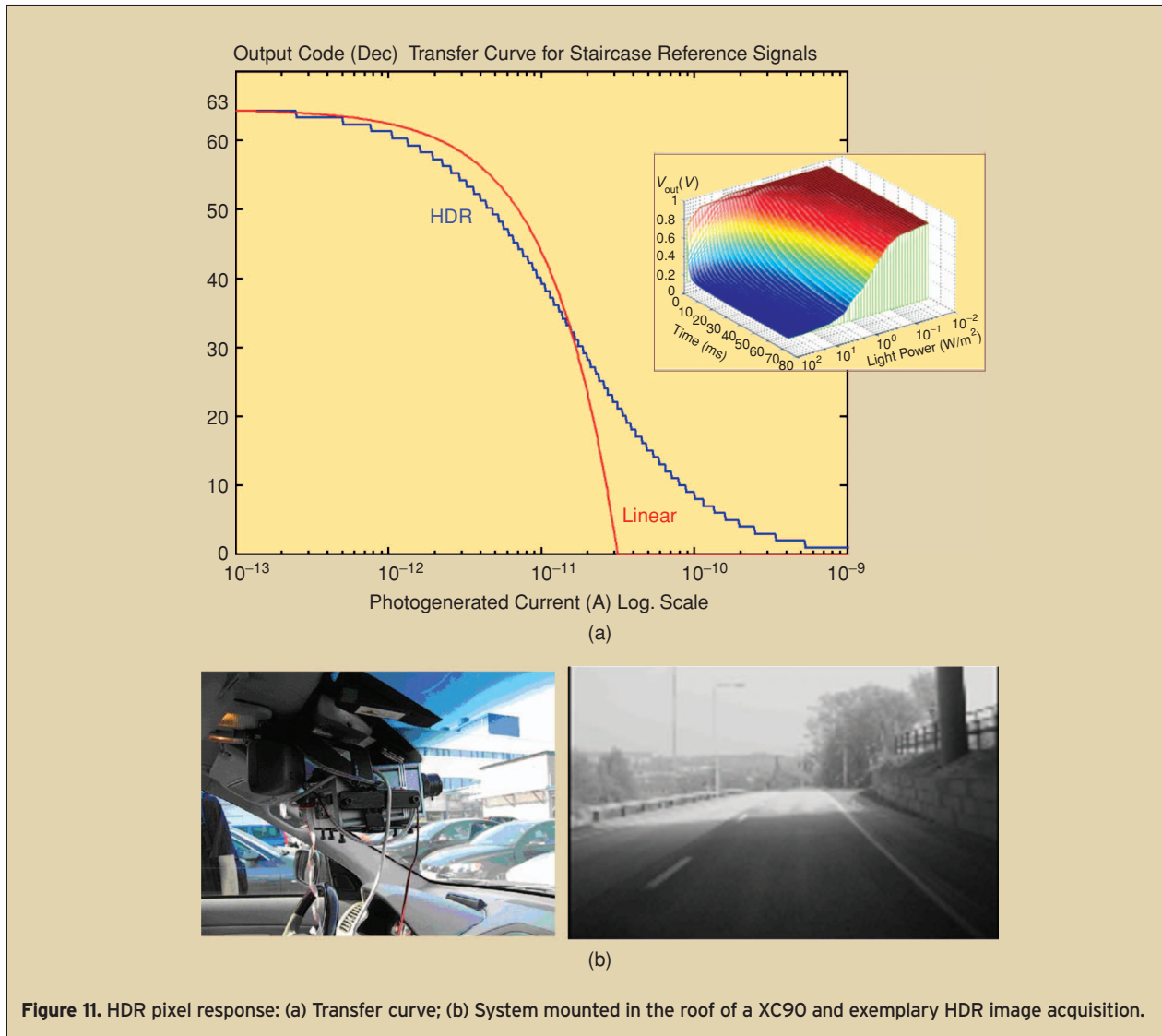


Figure 11. HDR pixel response: (a) Transfer curve; (b) System mounted in the roof of a XC90 and exemplary HDR image acquisition.

and). This picture shows an exemplary HDR image captured when the car is exiting a tunnel. Note that both the darker and brighter parts of the scene are captured with good level of details.

### B. Semi-Retinotopic Sensor Architecture

The pixel architecture of Figure 12(a) takes into account considerations regarding data storage reliability and the computational demands of the collision warning algorithm. Besides the photodiode and the comparator needed for HDR acquisition, the pixel contains three DRAM blocks, a DRAM refresh buffer, and a bidirectional I/O

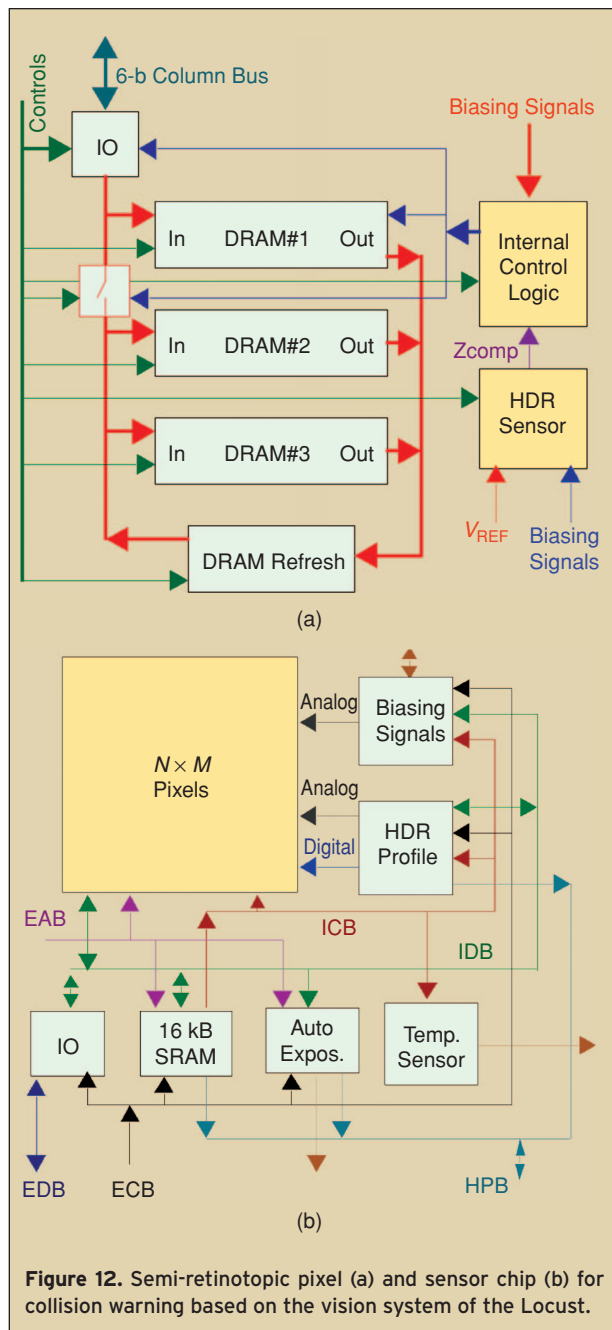


Figure 12. Semi-retinotopic pixel (a) and sensor chip (b) for collision warning based on the vision system of the Locust.

buffer which transmits VIO to the pixel during optical sensing and outputs the pixel values during readouts. DRAM#1 block is employed as VIO memory during optical acquisition. Thus, at the end of a given image capturing process, the contents in the three pixel memories correspond to three consecutive frames. This information is downloaded into the digital processor described in the next section which executes the collision alarm algorithm. Afterwards, the chip moves DRAM#2 to DRAM#3, and DRAM#1 to DRAM#2, leaving DRAM#1 available for the next optical acquisition.

Figure 12(b) shows the architecture of the complete sensor which, besides the sensor array, contains the following blocks:

- A 16 kBytes SRAM block which is used by the processor in calculations
- An input/output digital buffer which stores 150 pixels (a whole row) and allows data transfer rates at high-speed (128 Mbytes/s)
- A HDR profile block which stores, in digital format, the waveforms to be applied at VIO[5:0] during optical acquisition, and the digital codes to be provided to the Digital-to-Analog converter which generates  $V_{REF}(t)$
- A biasing generator, which creates the required analog signals for the chip
- A PTAP temperature sensor which is used to adapt the DRAM refreshing period, and
- An auto-exposure block. This auto-exposure block allows the definition of a region of interest and a target value for the average value for the pixels within that region. It computes the mean value of the pixels in the defined region of interest during image downloading and generates a feedback signal to adapt the sensor response to the global illumination conditions.

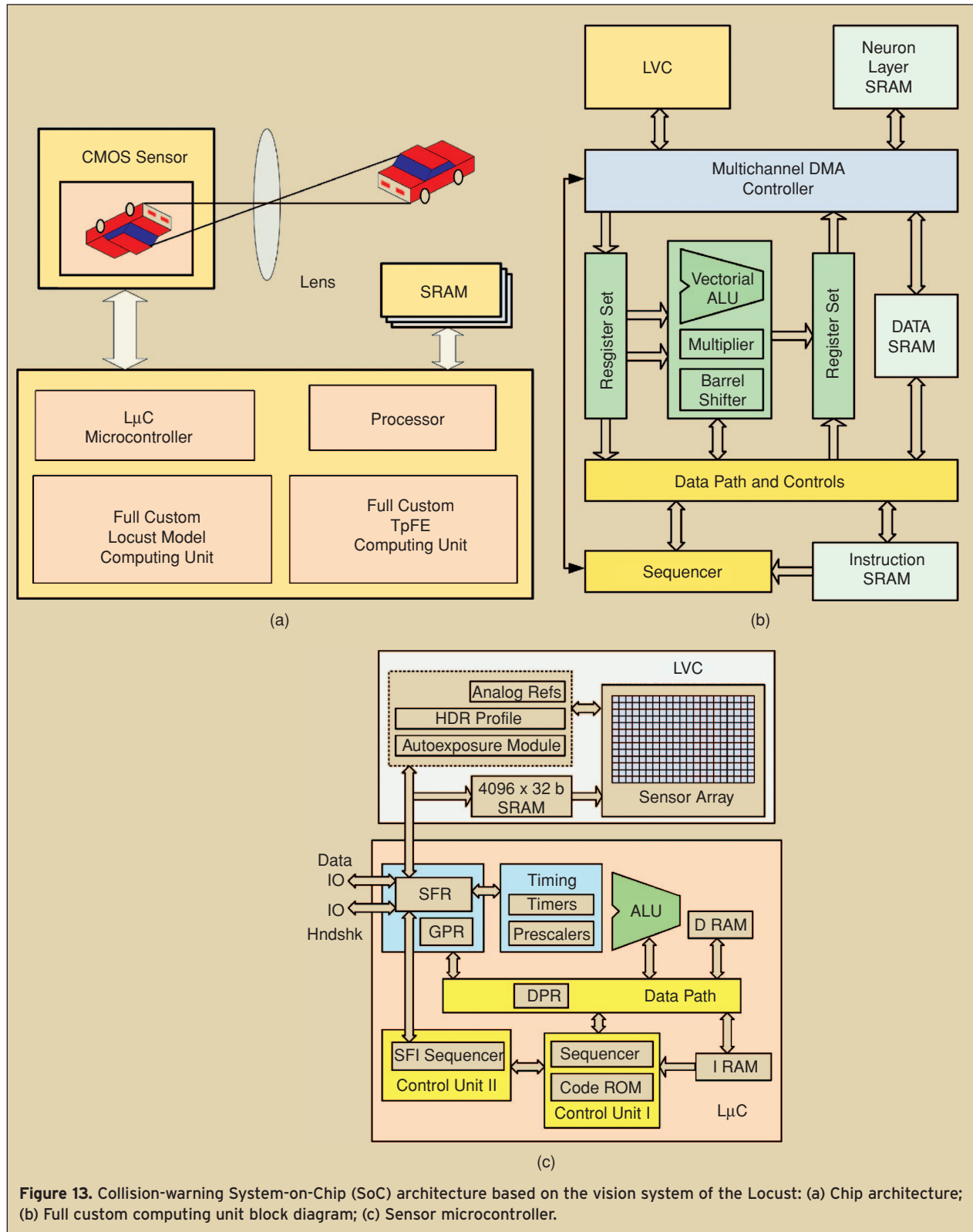
### C. Dedicated Digital Processor

Figure 13(a) shows the architecture of a *System-on-Chip* consisting of the semi-retinotopic sensor and a dedicated digital processor. This latter processor embeds four cores dedicated respectively to: a) control the sensor (L $\mu$ C micro-controller); b) perform the arithmetic operations and memory access tasks involved in the emulation of the LGMD model (Full Custom Locust Model Computing Unit); c) perform the corresponding operations for the Topological Feature Extractor (Full Custom TpFE Computing Unit); d) control and coordinate the overall operation. The first one is a full custom RISC micro-controller; the second and the third are identical full-custom arithmetic processing cores; and the fourth is a general purpose processor.

The first three cores above operate in parallel, synchronously, in order to guarantee real-time operation

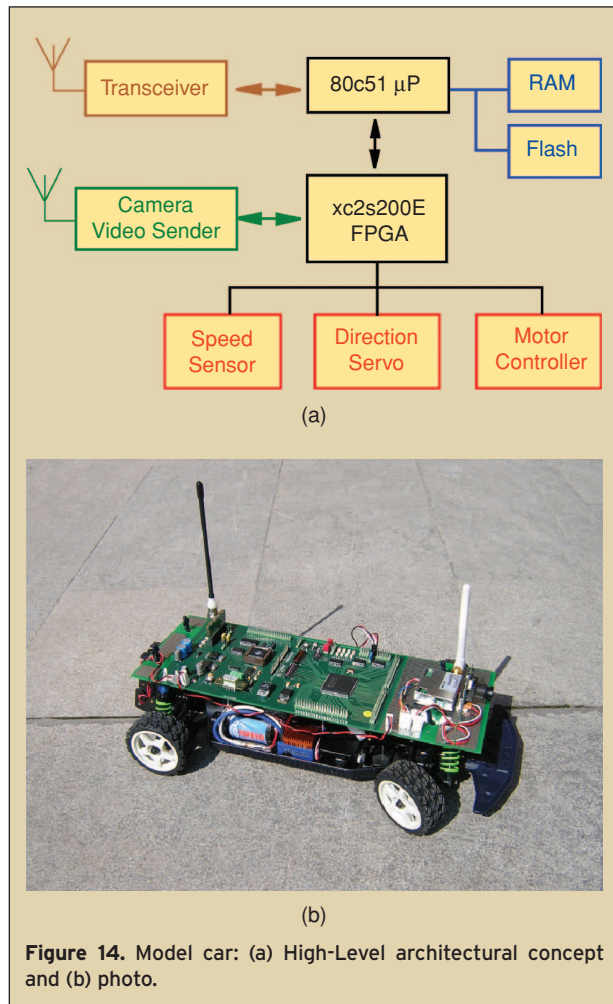
with a fixed frame rate. As compared to a single core choice, the multi-core solution yields reduced hardware complexity. Hence, its corresponding hardware design cycles are shorter. Besides, the multi-core architecture is

easier to re-program when fine tuning is required to fit the model response to real-time automotive scenarios. Conversely, the single-core processor is prone to exhibit non-deterministic behaviors that impact on the frame



**Figure 13.** Collision-warning System-on-Chip (SoC) architecture based on the vision system of the Locust: (a) Chip architecture; (b) Full custom computing unit block diagram; (c) Sensor microcontroller.

rate. As the matter of fact, successful automotive vision processors use multi-core solutions for computationally intensive applications, real-time visual recognition and scene interpretation [45]–[47].



**Figure 14.** Model car: (a) High-Level architectural concept and (b) photo.



**Figure 15.** Installation of the collision-warning system in the rear mirror area of the XC90.

The core labelled  $L\mu C$  micro-controller in Figure 13(a) is devoted to low-level control functions, while the so-called full custom computing units are devoted to intensive arithmetic calculus. The corresponding tasks are enumerated below:

- Low-level control of the HDR sensor. These tasks comprise the downloading of images and the control of the surrounding circuitry of the sensor array: control of the HDR profile block, the internal analog references, the auto-exposure block and the internal DRAM memories refresh and moving data processes.
- Emulation of the LGMD model. These tasks include memory transfers, matrix calculus and convolutions related with the LGMD neural structure model: the ON-OFF cells movement map, the inhibition layer low pass filter and the S-units layer calculations.
- Topological Feature Estimator algorithm. These tasks include matrix calculus, means, variances and arithmetic operations related with the geometrical descriptors of the objects that are in the field of view.

The digital processors and the HDR CMOS image sensor are arranged into three levels of control hierarchy: the general-purpose processor at the top-level; the arithmetic computing units together with the RISC micro-controller at the second; and the HDR CMOS image sensor at the third. This multi-core design is flexible and powerful enough to accept changes and improvements of the routines and models without affecting the real-time performance of the collision-warning.

The control-commanding requirements of the HDR sensor include asynchronous and real-time low-level tasks. The custom micro-controller included in the system, called  $L\mu C$ , frees the general purpose processor from these tasks, increasing the overall system efficiency. This controller receives high level commands from the host processor and translates them into a series of function sequences to control the HDR sensor circuitry.

The  $L\mu C$  is a RISC computer with fixed encoding register-register Harvard architecture whose programming is realized in assembler. Its architecture (see Figure 13(c)) comprises General Purpose Registers (GPR), Special Function Registers (SFR), an ALU, a bidirectional shifter, timers and two control units with sequencers. The device accepts up to 5 interrupts sources.

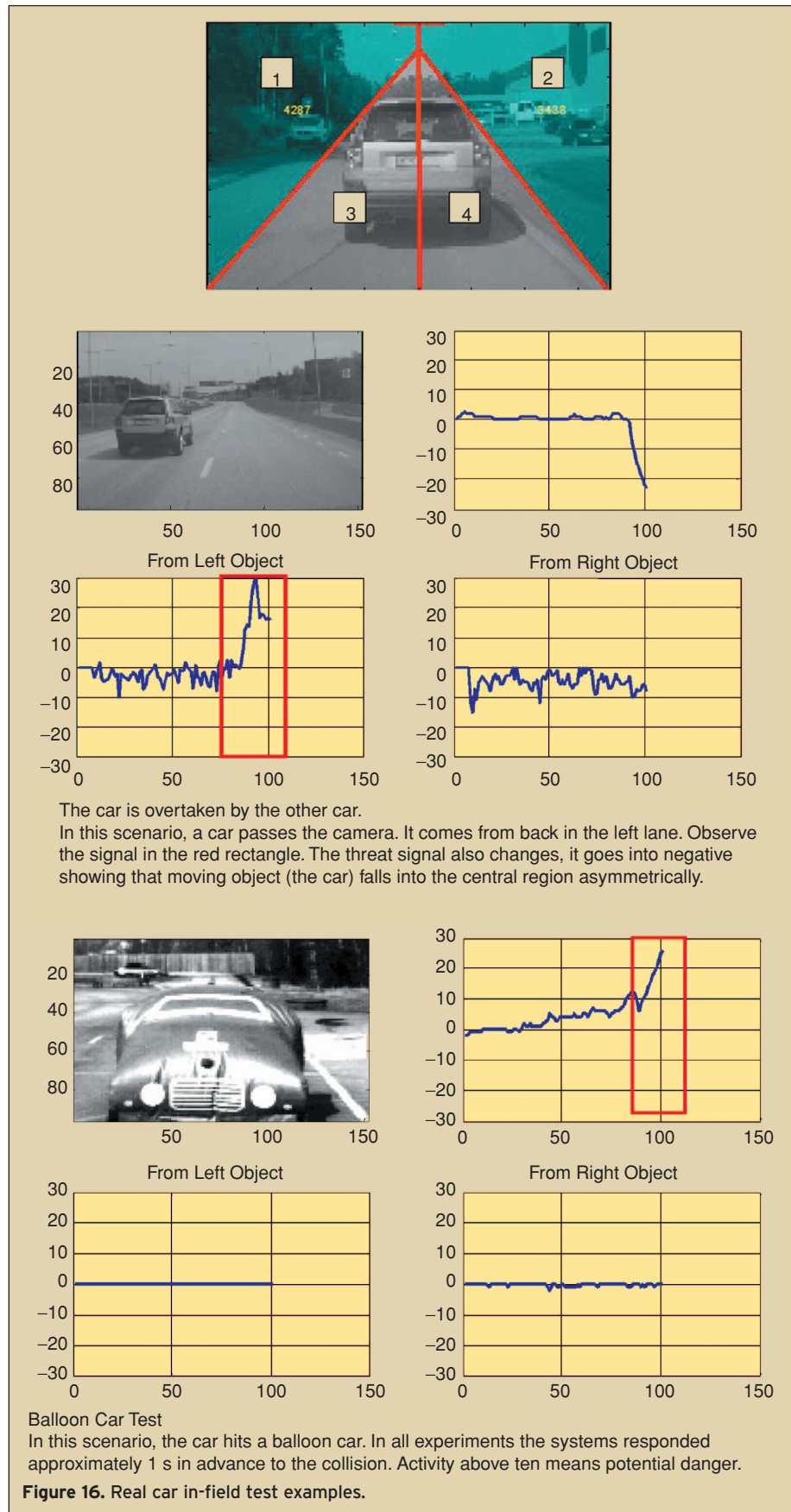
The  $L\mu C$  architecture is designed to receive new high level commands from the host CPU and to send data, coming from the micro-controller control routines, even if the  $L\mu C$  is busy. Its data path includes special features to speed-up the interchange of information between registers and between registers and memory. The controller's

instruction-set has a subset of instructions designed to accelerate image uploading and downloading processes while saving CPU load.

The full custom arithmetic computing units are conceived to deal with memory transfers and matrix calculus related with neurons models and statistical descriptors. Besides coordinating the operation of the whole system, the general purpose processor deals with low processing demanding scalar calculations of the LGMD model and the object classification.

Both units, Figure 13(b), include a vectorial computing core, with functionality resembling that of standard DSP execution units. It contains a vectorial ALU, a multiplier and a barrel shifter, plus two sets of registers for temporal data storage and a programmable sequencer. In addition, a multi-channel Direct Memory Access device (DMA), which operates as a stand-alone sub-system, is devoted to image and intermediate data transfers, servicing interrupts when data transactions are complete. The computing cores, once programmed, work as peripheral units, processing raw data corresponding to the sensed images, and delivering processed information according to the programmed sequences of instructions.

The computing capabilities of the processing units are oversized to allow new functions and enhancements, such as including the speed of the vehicle together with the steering angle within the Locust model and improving the TpFE capabilities.





#### 4. System Integration into Cars and Test

Integration into a car and testing are the mandatory culmination of all tasks and the gateway for eventual practical usage. In addition, they are necessary for refinement of the models and the hardware/software processors. This latter task requires test platforms which are handy, manageable, open and flexible. Since these features are difficult to achieve with real cars, resorting to model cars is absolutely necessary during the first stages of model development and tuning.

Figure 14(a) shows the architecture of a model car (photo in Figure 14(b)) which is controlled via radio by interchanging control commands and state information with an external computer. The electronic system of the car comprises: a radio transceiver with a FSK modem; an expandable embedded single board computer for radio packet transmission management tasks; a full custom data IO handling control unit; peripheral control units devoted to control the electromechanical subsystems of the car; and a camera connected to a SHF emitter for image capture and transmission. The mechanical subsystem contains a servo for steering angle control, a high speed electric motor and differential drive.

For practical use, the model car must be complemented with scaled-down reproductions of the benchmark traffic scenarios considered. Realistic situations are replicated in these scenarios and the feedback from qualitative and quantitative tests employed to refine the models. Particularly, the model car is crucial for experimenting with dangerous traffic situations which are not feasible in real cars.

The most significant milestone of the model car tests is a stable hardware platform, ready to integrate into an actual car. A Volvo XC90 was prepared, mechanically and electrically, for that purpose. The sensor system was mounted into the specially made bracket in the interior rear mirror area as shown in Figure 15. A Head Up Display and an audible warning device were installed. The Head Up Display is the black plastic bar on the dashboard, in the front side of the instrument cluster cover. Inside the black plastic cover there is a row of red LEDs that are pointing at the windscreen (approximately 15cm up from the lower edge of the windscreen). When there is a collision alarm, a virtual brake light is projected on the windscreen glass as a red horizontal line. An audible warning is also given by activating the buzzer that is mounted in the *environmental node* which is connected to the CAN bus in the vehicle.

In-field tests covered many different scenarios involving pedestrians and other cars. To enhance the selectivity for objects moving in different directions, the image is divided into four regions (see picture at the top in Figure 16). The regions are defined by their separating sections and sections are defined by endpoints that can be dynamically adjusted to the geometry of the

road. Figure 16 shows some representative examples of the way this segmentation works. Problems are basically encountered with the handling of some shadows due to the monochrome and monocular nature of the sensor. In some cases, shadows produce false alarms. Ways to overcome this drawback requires either incorporating color information, or 3D vision or advanced adaptive brightness control algorithms.

#### Conclusions

Conventional engineering methodologies follow a *top-down* approach (system specification, behavioral modeling, architecture and block selection, block implementation, block assembling, system simulation and tuning, verification and refinement). Alternatively, biology has evolved to solve complex sensory-perception-actuation problems by following what can be considered as a *bottom-up* approach (systems evolve through the organization of elementary units which improve by following a kind of trial-and-error sequence of events). This paper outlines the main facets and results of a hybrid strategy that combines a bottom-up route from biological behaviors up to circuit implementations; and a top-down route from system specifications to processor and chip architectures and then finally to system integration and test.

Such hybrid methodological flow is needed to go from the mathematical modeling of the behavior of biological structures to the in-field test of collision threats in real traffic scenarios. The outcome of such a combination of multidisciplinary activities is the practical demonstration of the possibilities of biological systems when supplemented with proper circuit architecture design. It motivates further developments looking at the design of automotive-qualified vision processors for dealing with collision threats.

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Prof. Rodríguez-Vázquez founded and headed a research unit on High-Performance Analog and Mixed-Signal VLSI Circuits of the Institute of Microelectronics of Seville (IMSE-CNM). His team made pioneering R&D activities on bio-inspired microelectronics, including vision chips and neuro-fuzzy interpolators and controllers. His team also made significant contributions to the application of chaotic dynamics to communications, including the design and production of the first world-wide chaos-based communication MoDem chips. Some 30 high-performance mixed-signal chips were successfully designed by his team during the last 15 years in the framework of different R&D programs and contracts. These include three generation of vision chips for high-speed applications, analog front-ends for XDSL MoDems, ADCs for wireless communications, ADCs for automotive sensors, chaotic signals generators, complete MoDems for power-line communications, etc. Many of these chips are state-of-the-art in their respective fields. Some of them entered in massive production.

In 2001, he was one of the co-founders of AnaFocus, a high-technology company focused on the design of mixed-signal circuits with emphasis on CMOS smart imagers and bio-inspired vision systems on chip. He has been heading AnaFocus since 2004.

Prof. Rodríguez-Vázquez has authored/edited: eight books; around 40 chapters in contributed books, including original tutorials on chaotic integrated circuits, design of data converters and design of chips for vision; and more than 400 articles in peer-review specialized publications. He has served as Editor, Associate Editor and Guest Editor for different IEEE and non-IEEE journals, as chairman for different international conferences and is in the committee of some international journals and conferences. He has received a number of international awards for his research work (including the IEEE Guillemin-Cauer best paper award) and was elected Fellow of the IEEE for his contributions to the design of chaos-based communication chips and neuro-fuzzy chips. He is an IEEE Fellow.