Editorial

Power and timing modelling, optimisation and simulation

Practical implementations of digital VLSI circuits are more and more limited by power and timing constraints. On one hand, dissipating and reducing the increasing power density in modern high performance VLSI cores has become a typical design constraint; on the other hand, a wide spectrum of portable appliances demands for lower power consumptions in order to save battery life. All of these power-derived constraints come together with the higher performance demands that call for aggressive timing optimisation techniques.

In this scenario, the design and verification of current VLSI circuits and systems heavily relies on power and timing estimation techniques commonly implemented in CAD tools through the use of behavioural models. The development of these models and tools has become a major issue in the last decade, together with the improvement of low-power and high-performance design methods.

Since VLSI integration has reached the level of hundreds of million transistors in a single chip, full system verification at the transistor or gate levels is no longer feasible, leading to a variety of power and timing estimation and design techniques that apply to different levels of abstraction with very different coverage and accuracy objectives. There are several aspects that need attention from both research and development, including:

- Low-power design
- Timing-driven design
- Power and timing modelling
- Logic-level power and timing simulation
- High-level power and timing simulation
- Instruction-level optimisation
- Low-power encoding techniques.

The motivation behind bringing together this Special Section was born at the International Workshop on Power and Timing Modelling, Optimisation and Simulation (PATMOS) held in Turin in September 2003. This was the thirteenth in a series of international workshops held in several locations in Europe. Over the years, PATMOS has gained recognition as one of the major European events devoted to the power and timing aspects of integrated circuit and system design. Proceedings for this meeting are available through Springer-Verlag's *Lecture Notes in Computer Science* collection. Some of the most appreciated contributions to this edition of the workshop, covering major topics of the area, have been expanded and updated for this Special Section of *IEE Proceedings Computer & Digital Techniques*. All this has been possible thanks to the excellent work and support of the IEE editorial staff and the PATMOS Technical Program Committee.

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