LOW-POWER LOGIC STYLES FOR FULL-ADDER CIRCUITS[1]

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ABSTRACT

This paper contributes to a better knowledge of the behaviour of conventional CMOS and CPL full-adder circuits when low voltage, low power or small power-delay products are of concern. It completes and overcomes limitations of previous studies as optimal power-delay curves, for CPL and CMOS full adders, have been built up using an automatic sizing tool based on statistical optimization. Supply voltages of 3.3V and 1.5V have been considered. This study shows that full adders with minimum power consumption are accessible by using the conventional CMOS design style. As a counterpart, minimum delay full adders are obtained with CPL.

1. INTRODUCTION

Requirements of portability and reliability for electronic circuits lead to an increasing importance of the power consumption issues. If these requirements are addressed at the circuit design level, the selection of a proper design style is of capital importance. That is because the logic style strongly influences parameters such as switching capacitance, transition activity, and short-circuit currents, which are the parameters governing power dissipation.

Conventional CMOS logic style presents robustness against voltage scaling and high noise margins, so allowing a reliable operation at low voltages. Pass-transistor logic styles have emerged as an attractive replacement for conventional CMOS logic. In particular, Complementary Pass-Transistor Logic (CPL) is a well known low-power logic style. Pass-transistor logic is attractive as fewer transistors are needed to implement important logic functions, uses smaller transistors and smaller capacitances than conventional CMOS.

The specialized literature [1-8] reflects the amount of work performed on proper choice of the best logic style for the implementation of specific circuits, namely full-adders. One of the main reasons for this is that full-adders are circuits widely used in arithmetic circuits, for example in multipliers, where they are key macrocells. Recently, there has been some controversy concerning the best low-power logic style for building full-adder circuits [9]. Comparisons of full-adder circuits have used the best solution (in transistor count) for CPL solutions but a suboptimal one for the CMOS counterpart. So, these comparisons are not representative enough. In addition, the key issue of transistor sizing is, in general, not addressed. A single full-adder of each type are compared without any mention to the criteria for transistor sizing. Thus, a more refined study is needed.

This paper aims to fulfil this gap by contributing to a better knowledge of the behaviour of conventional CMOS and CPL full-adder circuits when low voltage, low power or small power-delay products are of concern. The methodology we have used to perform this study is based on the building of the optimal power-delay curves for both approaches. It sizes the circuit transistors in order to obtain optimal circuits, that is, circuits placed on the optimal power-delay curve. That search has been done using FRIDGE [10], an automatic sizing tool based on statistical optimization. The tool allows to obtain transistor sizes through a constrained optimization problem solved following an iterative procedure built around an electrical simulator. Resulting transistor sizes provide the closest solution found covering all the specifications.

The paper is organized as follows. Section II reviews basic concepts on full-adders and shows the schematics for the two full-adders studied. Section III describes how the optimal power-delay curves have been obtained. In Section IV, the results of this study are discussed and finally, some conclusions are given.

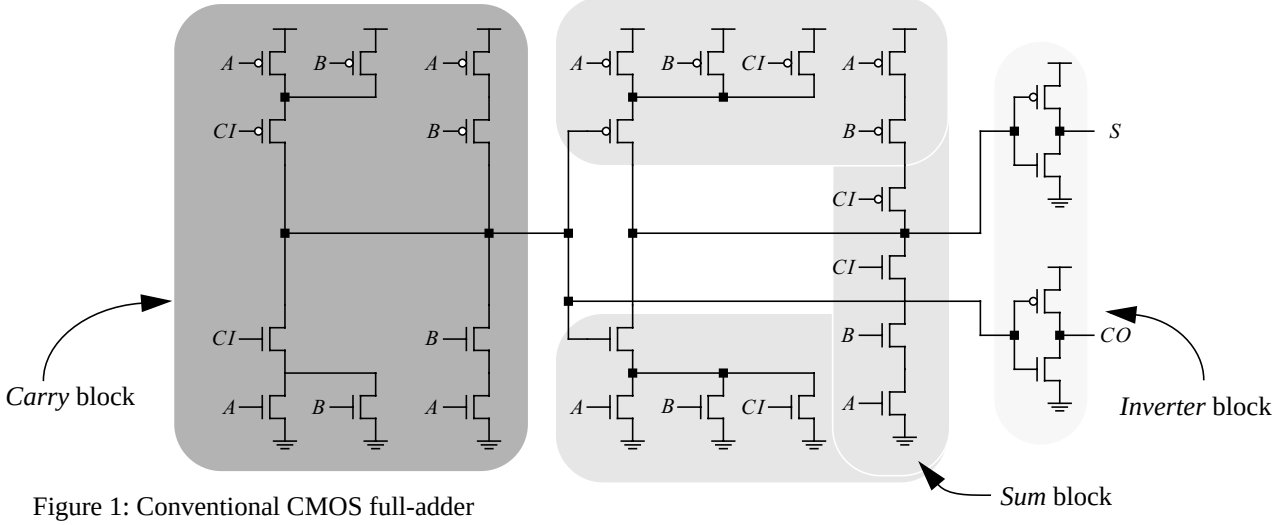

Figure 1: Conventional CMOS full-adder

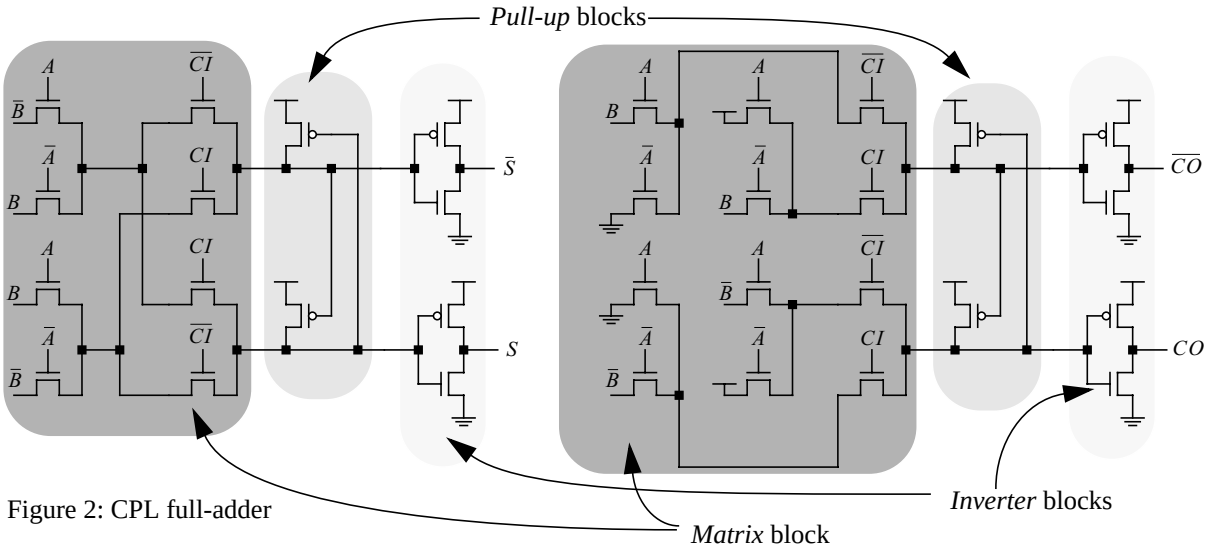

Figure 2: CPL full-adder

2. FULL ADDERS

A full-adder (FA) is a logic circuit which takes three binary inputs, A, B, and CI and provides two binary outputs, S and CO, the *Sum* bit and the *Carry-out* bit. Binary number $(CO\ S)$ is the binary representation of the arithmetic sum of the inputs. Basic logic equations for outputs S and CO can be easily obtained:

$$\begin{aligned} S &= A \oplus B \oplus CI \\ CO &= A \cdot B + A \cdot CI + B \cdot CI \end{aligned} \qquad (1)$$

There are many different realizations for the static CMOS one-bit FA. The two design style alternatives to be considered in this study are the conventional CMOS logic style and the CPL logic style. The schematics used as inputs to the automatic sizing tool are shown in Figures 1 and 2. The conventional CMOS circuit shown in Figure 1 uses the 28-transistor version [2] (instead the often-used 40-transistor version). This circuit presents some logic optimization because it uses variable $\overline{CO}$ in the calculation of the *Sum* bit. The CPL version [2] is shown in Figure 2.

The conventional CMOS FA:

A closer study of the schematic in Figure 1 reveals three relevant blocks whose transistors must be sized carefully: the *Carry* block, the *Sum* block and the *Inverter* block. The transistor sizing parameters which must be optimized by the automatic sizing tool are:

	*n*MOS	*p*MOS
Carry block	$(w_n)_C$	$(w_p)_C$
Sum block	$(w_n)_S$	$(w_p)_S$
Inverter block	$(w_n)_I$	$(w_p)_I$

Lengths are fixed at 0.8µm.

The CPL FA:

Schematic in Figure 2 also reveals three relevant blocks: the *Matrix* block, the *Pull-up* block and the *Inverter* block. Also, all the transistor lengths have been fixed at 0.8μm. Now, the transistor sizing parameters are:

	*n*MOS	*p*MOS
Matrix block	$(w_n)_M$	—
Pull-up block	—	$(w_p)_P$
Inverter block	$(w_n)_I$	$(w_p)_I$

Next, we describe the process followed to obtain the optimal power-delay curves.

3. OPTIMAL POWER-DELAY CURVES

The question about the best low-power logic style (conventional CMOS or CPL) for FA circuits can be answered by building the optimal power-delay curves for both of them. For that, transistor sizes that provide the minimum power consumption for a given delay must be obtained.

Derivation of optimal power-delay curves is a very time-consuming task, and generally requires a deep knowledge of the electrical behaviour of the circuit. We have eased this task by resorting to FRIDGE [10], an automatic sizing tool based on statistical optimization which is able to start from an arbitrary initial point. FRIDGE is built on top of the electrical simulator HSPICE and it is able to accept constraints on different design objectives.

The procedure we have followed begins calculating the power consumption and the delay of the circuit when minimum size transistors are assumed. This point in the power-delay curve is called minimum-size point (the MS point placed at the right end of the curve) and its delay is used as the initial point for subsequent optimizations. Next, a FRIDGE loop is started. At each iteration, a delay constraint (a vertical line in a power-delay curve) less than the previous one, is fixed. This constraint separates the feasible region (on the left) from the infeasible one (on the right). FRIDGE tries to obtain the optimal circuit, i.e., the transistor sizes which minimize the power consumption and meet the delay constraint. Case of obtaining a solution, a new point in the optimal power-delay curve is added. In other case, the loop is broken. So, the procedure ends when the automatic tool is not able to provide a solution for the given delay. The point of minimum delay (the MD point placed at the left end of the curve) has been reached and no further solution is possible. As FRIDGE is based on HSPICE, power dissipation and delay are accurately assessed. 20 MHz input waveforms containing all possible transition of input combinations are simulated and the worst case delay and the RMS power dissipation obtained from this simulation. Both circuits have been loaded in a similar way, a typical load for full-adder applications.

The procedure above described has been applied to the circuits in Figures 1 and 2 with supply voltages of 3.3V and 1.5V and an standard 0.8 mm CMOS process technology. Figures 3 and 4 show the power-delay curves obtained (solid line curves) for 3.3 and 1.5, respectively. It is also interesting to study how these curves are modified if the layout of the circuits is taken into account. Each optimal power-delay circuit has been laid out. Layouts for the conventional CMOS circuits have been automatically generated in CADENCE. However, we have resorted to a full-custom layout style for the CPL circuits as it has been documented [9] the high sensitivity to parasitics that this logic style exhibits. The dashed-line curves in the Figures come from post-layout simulations.

4. RESULTS AND COMPARISONS

From the solid line curves in Figure 3 and Figure 4, some important facts can be derived. First, the wide range where conventional CMOS solutions can be found. By an adequate sizing of transistors, delays between 1.6ns and 3.2ns for 3.3V, and delays between 7.5ns and 19.9ns for 1.5V can be obtained for this design style. When CPL solutions are considered, the interval is much smaller, between 1.3ns and 2.2ns for 3.3V and between 6.5ns and 10.1ns for 1.5V. Power consumption for conventional CMOS style ranges also in a wider interval, from 130μw to 872μw for 3.3V and from 11μw to 91μw for 1.5V, when compared to CPL solutions ([276μw, 523μw] for 3.3V and [22μw, 44μw] for 1.5V).

Secondly, solutions with a power consumption below 276μw for 3.3V and 22μw for 1.5V are accessible only by using the conventional CMOS design style. There are no CPL solutions. As a counterpart, there are no conventional CMOS solutions if a delay below 1.6ns for 3.3V and 7.5ns for 1.5V is required. There are only CPL solutions.

Finally, there is a crosspoint between CPL and conventional CMOS curves both for 3.3V and 1.5V. They are placed at $CP_{3.3V}$, (2ns, 282μw), for the 3.3V curve and at $CP_{1.5V}$, (9.8ns, 22μw), for the 1.5V one. This means that in the region where both solutions are possible, for a given

power consumption above the corresponding to the crosspoint, CPL solutions exhibit less delay than conventional CMOS solutions. Also, if the power consumption is below the corresponding crosspoint, the conventional CMOS solutions have less delay than CPL ones. A similar analysis is applicable to the delay. In consequence, the best option for building full adders uses CPL logic style for circuits placed at the left of the crosspoint and conventional CMOS solutions for points at the left of the crosspoint.

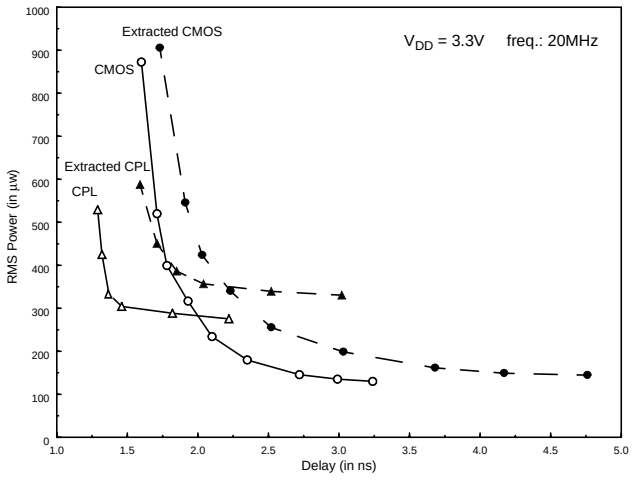

Figure 3: Power-delay curves for V_{DD}=3.3V

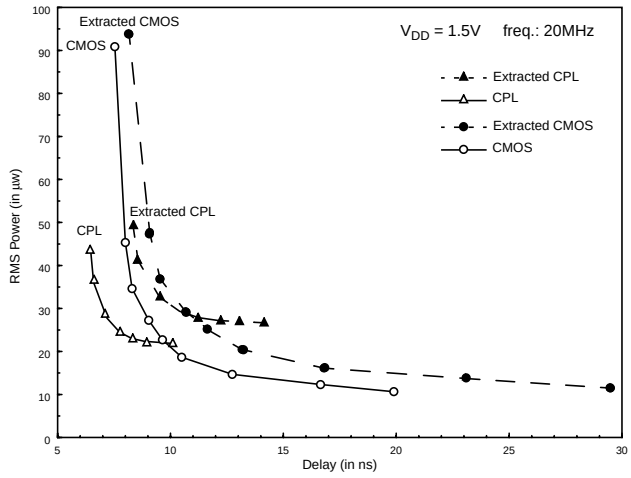

Figure 4: Power-delay curves for V_{DD}=1.5V

5. CONCLUSION

Optimal power-delay curves for CPL and CMOS full adders for supply voltages of 3.3V and 1.5V have been built up. These curves show that both logic styles can exhibit performance advantages depending on the constraints imposed by each particular application. CMOS produces the more power efficient solutions while CPL generates the shortest delay designs.

6. REFERENCES

[1] A.P. Chandrakasan and R.W. Brodersen, *Low-Power Digital CMOS Design*. Norwell, MA: Kluwer, 1995.

[2] N.H.E. Weste and K. Eshrahgian, *Principles of CMOS VLSI Design*. Reading, MA: Addison-Wesley, 1985.

[3] J.-M. Masgonty C. Arm, and C. Piguet, "Technology- and power-supply-independent cell library," in *Proc. IEEE Custom Integrated Circuits Conf.,* San Diego, CA, May 1991, pp. 25.5/1-4

[4] N. Zhuang and H. Wu, "A New Design of the CMOS Full Adder," *IEEE J. Solid-State Circuits*, vol. 27, no. 5, pp. 840-844, May 1992

[5] K. Yano, Y. Sasaki, K. Rikino, and K. Seki, "Top-Down Pass-Transistor Logic Design," *IEEE J. Solid-State Circuits*, vol. 31, no. 6, pp. 792-803, June 1996.

[6] A. Parameswar, H. Hara, and T. Sakurai, "A Swing Restored Pass-Transistor Logic-Based Multiply and Accumulate Circuit for Multimedia Applications," *IEEE J. Solid-State Circuits*, vol. 31, no. 6, pp. 805-809, June 1996.

[7] I.S. Abu-Kather, A. Bellaouar, and M.I. Elmasri, "Circuit Techniques for CMOS Low-Power High-Performance Multipliers," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1536-1546, Oct. 1996.

[8] M. Izumikawa *et al.*, "A 0.25-µm CMOS 0.9-V 100-MHz DSP Core," *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 52-61, Jan. 1997.

[9] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079-1090, July 1997.

[10] F. Medeiro, R. Rodríguez-Macías, F.V. Fernández, R. Domínguez-Castro, J.L. Huertas, and A. Rodríguez-Vázquez, "Global Design of Analog Cells Using Statistical Optimization Techniques," *Analog Integrated Circuits and Signal Processing*, vol. 6, pp. 179-195, Kluwer Academics Pubs., Nov. 1994.