

Undersampling RF-to-Digital CT $\Sigma\Delta$ Modulator with Tunable Notch Frequency and Simplified Raised-Cosine FIR Feedback DAC

Sohail Asghar, Rocío del Río and José M. de la Rosa

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla)

C/Américo Vespucio, 41092 Sevilla, SPAIN

E-mail: [asghar,rocio,jrosa]@imse-cnm.csic.es

Abstract—This paper presents a continuous-time fourth-order band-pass $\Sigma\Delta$ Modulator for digitizing radio-frequency signals in software-defined-radio mobile systems. The modulator architecture is made up of two resonators and a 16-level quantizer in the feedforward path and a raised-cosine finite-impulsive-response feedback DAC. The latter is implemented with a reduced number of filter coefficients as compared to previous approaches, which allows to increase the notch frequency programmability from $0.0375f_s$ to $0.25f_s$, while keeping stability and robustness to circuit-element tolerances. These features are combined with undersampling techniques to achieve an efficient and robust digitization of 0.455-to-5GHz signals with scalable 8-to-15bit effective resolution within 0.2-to-30MHz signal bandwidth, with a reconfigurable 1-to-4GHz sampling frequency¹.

I. INTRODUCTION

Future generations of Software-Defined-Radio (SDR) transceivers will perform most of the signal processing in the digital domain, thus allowing to increase the programmability and adaptability to a large number of standards and operation modes of the hand-held devices based on this technology. The most critical key building block enabling such a technology is the Analog-to-Digital Converter (ADC). This circuit should be ideally placed at the antenna so that Radio Frequency (RF) signals could be directly digitized, thus being processed in a flexible way by running software on a Digital Signal Processor (DSP) [1].

Unfortunately, the efficient implementation of SDR mobile terminals is still far from a consumer product deployment, mostly limited by the unfeasible power-hungry specifications required for the ADC. However, recent advances in Continuous-Time (CT) Sigma-Delta Modulation ($\Sigma\Delta$) techniques – fueled by the continuous downscaling of CMOS processes – are pushing RF digitization forward, taking significant steps towards making SDR-based phones a reality [2]–[7].

The majority of reported RF *digitizers* are Band-Pass (BP) CT- $\Sigma\Delta$ Ms which include diverse strategies to reduce the required sampling frequency and mitigate the impact of interference signals. Among others, some of the proposed techniques are frequency-translation [8], out-of-band embedded filtering

[5] and *undersampling* or *subsampling* [2], [3], [7], [9], [10]. The latter allows to digitize RF signals placed at $f_{RF} > f_s/2$ (with f_s being the sampling frequency), while still keeping high values of the OverSampling Ratio (OSR), since the signal bandwidth is typically $B_w \ll (f_{RF}, f_s)$ [9], [10].

The performance of undersampling $\Sigma\Delta$ Ms is mainly degraded by two major limiting factors. One is the attenuation of the RF alias signal in the Nyquist band and the other is the reduction of the quality factor of the noise transfer function. These problems can be partially mitigated by combining Finite-Impulsive-Response (FIR) filters and raised-cosine waveform for the Digital-to-Analog Converter (DAC) in the feedback path of the modulator [7], [11], [12]. However, this approach increases in practice the number of $\Sigma\Delta$ M loop-filter coefficients, with the subsequent penalty in terms of sensitivity to technology process variations and limited range of notch frequency programmability while keeping stable behavior.

This problem, which is aggravated as the loop-filter order increases, is addressed in this paper by simplifying the implementation of undersampling CT BP- $\Sigma\Delta$ Ms with raised-cosine FIR DACs. The proposed architecture reduces the required number of feedback paths and gain coefficients, while providing excess loop delay compensation and guaranteeing stability and the equivalence with the corresponding Discrete-Time (DT) system in a widely programmable range of 0.0375 -to- $0.25f_s$ notch frequencies. These features are put together and applied to the system-level design of a fourth-order topology with embedded 4-bit quantization intended for RF-to-Digital conversion in SDR applications.

II. DESIGN CONSIDERATIONS OF RF $\Sigma\Delta$ MS

Fig. 1 shows the conceptual block diagram of a SDR receiver, where after being filtered and preamplified by the LNA, RF signals are digitized by a CT BP- $\Sigma\Delta$ M and most of the signal processing is carried out by a DSP. The majority of reported BP- $\Sigma\Delta$ Ms use a fixed notch frequency, f_n , and hence a widely programmable frequency synthesizer is required to place the in-coming signal within the passband of the BP- $\Sigma\Delta$ M. Alternatively, the design of the synthesizer can be simplified if a reconfigurable BP- $\Sigma\Delta$ Ms with tunable f_n is used instead [6].

¹This work was supported by the Spanish Ministry of Science and Innovation (with support from the European Regional Development Fund) under contract TEC2010-14825/MIC.

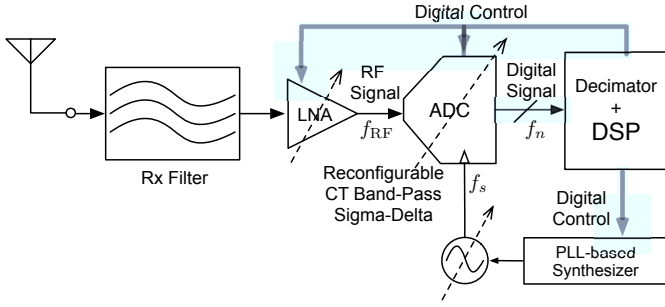


Fig. 1. Conceptual diagram of a SDR receiver based on a CT BP- $\Sigma\Delta$ M.

A. Modulator Specifications

In order to find out the specifications of a BP- $\Sigma\Delta$ M in a SDR receiver like that shown in Fig. 1, a number of wireless standards were considered, namely: GSM, EDGE, GPRS, CDMA-2000, WCDMA, Bluetooth, WLAN (IEEE 802.11a/b/n), WiMAX and LTE. Handling all these operating modes in the SDR of the system in Fig. 1 requires digitizing signals with carrier frequencies ranging from 0.455GHz (CDMA-2000) to 5.093GHz (WiMAX) with channel bandwidths (B_w) varying from 0.2MHz (GSM) to 30MHz (LTE).

The calculation of the required Dynamic Range (DR) involves considering the different ranges of input signals for each standard, ranging from the minimum level (determined by the standard sensitivity) to the strongest out-of-band blockers, while satisfying the required Noise Figure (NF) and linearity. As a case study, and considering a LNA with 15-dB gain, 3-dB NF and an off/on chip blocker attenuation of 15dB, the computation of the BP- $\Sigma\Delta$ M effective resolution – beyond the scope of this paper – yields to a scalable DR of 90dB to 50dB from $B_w = 200$ kHz to $B_w = 30$ MHz, respectively.

B. Benefits of Undersampling

The modulator requirements detailed above imposes very aggressive specifications, particularly in terms of the sampling frequencies required by the ADC. These requirements can be relaxed by using undersampling techniques. To this end, let us consider that RF signals with bandwidth, B_w , are located at a given frequency, f_{RF} , and they are processed in Fig. 1 by a BP- $\Sigma\Delta$ M working at f_s . In terms of the carrier signal at f_{RF} , the signal is *undersampled*, since $f_s < 2f_{RF}$. However, in terms of B_w , the modulating signal, which contains the information, is *oversampled* since $B_w \ll f_s$.

Therefore, the output spectrum of the BP- $\Sigma\Delta$ M in Fig. 1 has a replica of the input (RF) signal with noise shaped at a lower frequency, f_n , given by [13]:

$$f_n = \begin{cases} \text{rem}(f_{RF}, f_s) & \lfloor \frac{2f_{RF}}{f_s} \rfloor \text{ is even} \\ f_s - \text{rem}(f_{RF}, f_s) & \lfloor \frac{2f_{RF}}{f_s} \rfloor \text{ is odd} \end{cases} \quad (1)$$

where $\text{rem}(x, y)$ stands for the remainder of x/y . Note from the above expression that in order to downconvert a RF signal without overlapping, three conditions need to be fulfilled: (a) $f_s > 2B_w$ (Nyquist theorem); (b) $f_n - B_w/2 > 0$ and (c) $f_n < f_s - B_w/2$. As an illustration, Table I shows several

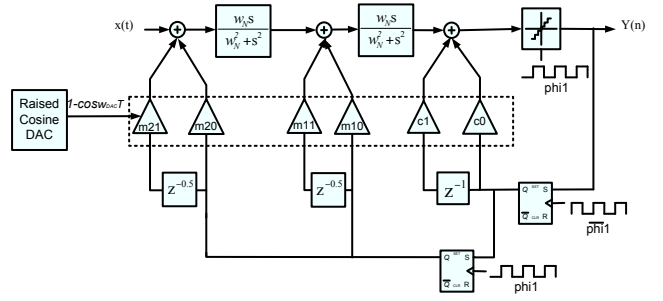


Fig. 2. Block diagram of the proposed undersampling CT BP- $\Sigma\Delta$ M.

alternative values of f_s and f_n for different wireless standards under consideration. Therefore, taking into account the three mentioned conditions (a)-(c) and the whole range of f_{RF} to be covered by the undersampling BP- $\Sigma\Delta$ M in Fig. 1, f_s should be programmable to the following values: 1, 2, 2.5 and 4GHz. In addition, a widely programmable value of f_n is required, ranging from $0.0375f_s$ to $0.237f_s$.

III. PROPOSED RF-TO-DIGITAL $\Sigma\Delta$ M ARCHITECTURE

Fig. 2 shows the block diagram of the proposed CT BP- $\Sigma\Delta$ M. It consists of a fourth-order single-loop topology made up of two resonators. In order to reduce the impact of alias signal attenuation a raised cosine DAC has been used and combined with half-delayed FIR based feedback loop in order to increase the degrees of freedom in the synthesis process when applying a DT-to-CT transformation method [11].

Two additional feedback paths, with gains c_0 and c_1 , are included to compensate for the excess loop delay error. The latch driving the first compensation path, i.e. the path with gain c_0 , has the opposite phase to the clock signals driving the quantizer and the other feedback paths. The second compensation path is introduced with a full sampling-period delay. This way, the modulator exhibits a full digital delay between the quantizer output and main DAC inputs. Also a minimum of one full delay does exist between the modulator output to the input of the quantizer through both compensation paths, which gives a full sampling-period delay margin for the quantizer+DAC operation.

Compared to previous approaches of CT BP- $\Sigma\Delta$ M based on raised-cosine FIR feedback DACs [7], [11], the proposed architecture uses a two-tap FIR structure instead of three-tap

TABLE I
ALTERNATIVES VALUES OF f_n AND f_s FOR DIFFERENT STANDARDS

Standard	f_{RF} (GHz)	f_s (GHz)	f_n (GHz)	f_n/f_s
CDMA-450	0.455	0.25	0.045	0.18
		0.50	0.045	0.09
		2	0.455	0.28
GSM (850-MHz Band)	0.882	0.5	0.119	0.24
		4	0.882	0.22
CDMA (2.14-GHz Band)	2.14	1	0.14	0.14
		2	0.14	0.07
WiMax (5-GHz Band)	5.09	1.25	0.094	0.08
		2.5	0.094	0.04
		5	0.094	0.02

based implementation. For instance, the modulator in [11] uses 16 feedback coefficients instead of only 6 coefficients used in the proposed architecture. This simplification of the loop-filter implementation results in an improvement of the sensitivity of the modulator with respect to circuit-element tolerances and mismatches. The latter is particularly critical in SDR applications, since a high degree of tunability is required to have a widely programmable notch frequency as stated in previous section.

The modulator is synthesized in two steps. First, a DT BP- $\Sigma\Delta M$ is obtained from an equivalent Low-Pass (LP) system which fulfills the required specifications. Second, a DT-to-CT transformation is applied to obtain the desired CT system.

A. LP-to-BP Transformation

The desired fourth-order DT BP- $\Sigma\Delta M$ is obtained by applying the following transformation [14]:

$$z^{-1} \rightarrow \frac{\cos(2\pi f_n)z^{-1} - z^{-2}}{\cos(2\pi f_n)z^{-1} - 1} \quad (2)$$

to a LP- $\Sigma\Delta M$ which satisfies the required specifications in terms of DR and B_w , for the different standards stated in Section II. This way, applying the transformation in (2) to the Noise Transfer Function (NTF) of a second-order LP- $\Sigma\Delta M$, the desired $NTF(z)$ is obtained for a fourth-order BP- $\Sigma\Delta M$ with center frequency at f_n . Once the desired BP $NTF(z)$ is obtained, the loop filter transfer function, can be easily derived as $H(z) = 1 - 1/NTF(z)$.

B. DT-to-CT Transformation

The loop-filter transfer function, $H(s)$, of the CT BP- $\Sigma\Delta M$ is derived from the well-known DT-to-CT equivalence:

$$H(z) \equiv Z\{L^{-1}[H(s) \cdot H_{\text{COS-FIR-DAC}}(s)]\} \quad (3)$$

where $Z(\cdot)$ and $L(\cdot)$ denotes the Z -transform and L -transform symbols and $H_{\text{COS-FIR-DAC}}(s)$ is the transfer function of the raised-cosine FIR-based DAC. As this DAC transfer function uses half-delay, modified Z -transform is a more suitable technique to compute (3) with delays which are not integral multiples of the sampling time [11].

In order to calculate the modified Z -transform of (3), partial fraction forms were considered for the different resonator feedback paths including the unit delay in Fig. 2, expressed as:

$$TF_{m_{uv}}(z) = \sum_{k=1}^2 \left[\frac{a_k}{(p_k + z)^k} + \frac{a_k^*}{(p_k^* + z)^k} \right] + \frac{b_1}{z} + \frac{b_2}{z^2} \quad (4)$$

where subscript $m_{u,v}$ denotes the different gains used in the feedback paths, and $u, v = 1, 2$ and (p_k, p_k^*) stand for the complex conjugate poles of the transfer function for a given f_n . Two additional terms, b_1/z and b_2/z^2 , result from the mentioned partial form decomposition. These terms can be cancelled out by the compensation feedback paths, with gains c_0 and c_1 . This way, applying superposition and replacing all

expressions of $TF_{m_{uv}}(z)$ in (3), the modulator loop-filter coefficients, m_{1k} , m_{2k} and c_k , with $k = 0, 1$, can be obtained for all required values of f_n . As an illustration, Table II shows the values of a_k and b_k obtained from replacing $TF_{m_{uv}}(z)$ in (3) for $f_n = 0.2f_s$ ($p_1 = p_2 = -0.309 \pm 0.95i$, where $i \equiv \sqrt{-1}$). In this case, the corresponding TFs for the compensation paths are $TF_{c_0} = 2z^{-1}$ and $TF_{c_1} = 2z^{-2}$, and the resulting loop-filter coefficients are $m_{10} = 0.3$, $m_{11} = 0.53$, $m_{20} = 0.048$, $m_{21} = 0.037$, $c_0 = 0$ and $c_1 = 0.25$.

Following the same procedure, loop-filter coefficients can be calculated for different values of f_n as illustrated in Table III.

IV. SIMULATION RESULTS

Fig. 3 shows the output spectra for different cases of notch frequencies corresponding to RF signals located at 0.44 GHz (Fig. 3(a)), 2.14GHz (Fig. 3(b)) and 5.09GHz (Fig. 3(c)). Combining undersampling techniques with reconfigurable f_n , the modulator is able to digitize RF signals lying within the ranges $0.7875f_s$ -to- f_s , $1.7875f_s$ -to- $2f_s$, $2.7875f_s$ -to- $3f_s$, $3.7875f_s$ -to- $4f_s$, etc. The modulator can operate in a normal operation, i.e. without using undersampling, with a variable $0.0375f_s$ -to- $0.25f_s$ value of f_n . This way, as illustrated in Table I, a number of different signal frequencies and bandwidths in the range of $B_w = 0.2$ -to-30MHz, can be handled with an scalable 90-to-50dB SNR. As an illustration, Fig. 4 shows several SNR-versus-input level curves considering different cases of input signal bandwidths and notch frequencies depicted in Fig. 3.

As stated in previous sections, one of the benefits of the presented architecture is the reduced number of coefficients, which is directly translated in a lower sensitivity to mismatch and circuit-element tolerances. As an illustration of the robustness of the proposed $\Sigma\Delta M$, Fig. 5 shows the histogram of SNR of a 150-run Monte Carlo simulation for CDMA-450 (Fig. 5(a)) and WiMAX (Fig. 5(b)) standards. In both cases an standard deviation of 10% was considered in all loop-filter coefficients. It can be shown how the SNR is degraded in 3-4dB in the worst cases.

TABLE II
VALUES OF a_i , b_i AND p_i IN (4) FOR $f_n = 0.2f_s$

$TF_{m_{uv}}$	a_1	a_2	b_1	b_2
$TF_{m_{10}}$	$0.49 \pm 0.35i$	0	-1	0
$TF_{m_{11}}$	$0.18 \pm 0.58i$	0	-0.43	-0.61
$TF_{m_{20}}$	$-0.32 \pm 0.12i$	$0.31 \pm 0.22i$	0.65	0
$TF_{m_{21}}$	$0.39 \pm 0.27i$	0.38	0.78	0.11

TABLE III
LOOP-FILTER COEFFICIENTS FOR DIFFERENT VALUES OF f_n/f_s

Coefficient	$f_n = 0.06f_s$	$f_n = 0.15f_s$	$f_n = 0.246f_s$
m_{10}	-1.42	-0.91	3.13
m_{11}	0	0.98	0.63
m_{20}	-0.14	-0.17	-0.24
m_{21}	-0.13	0.15	3.31
c_0	-0.5	0.18	-0.22
c_1	0	0.20	0

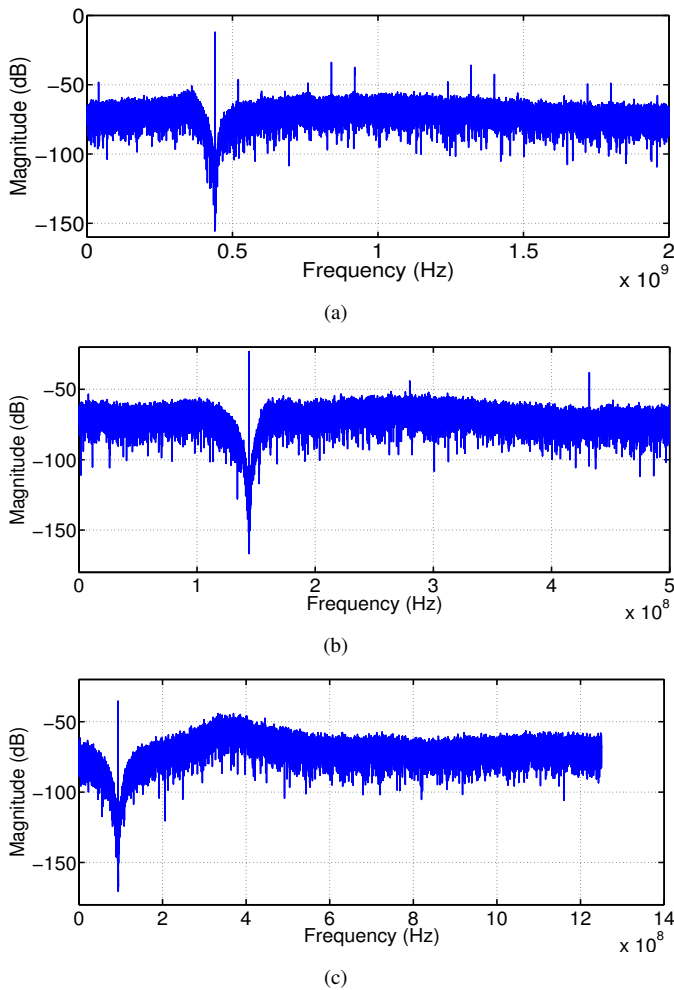


Fig. 3. Modulator output spectra for different cases of f_{RF} and f_s : (a) $f_{RF} = 0.44\text{GHz}$, $f_s = 1\text{GHz}$ (normal operation) (b) $f_{RF} = 2.14\text{GHz}$, $f_s = 1\text{GHz}$ and (c) $f_{RF} = 5.09\text{GHz}$, $f_s = 2.5\text{GHz}$ (undersampling operation).

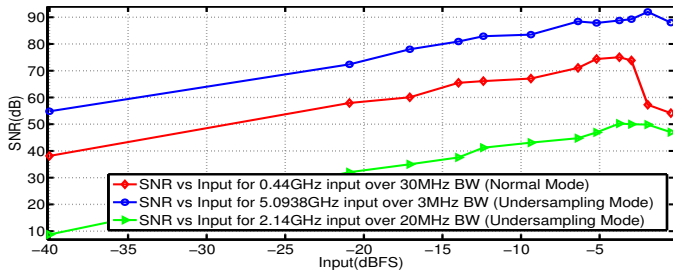


Fig. 4. SNR versus input signal level for different input signals.

V. CONCLUSIONS

An improved implementation of an undersampling CT BP- $\Sigma\Delta$ s with raised-cosine FIR feedback DAC has been presented. The modulator architecture reduces the number of loop-filter coefficients with respect to previous approaches, which results in a larger robustness with respect to mismatch, while keeping stability and a complete equivalence between the discrete-time system and the continuous-time implementation. These advantages make the proposed modulator very suited for RF digitization in next generation software-defined-radio mobile systems.

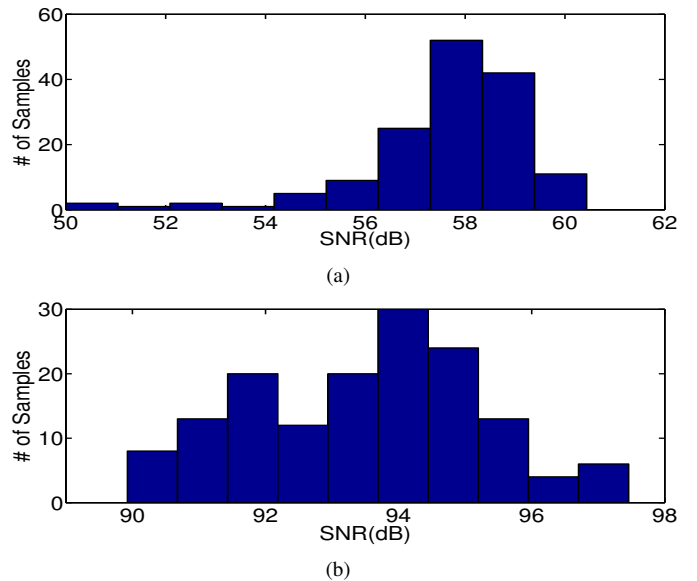


Fig. 5. Monte Carlo simulations for two different standards: (a) CDMA-450 ($f_{RF} = 0.44\text{GHz}$) (b) WiMAX ($f_{RF} = 5.09\text{GHz}$).

REFERENCES

- [1] J. Mitola, "The Software Radio Architecture," *IEEE Communications Magazine*, pp. 26–38, May 1995.
- [2] J. Ryckaert, J. Borremans, B. Verbruggen, L. Bos, C. Armiento, J. Craninckx, and G. van der Plas, "A 2.4 GHz Low-Power Sixth-Order RF Bandpass $\Sigma\Delta$ Converter in CMOS," *IEEE J. of Solid-State Circuits*, vol. 44, pp. 2873–2880, November 2009.
- [3] N. Beilleau, H. Aboushady, F. Montaudon, and A. Cathelin, "A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass $\Sigma\Delta$ ADC for a SDR ISM-band Receiver in 130nm CMOS," *Proc. of the IEEE Radio Frequency Integrated Circuits Symp.*, 2009.
- [4] J. Ryckaert *et al.*, "A 6.1GS/s 52.8mW 43dB DR 80MHz Bandwidth 2.4GHz RF Bandpass $\Sigma\Delta$ ADC in 40nm CMOS," *Proc. of the IEEE Radio Frequency Integrated Circuits Symp.*, pp. 443–446, June 2010.
- [5] K. Koli *et al.*, "A 900-MHz Direct Delta-Sigma Receiver in 65-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 45, pp. 2807–2818, December 2010.
- [6] H. Shibata *et al.*, "A DC-to-1GHz Tunable RF $\Sigma\Delta$ ADC Achieving DR=74dB and BW=150MHz at $f_0 = 450\text{MHz}$ Using 550mW," *IEEE ISSCC Digest of Technical Papers*, pp. 150–151, February 2012.
- [7] S. Gupta *et al.*, "A 0.8-2GHz Fully-Integrated QPLL-Timed Direct-RF-Sampling Bandpass $\Sigma\Delta$ ADC in 0.13 μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 47, pp. 1141–1153, May 2012.
- [8] H. Tao and J. M. Khoury, "A 400-MS/s Frequency Translating Bandpass Sigma-Delta Modulator," *IEEE J. of Solid-State Circuits*, vol. 34, pp. 1741–1752, December 1999.
- [9] A. I. Hussein and W. Kuhn, "Bandpass $\Sigma\Delta$ Modulator Employing Undersampling of RF Signals for Wireless Communications," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, pp. 614–620, July 2000.
- [10] A. Naderi, M. Sawan, and Y. Savaria, "On the Design of Undersampling Continuous-Time Bandpass Delta-Sigma Modulators for Gigahertz Frequency A/D Conversion," *IEEE Trans. on Circuits and Systems – I: Regular Papers*, vol. 55, pp. 3488–3499, December 2008.
- [11] N. Beilleau, H. Aboushady, and M. Loureat, "Using Finite Impulse Response Feedback DACs to design $\Sigma\Delta$ Modulators based on LC Filters," *Proc. of the IEEE Intl. Midwest Symp. on Circuits and Systems (MWSCAS)*, pp. 696–699, August 2005.
- [12] A. Ucar, E. Cetin, and I. Kale, "A Continuous-Time Delta-Sigma Modulator for RF Subsampling Receivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, pp. 272–276, May 2012.
- [13] D. M. Akos *et al.*, "Direct Bandpass Sampling of Multiple Distinct RF Signals," *IEEE Trans. on Communications*, vol. 47, pp. 983–988, July 1999.
- [14] A. K. Ong, *Bandpass Analog-to-Digital Conversion for Wireless Application*. Stanford University, PhD dissertation, 1998.