Evaluation of the AMS 0.35 μm CMOS Technology for Use in Space Applications

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AMS 0.35 μm CMOS for Space Applications

- **Introduction**
- The Characterization Plan
- Low-Temperature Characterization
- Equivalent Width for ELTs
- TID Characterization
- SEE Characterization
- Conclusions and Future Work

Introduction

- Application of IMSE and US Mixed-Signal Design expertise to space ASICs
  - Collaboration with Instituto Nacional de Técnica Aeroespacial (INTA) started in 2008
  - Selection of technology from an European foundry (AMS 0.35µm)
    - Mature, reliable, long-life (automotive market)
    - Reduced prototyping and low-volume production cost
    - Suitable for moderate performance MS designs
  - Start from the ground (technology evaluation and characterization)

Design, then try to see what happens….. or

See what happens, then design!

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The Characterization Plan

- Objectives
- Test Chips
- Test Hardware
- Test Software
- Test Facilities

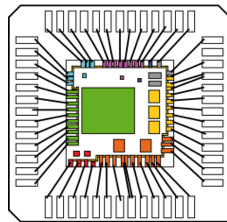
Objectives

- Evaluation
  - At low-temperature (-110ºC)
  - Radiation (TID, SEE)
- Development
  - Models of Enclosed-Layout Transistors
  - RHBD Digital Library
- Application
  - Two instrumentation chips for Mars missions
  - Future use in internal projects and in collaboration with other interested groups

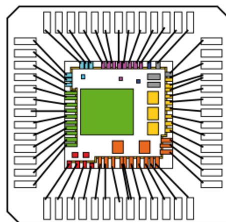
Test Chips (1)

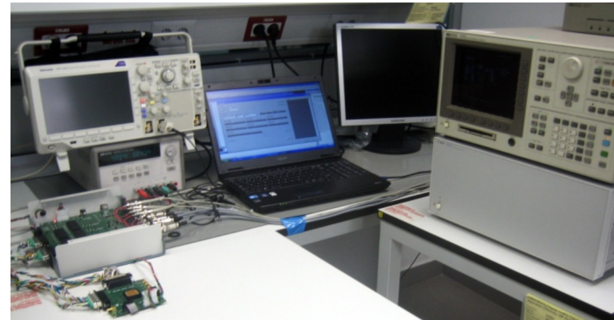
MOS Transistors
Bipolar Transistors
Resistances
Diodes
Ring Oscillator
Shift Registers
Latch-Up Structures

CHIP#1



CHIP#2

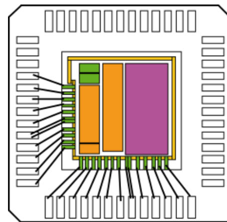


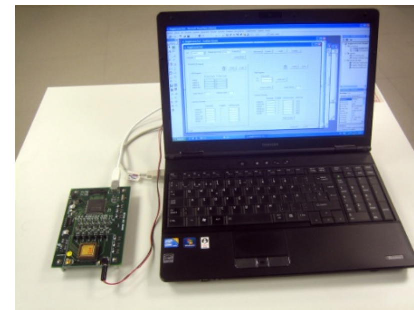


- Geometry
- Temperature
- TID

Library Cells
Shift Registers
Combinational Logic

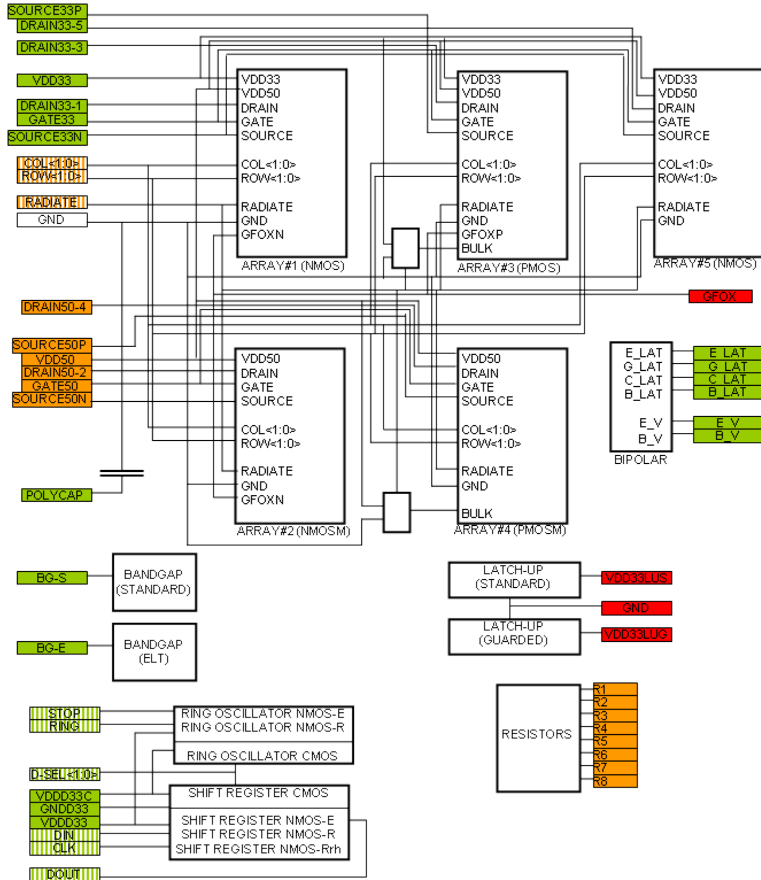
CHIP#3

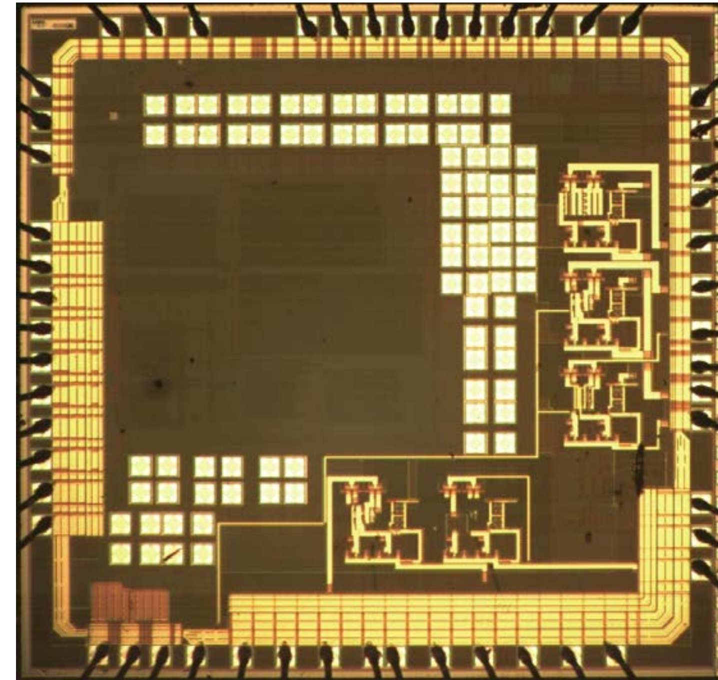




- SEUs & SETs
- Latch-Ups

Test Chips (2) – CHIPS #1 & #2



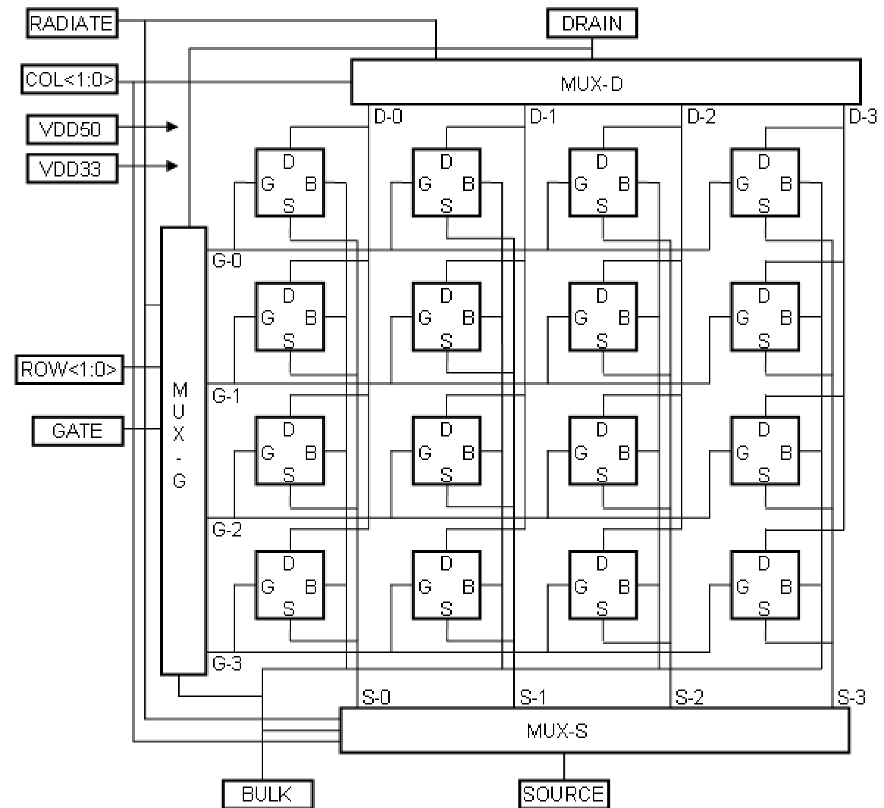


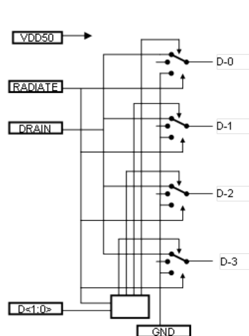
CHIP#1 with five multiplexed arrays of 4 x 4 CMOS transistors

Test Chips (3) – Muxed Arrays

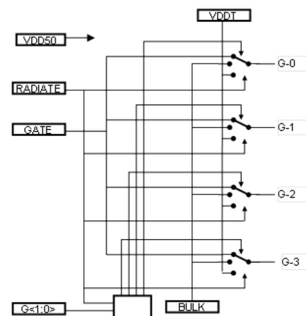
MUX-D connects to DRAIN the drains of all transistors in its column, other columns have its drain open; MUX-S connects to SOURCE the source of all transistors in its column, other columns have its source to BULK; MUX-G connects to GATE the gates of all transistors in its row, other rows have its gate to BULK (GND (NMOS) or to VDD (PMOS)). SOURCE, GATE and DRAIN are connected externally to the measuring equipment.

RADIATE sets all transistors with gate to VDD and all other terminals grounded.



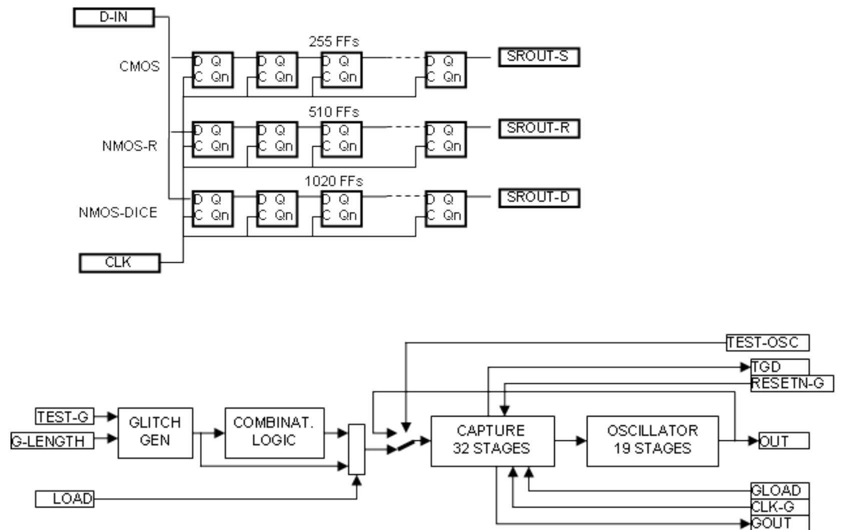


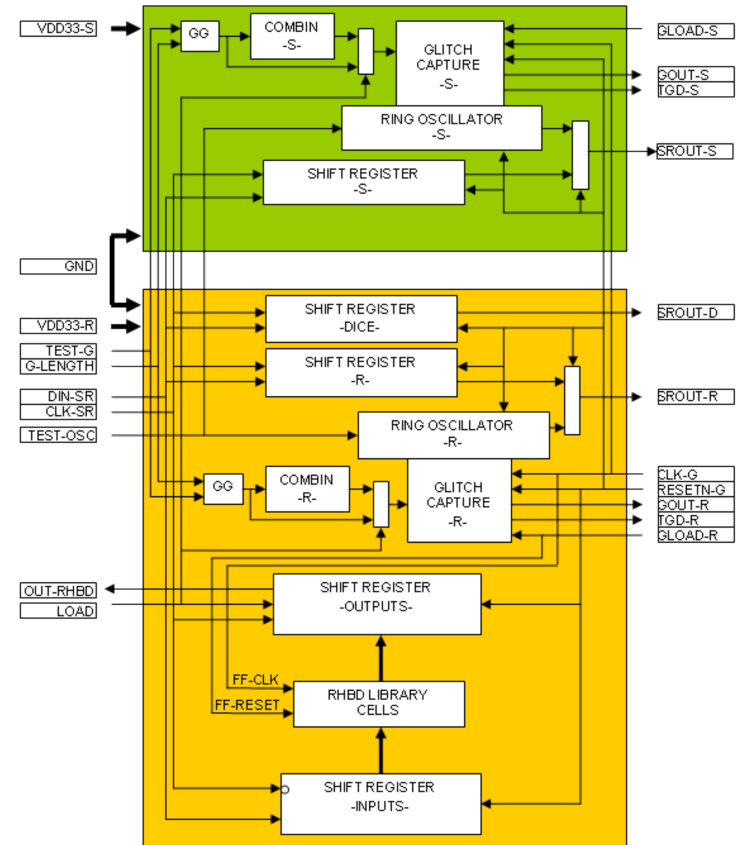
MUX-D



MUX-G

Test Chips (4) – CHIP#3





Dedicated to evaluation of SEU, SET and SEL in standard and RHBD digital cells.

PC

- Programming of configuration register
- Control of HP 4155A (test configuration, execution & data trace)
- Output-data local storage
- Test Automation

Switch Matrix Board

Connects measurement lines and stores the configuration bits for control of DUT.

HP 4155A Semiconductor Parametric Analyzer

- Stimuli generation
- Output data sampling

ASIC board

Placed inside climatic chamber for controlled-temperature tests

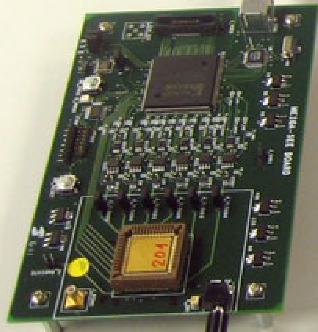
Temperature & TID Characterization Hardware

ASIC board

ADCs to detect and resolve over-current in supply lines due to latch-ups

FPGA monitors SEU, SET & Latch-Up events and resets power lines if neccessary

Monitors up to six different supplies

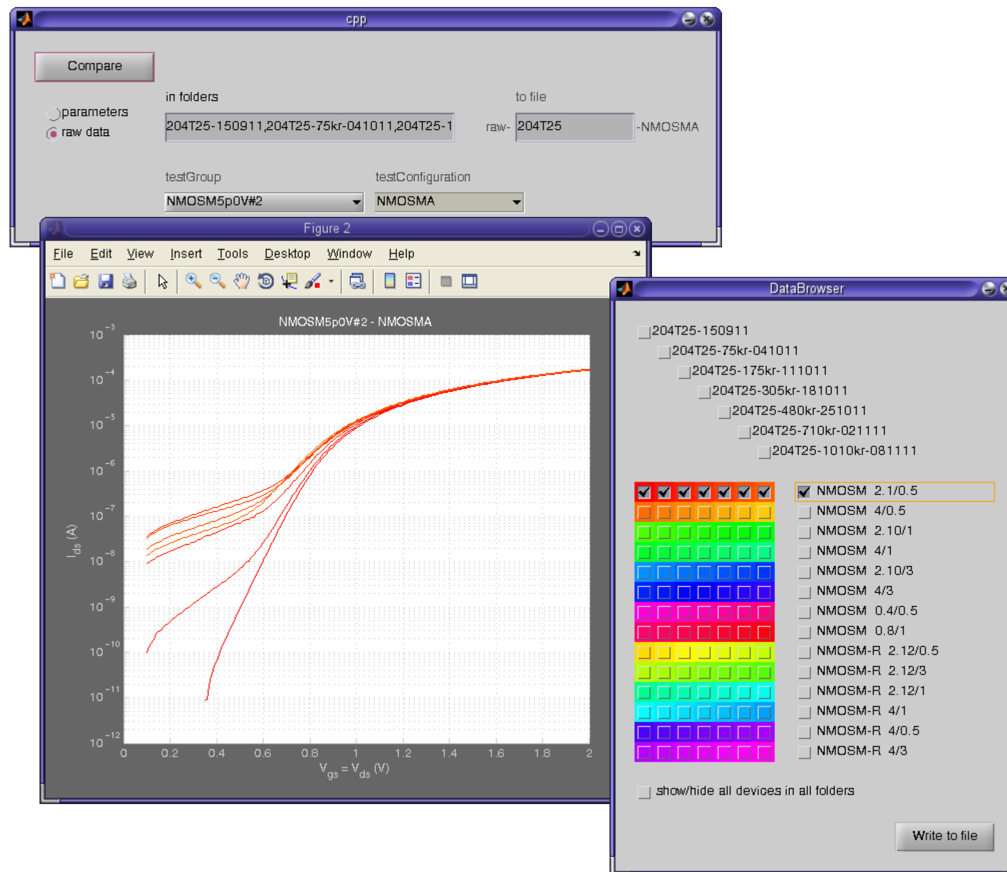


PC

- Periodically reads SEU, SET & Latch-Up totals from the FPGA
- Output-data local storage

SEE Characterization Hardware

Postprocessing Software



MATLAB scripts

Raw data visualization

Parameter extraction

Graphical data comparison among tests performed in different conditions

Export selected data to text files

Data Post-processing

- Raw data is compensated for:
  - Voltage drop in multiplexer switches
  - Body-effect due to increase in source voltage
  - Leakage currents in input pads and multiplexers

CMOS Parameters Extracted:

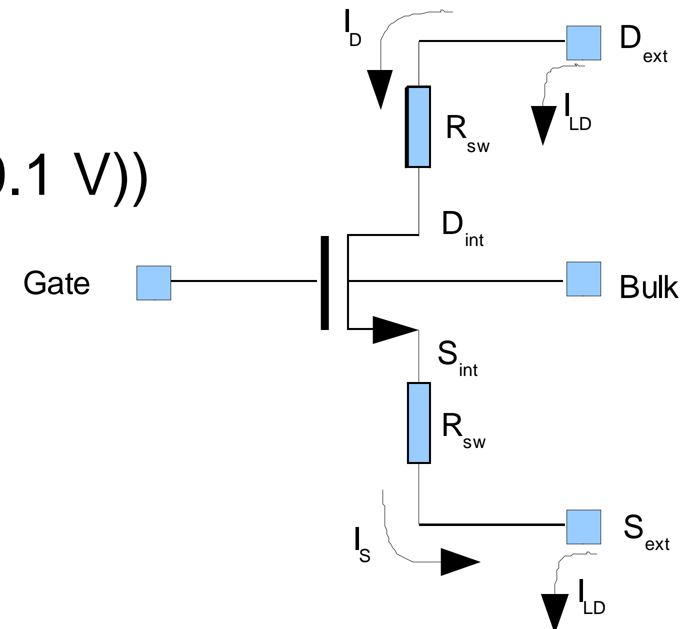
V_{th} (linear (V_{ds}=V_{gs}) and saturation (V_{ds}=0.1 V))

Subthreshold leakage current

Gain Factor (*KP*)

Body effect

Saturation current



Test Facilities

- Low-Temperature
  - Instituto de Microelectrónica de Sevilla
  - Instituto Nacional de Técnica Aeroespacial (INTA)
- TID
  - Laboratorio de Radiofísica – Univ. de Santiago de Compostela
- SEE
  - Centre de Ressources du Cyclotron – Louvain-la-Neuve
  - Centro Nacional de Aceleradores - Sevilla

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Operation at Low Temperature

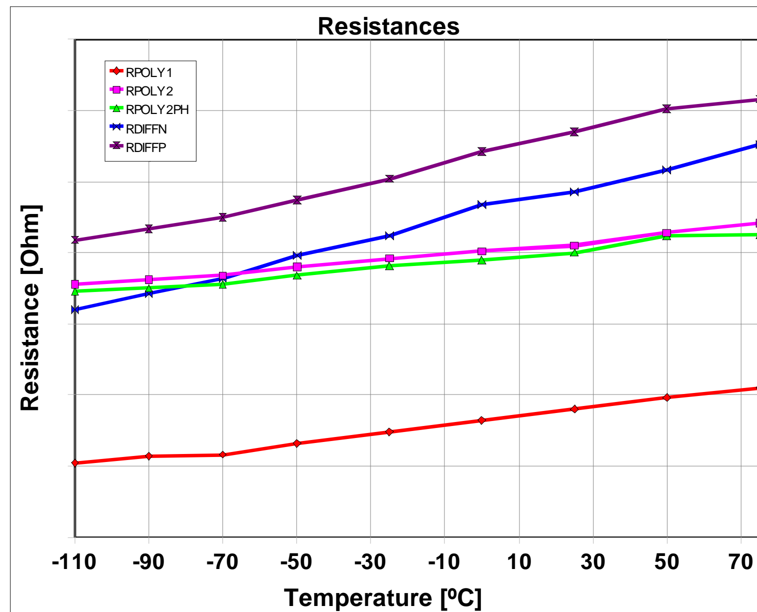
- Instruments located in the outside of the main spacecraft body (masts, booms) have to stand temperatures below the range characterized by the foundries.
  - Alternatives:
    - Heat the ASIC to keep it within the standard temperature range (complex assembly and high power consumption)
    - Characterize the behaviour at lower temperatures, adapt the models if needed, and take extra margins in the design.

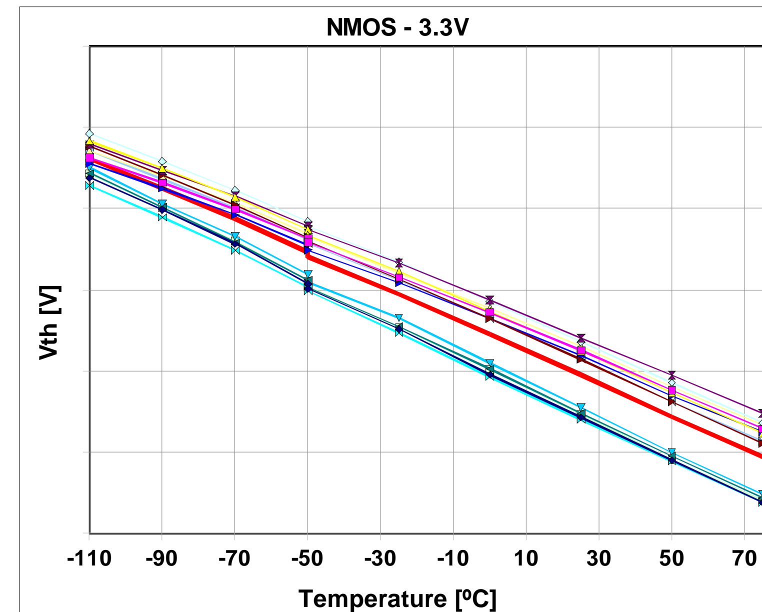
Low Temperature Measurements

- IMSE
  - Down to -55ºC using Thermonics T-2650BV
- INTA
  - Down to -110ºC using SUN Systems liquid N_2 cooled thermal chamber.

Low-Temperature (-110ºC) setup at INTA

Low Temperature Results





Temperature dependence do not show unexpected behaviour beyond the range guaranteed by the foundry (-40ºC)

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Equivalent Width for ELTs

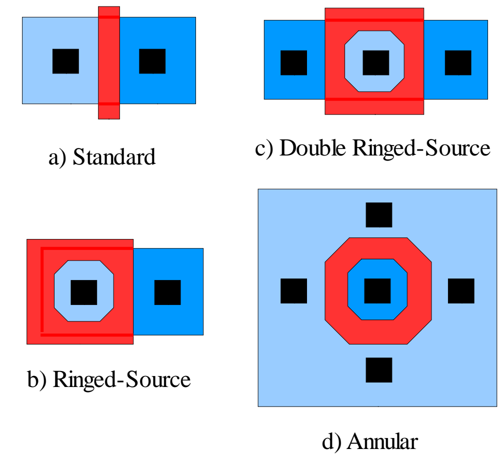
- Accounts for extra S-D current by an effective width W_{eff}
  - For Ringed-Source:

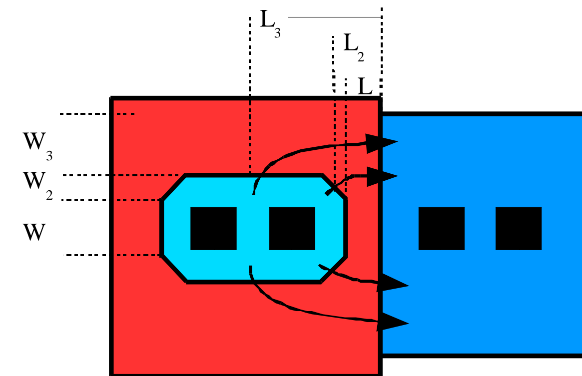
$$W_{eff} = W + 2 \cdot L \cdot \left[\frac{W_2}{L_2} + \left(\frac{2 \cdot n_c + 3}{4} \right) \cdot \frac{W_3}{L_3} \right]$$

  - For Double-Ringed Source:

$$W_{eff} = W + 4 \cdot L \cdot \left[\frac{W_2}{L_2} + \left(\frac{n_c + 5}{6} \right) \cdot \frac{W_3}{L_3} \right]$$

  - Incorporated in transistor models and extraction tools.





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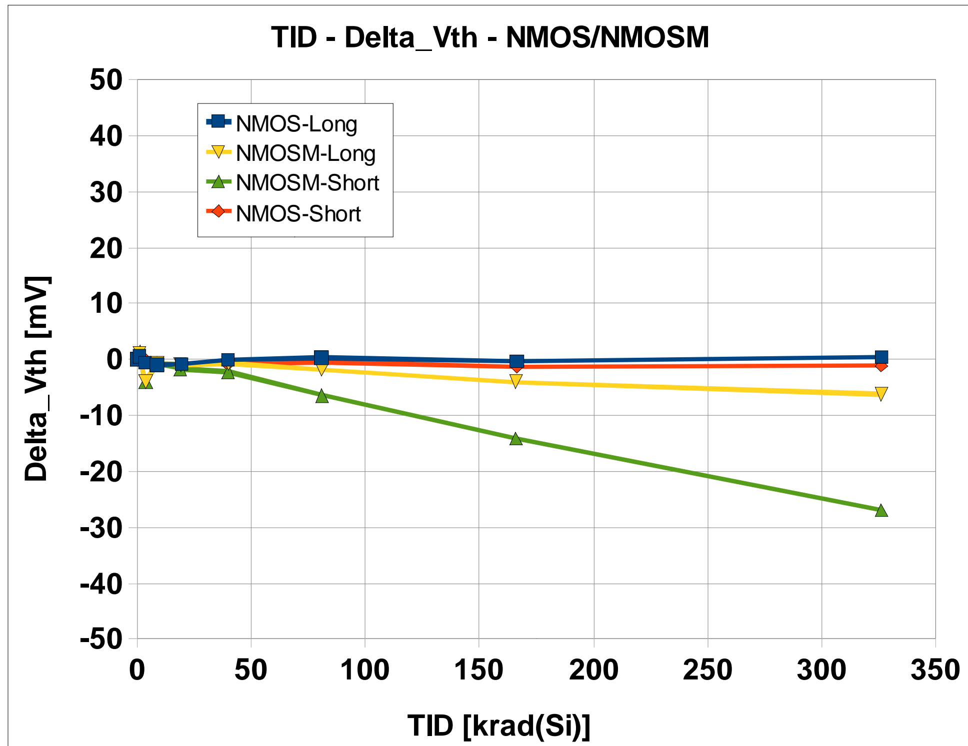
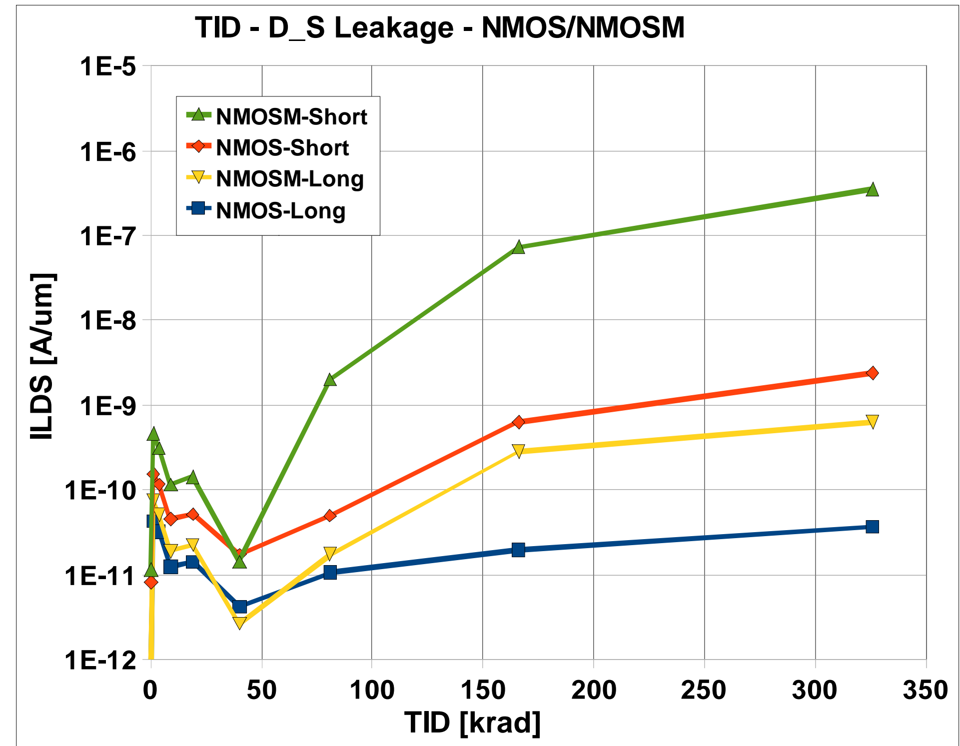
TID Tests

- Three TID Test Campaigns
  - CHIP#1, preliminary test, 1 day, 65 krad(Si)
  - CHIP#1, 4 samples, 9 days, 350 krad(Si)
    - From 0.02 rad/s to 2.5 rad/s, doubling at each step.
    - Annealing 6 weeks @RT, 84 hours @ 100ºC unbiased, 84 hours @ 100ºC biased.
  - CHIP#2, 4 samples, 6 irradiation steps of 42 hours each, reaching 1Mrad(Si) over 6 weeks, with delayed measurements.
    - From 0.5 rad/s to 2 rad/s, increasing by 1.33 at each step.
    - Annealing 16 days @RT -> 95 hours @ 100ºC unbiased -> 73 hours @ 100ºC unbiased.
  - Irradiations performed at Laboratorio de Radiofísica (USC, Spain)

Irradiation CHIP#1 – NMOS/M

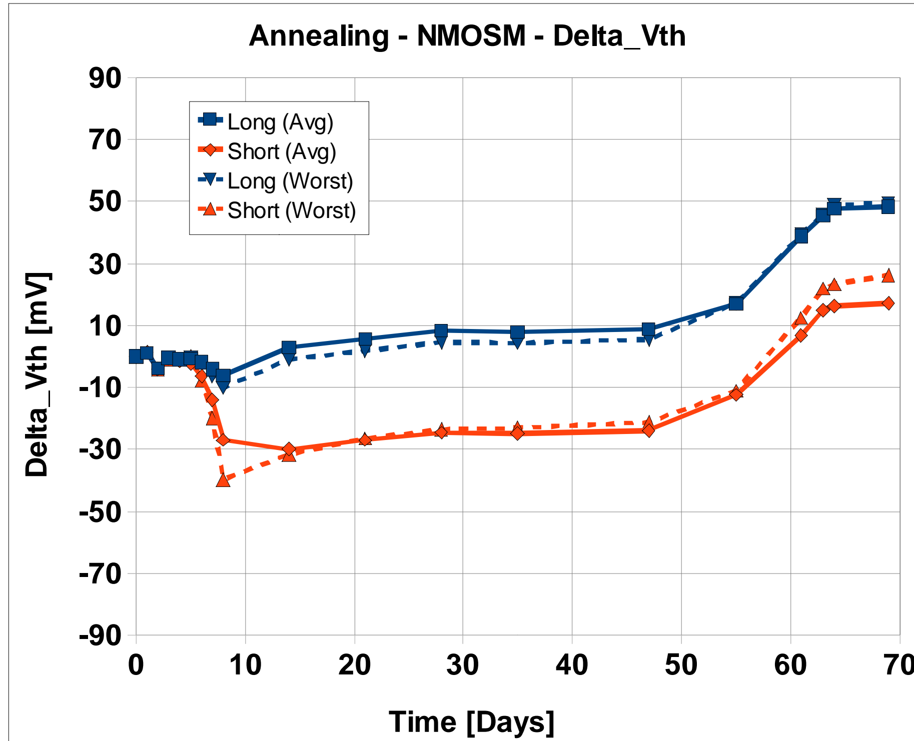


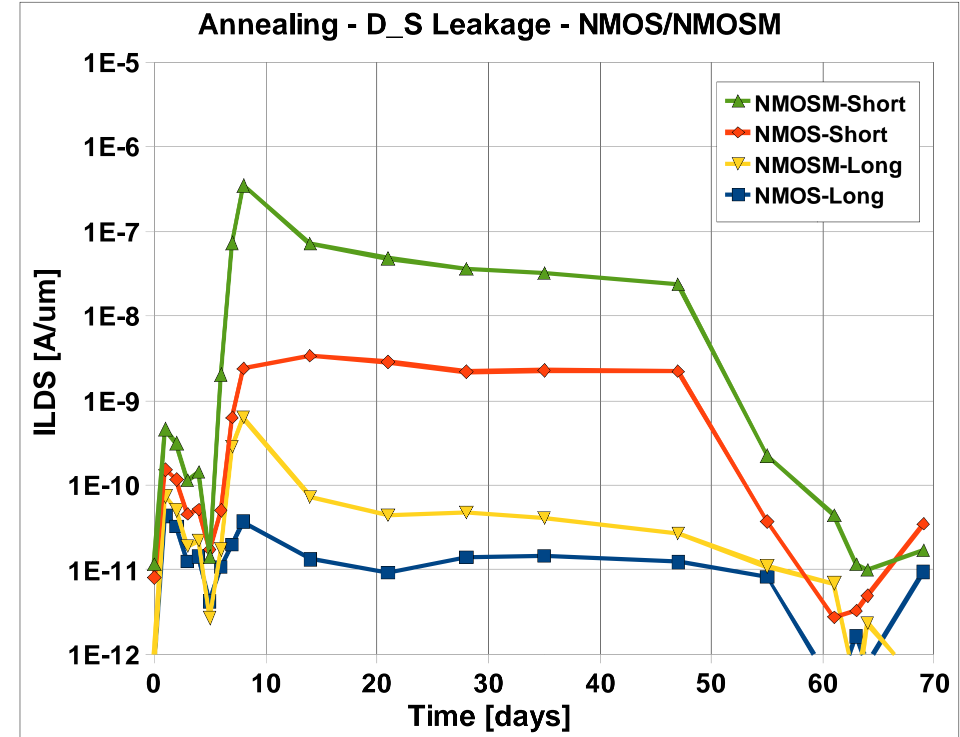


Drift inmediately after irradiation negligible for thin-oxide gates. More significant for thick-oxide with short length

Leakage important for short transistors. Negligible effect for long transistors with thin-oxide.

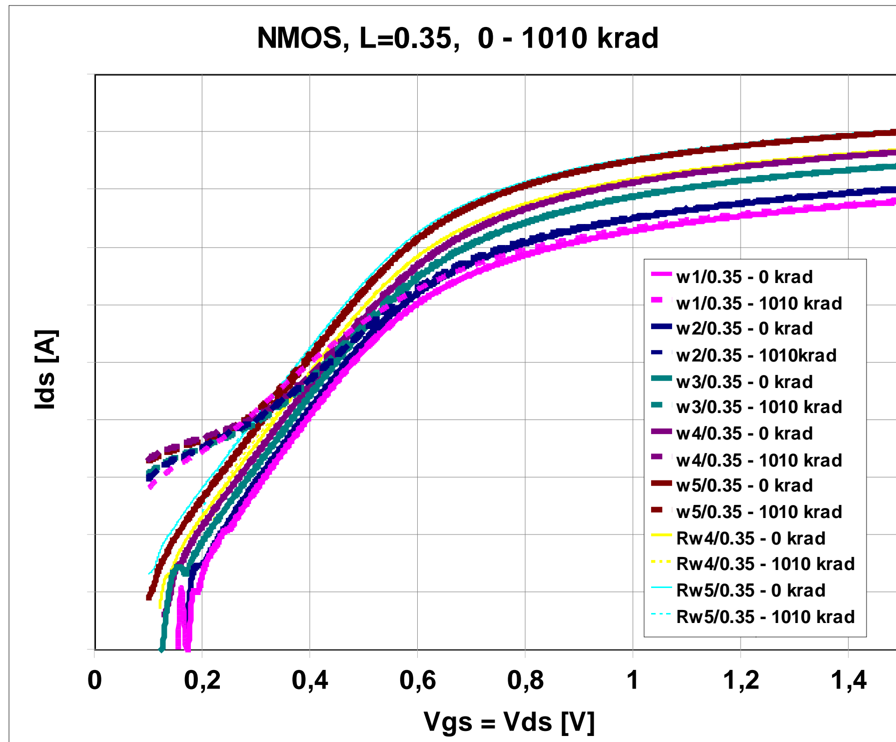
Annealing CHIP#1 – NMOS/M

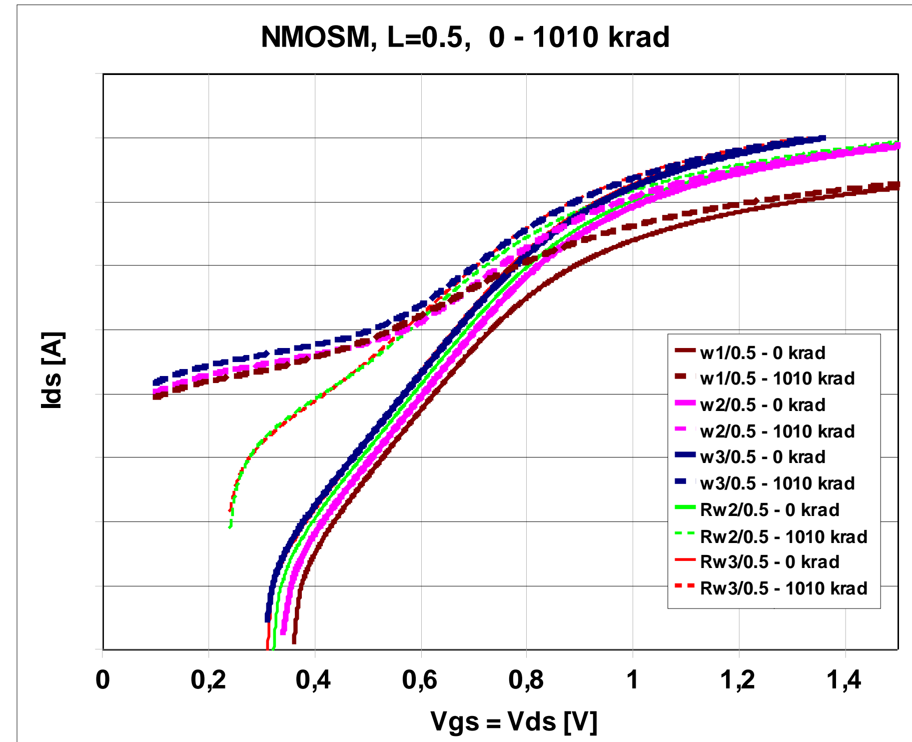




Irradiation: Days 0 to 9 (up to 350 krad(Si))
Annealing: Day 47, 6 wk @ RT; Day 54, 70h @100ºC unbiased, Days 61/ 63/ 64/ 69, after 90/ 112/ 133/ 157 hours @ 100ºC biased

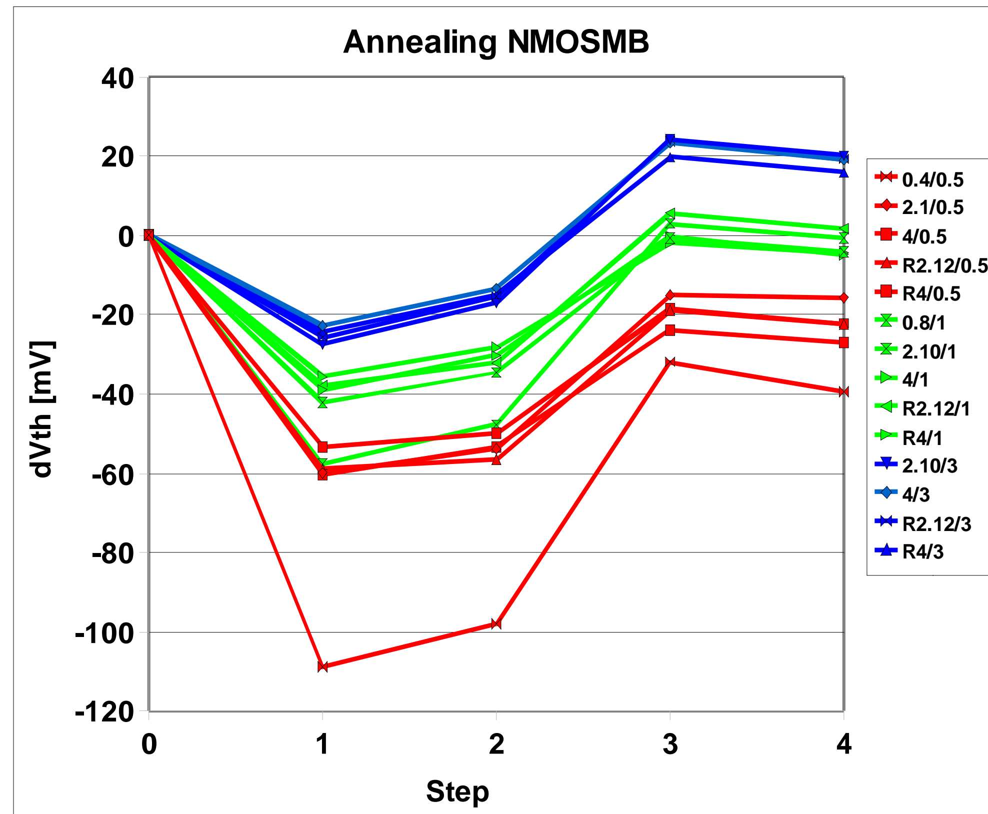
Ids vs. Vgs – NMOS/M (0-1Mrad) – CHIP#2





Irradiation: 6 weekly steps of 42 hours each (up to 350 krad(Si))
Thin-oxide (NMOS): Little effect for standard layout, negligible for ringed layout
Thick-oxide (NMOSM): Increase in zero bias leakage for standard transistors. Increased subthreshold swing in all types.

Dependence on Transistor Dimensions

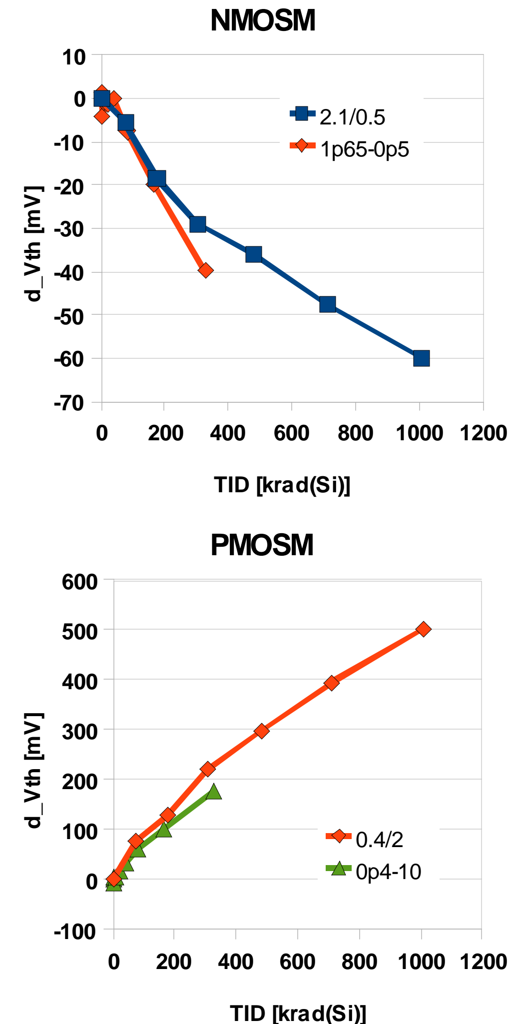


ΔV_{th} for thick-oxide NMOS after: 1) 1 Mrad(Si); 2) 16 days @25ºC; 3) 95 hours @ 100ºC; 4) 168 hours @ 100ºC

Note clustering on transistor length: 0.5µm (red); 1µm (green); 3µm (blue); and stronger effect for narrow transistors

Comparison of Irradiation Campaigns

- Comparison made using transistors of similar dimensions.
  - Upward shift of ΔV_{th} for NMOSM and PMOSM transistors in second TID test (up to 1 Mrad).
  - Probably due to longer time between irradiation steps, combined with faster annealing of oxide charges (N_{ot}) than interface charges (N_{it}).



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SEE Tests

- Eight-hours beam time using Heavy-Ion Cocktail #1 of Cyclone-UCL
  - Normal incidence, room temperature.
  - Measurements on 2 samples

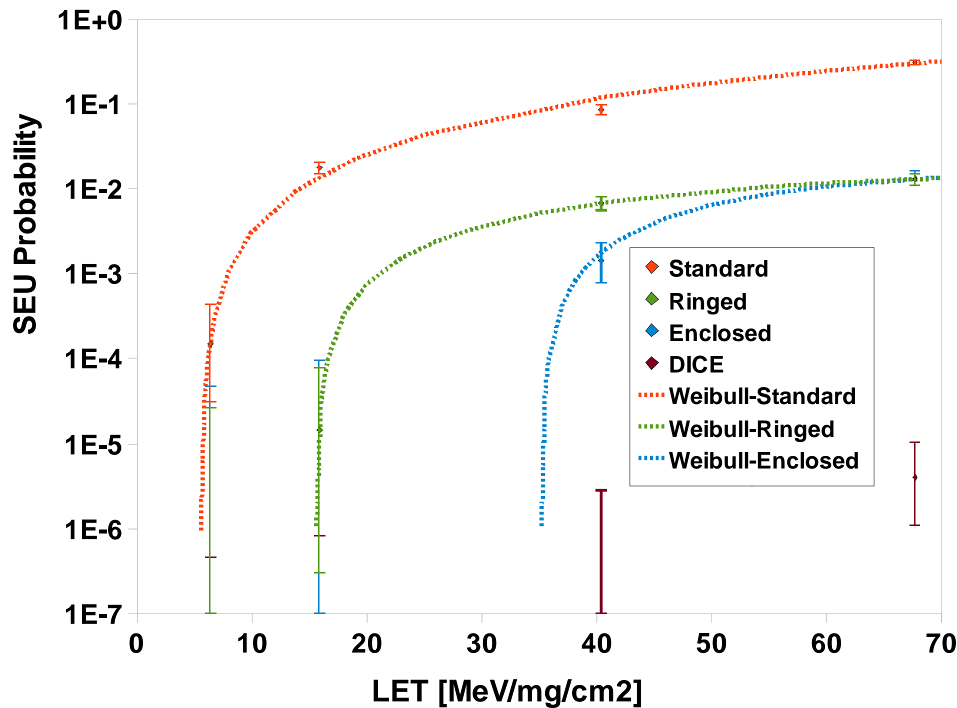
Ion	LET [MeV·cm²/mg]	DUT Energy[MeV]	Range [μm (Si)]
$^{15}N^{3+}$	3.3	60	59
$^{20}Ne^{4+}$	6.4	78	45
$^{40}Ar^{8+}$	15.9	151	40
$^{84}Kr^{17+}$	40.4	305	39
$^{124}Xe^{25+}$	67.7	420	37

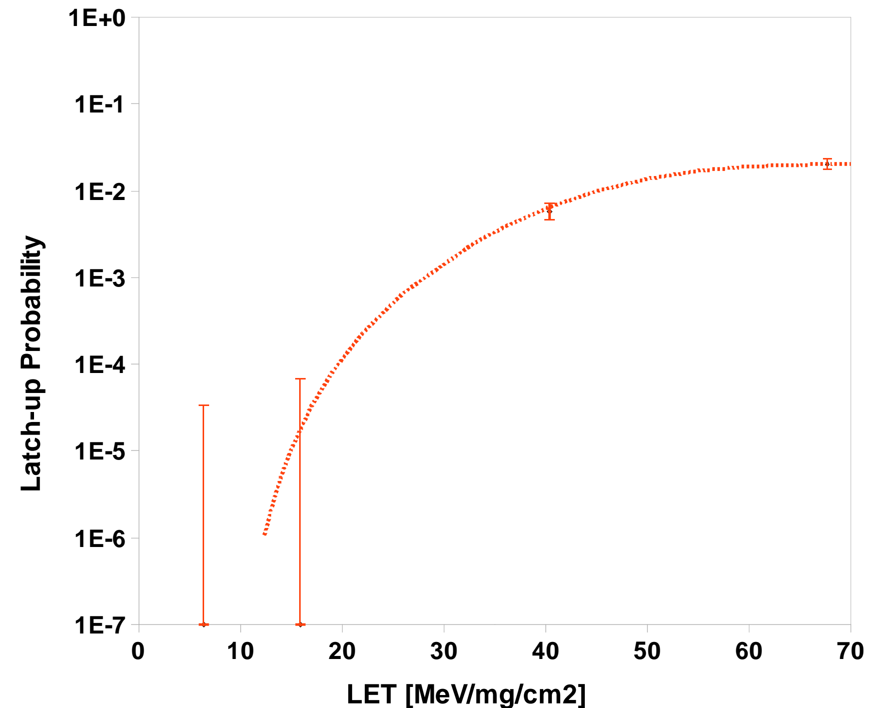
Ion Cocktail #1

LET [MeV·cm²/mg]	Fluence [1/s·cm2]	Standard	Ringed	Enclosed	DICE
6.4	$5.6\cdot10^{7}$	3	0	0	0
15.9	$2.8\cdot10^{7}$	178	1	0	0
40.4	$7.5\cdot10^{6}$	233	127	15	0
67.7	$5.5\cdot10^{6}$	617	179	104	4

SEU Errors

SEU & Latchup Results





SEU *Lth* [MeV·cm²/mg] / σ_{sat} [cm²]

Standard: 5.5 $2.8\cdot10^{-6}$

Ringed: 16.0 $3.3\cdot10^{-7}$

Enclosed: 35.0 $1.0\cdot10^{-7}$

Latch-Up *Lth* [MeV·cm²/mg] / σ_{sat} [cm²]

Standard: 9 $1.1\cdot10^{-5}$

RHBD: > 67.7 ?

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Summary of Tests

- **CHIP#1**
  - Temperature: -50, -25, 0, 25, 50, 75 ºC **@ IMSE**
  - Temperature: -50, -70, -90, -110 ºC **@ INTA**
  - TID: 1.15, 3.7, 8.9, 19.4, 40, 81, 167, 326, 366 krad(Si) **@ USC**
  - SEE: N, Ne, Ar, Kr, Xe **@ UCL**
  - Annealing **@ IMSE**

- **CHIP#2**
  - Temperature / -50, 25, 100 ºC **@ IMSE**
  - TID / 75, 175, 305, 480, 710, 1010 krad(Si) **@ USC**
  - Annealing **@ IMSE**

- **CHIP#3**
  - **SEE: @ UCL** (scheduled for October 2012)

Conclusions

Temperature

Behaviour down to -110ºC in good agreement with the prediction of the standard foundry models.

TID

V_{th} drift low (< 30 mV @ 300 krad(Si)) for thin-oxide transistors.

V_{th} drift moderate (+180mV PMOSM, -30mV NMOSM @ 300 krad(Si)) for thick-oxide transistors

Ringed-source layout is effective in reduction of TID induced S-D leakage in NMOS.

SEE

SEU L_{th} [MeV·cm^2/mg]: 5.5 (standard); 16 (ringed-source); > 68 (DICE)

Latch-Up L_{th} [MeV·cm^2/mg]: 9 (standard); > 68 (RHBD layout)

Future Work

- RHBD Digital Library
  - Perform SEE Tests
  - Improve cell layout and add more cell types
- Analog
  - Model dependence of V_{th} with radiation and transistor dimensions
  - Characterize bipolar devices for displacement damage using proton source at CNA

Thank you for your attention!