View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Digital.CSIC

Evaluation of RTD-CMOS Logic Gates

Juan Núñez, María J. Avedillo and José M. Quintana.
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas (CSIC) and Universidad de Sevilla
Américo Vespucio s/n, 41092-Sevilla, SPAIN
FAX: +34-954466666, E-mail: {jnunez, avedillo, josem}@imse.cnm.es

***Abstract*— The incorporation of Resonant Tunnel Diodes (RTDs) into III/V transistor technologies has shown an improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption. Currently, the incorporation of these devices into CMOS technologies (RTD-CMOS) is an area of active research. Although some works have focused the evaluation of the advantages of this incorporation, additional work in this direction is required. This paper compares RTD-CMOS and pure CMOS realizations of a set of logic gates which can be operated in a gate-level nanopipelined fashion, thus allows estimating logic networks operating frequency. Lower power-delay products are obtained for RTD/CMOS implementations.**

I. INTRODUCTION

Resonant tunneling devices (RTDs) are nowadays considered the most mature type of quantum-effect devices. They are already operating at room temperature and they exhibit very attractive characteristics as high-speed operation and low power consumption. RTDs are very fast non linear circuit elements which have been integrated with transistors to create novel quantum devices and circuits. This incorporation of tunnel diodes into III/V transistor technologies has shown an improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption [1], [2], [3].

The degree of development of resonant tunneling devices is very different. RTDs fabricated in III-V are, undoubtedly, the most mature and most reported circuits based on resonant tunneling use them combined with different types of transistors. Since the currently dominant technologies use silicon, plenty of efforts have been devoted to develop devices with negative resistance in this material. The resulting diodes have provided worse performance than those achieved in III-V technologies. Currently, the realization of tunnel diodes in silicon is a very active research area where progress are expected. In fact, it has been suggested that the addition of RTDs to CMOS technology could extend its life and even make investments worthwhile. It has been shown the integration of Resonant Interband Tunneling Diodes (RITDs) with standard CMOS [4] and SiGe HBT [5], and even its MOBILE operation. It has been also reported a RITD with a cutoff frequency of 20GHz, allowing for the first time, applications of mixed signal, RF and high speed logic circuits [6]. Simpler and compatible with CMOS process to fabricate Tunneling Diodes have been recently reported: structures that do not need Ge are decribed in [7], and in [8] a fabrication process based on CVD (Chemical Vapor Deposition) instead of MBE (Molecular Beam Epitaxy) is presented.

Another explored option is the development of procedures for III-V RTDs compatible with silicon substrates. Recently importance advances have been achieved in this area, such us the Tunneling Diodes in III-V materials and Ge using ART (Aspect Ratio Trapping) [9], [10].

Some works have focused the evaluation of the advantages of incorporating RTDs to CMOS technologies. In [11], the keeper transistor of the domino logic gates is replaced by an RTD, which significantly increases the noise immunity without affecting the area, delay and power consumption. A static memory cell is described in [12], consisting of the incorporation of a well-known DRAM cell topology with a pair of RTDs. This structure improves the performance of a typical 6-transistors SRAM cell in terms of the static power consumption in three orders of magnitude.

However, in our opinion, additional work in this direction is required. In particular, in the field of logic circuits, estimations of performance/count devices improvements obtained through the addition of RTDs have been evaluated for a set of logic functionalities (combinational gates and flip-flops) [13], [14], [15], but without taking into account their usage in gate networks. This is a key point, because as it will be explained in next section, RTD logic gates allow the implementation of a pipeline at the gate level. That is, each gate is a pipeline stage and thus it should be compare to CMOS logic styles operating in a similar way. Moreover, up to our knowledge there is a lack of recent studies in this area and as a consequence no data involving current technologies are available. This paper addresses these issues and contributes to provide results on how RTD-CMOS

realizations compare to pure CMOS gate-level pipelined ones when implemented in a commercial 130n*m* technology.

The paper is organised as follows: in Section II, RTD based logic gates working on the basis of the MOnostable to BIstable operating principle are described. In Section III, we present the set of logic gates that has been designed and evaluated. A comparison in terms of the power-delay product with the CMOS TSPC realizations of these structures is described in Section IV. Finally, some conclusions are given in Section V.

II. RTD BASED MOBILE LOGIC GATES

Logic circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) which exploits the negative differential resistance of their *I-V* characteristic (Figure 1*a*). The MOBILE [1] (Figure 1*b*) is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage . When V_{bias} is low, both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state). Output is high if the driver RTD is the one which switches and it is low if the load switches. When the load switches (the output goes to low or "0") and if otherwise when the driver switches (the output goes to high or "1"). Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration for an inverter MOBILE shown in Figure 1*c*, the peak current of the driver RTD can be modulated using the external input signal. RTD peak currents are selected such that the value of the output depends on whether the external input signal is "1" or "0". Assuming the same peak current density, j_p, for all the RTDs, the peak current is proportional to their area. For V_{bias} high, the output node maintains its value even if the input changes. That is, this circuit structure is self-latching allowing to implement pipeline at the gate level.

This circuit topology has been extended to systematically implement threshold gates. A threshold gate (TG) is defined as a logic gate with *n* binary input variables, x_i (i=1, …,*n*), one binary output *y*, and for which there is a set of (*n*+1) real numbers: threshold *T* and weights w_i, such that its input–output relationship is defined as:

$$F(x_1,\ldots,x_n) = \begin{cases} 1 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i \geq T \\ 0 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i < T \end{cases} \qquad (1)$$

Figure 1*d* shows the RTD/HFET implementation of a generic threshold gate [16] defined as $y=1$ *iff* $w_1x_1+w_2x_2-w_3x_3-w_4x_4 \geq T$, and *0* otherwise. The RTD peak currents determine the weights and the threshold *T*. Input stages controlled by

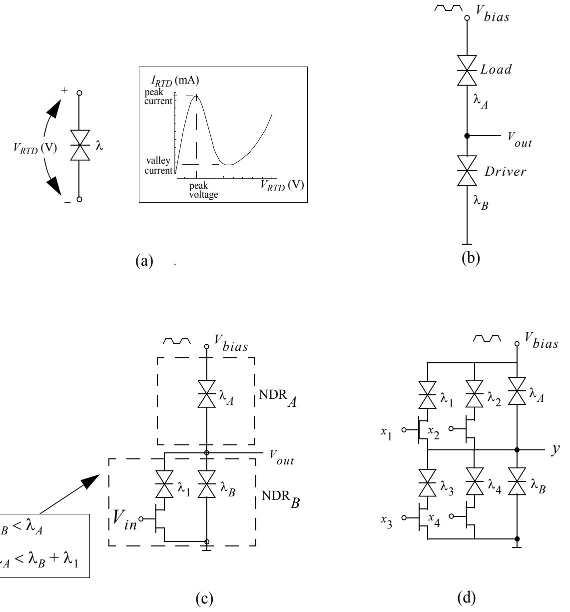


Figure 1. RTD MOBILE circuits. a) RTD *I-V* characteristic. b) Basic MOBILE c) MOBILE inverter.d) MOBILE TG.

external inputs are placed in parallel to driver or load RTDs depending on whether the associated weight is positive or negative, allowing the control of the peak currents of both.

III. DESIGN OF RTD-CMOS THRESHOLD LOGIC GATES

To illustrate the design of threshold logic gates using RTD-CMOS we have chosen four typical gates: binary inverter, NAND, NOR and inverted majority (NMAJ) gates.

The equation of the binary inverter can be written in terms of (1) considering that w_1=-1 and *T*=0. The circuit diagram is shown in Fig. 2*a*, where f_x represents the area factor of the driver and the input-stage RTD. The load RTD has been sized 1.5 times larger than the driver RTD has, so that a correct operation can be achieved.

An *n*-input NOR gate corresponds to a TG in which w_i=-1 and *T*=0. Since the weights associated to each input-stage are the same, it is possible to group them using one RTD and *n* NMOS switch transistors, as shown in Fig. 2*b*.

In the *n*-input NAND gate, the weights are equal to -1 and the threshold, *T*=1-*n*. The functional part of this gate is obtained by connecting *n* switch transistors in series (only when all inputs are equal to logic level '1', the functional branch will be triggered). Figure 2*c* shows the circuit diagram of this TG.

The inverted majority gate of *n* inputs (*n* is odd), $NMAJ_n$, can be written in terms of Eq. 1 as follows:

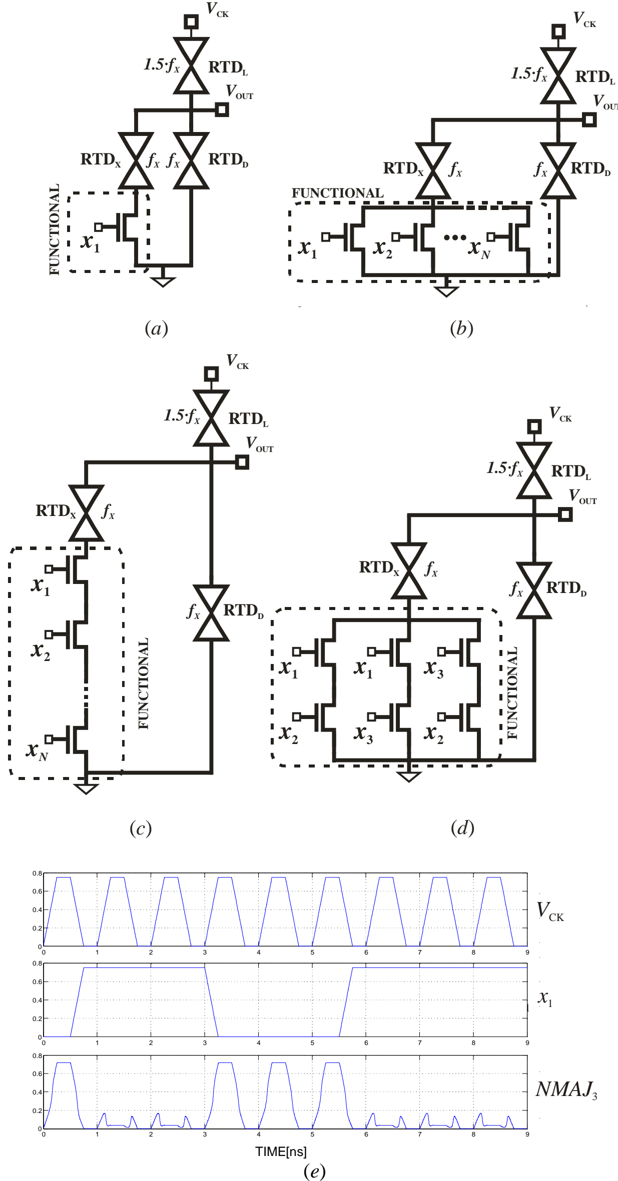


Figure 2. RTD-based circuit diagrams (*a*) Binary inverter (*b*) *n*-input NOR gate (*c*) *n*-input NAND gate (*d*) $NMAJ_3$ (e) $NMAJ_3$ simulation results.

$$NMAJ_n(x_1,\ldots,x_n) = \begin{cases} 1 \;\; iff \;\; \sum_{i=1}^{n} x_i < \lceil n/2 \rceil \\ 0 \;\; iff \;\; \sum_{i=1}^{n} x_i \geq \lceil n/2 \rceil \end{cases} \quad (2)$$

The operation of an RTD-CMOS $NMAJ_3$ gate is shown in Fig. 2*e*. In this experiment, x_2 and x_3 are equal to '0' and '1', respectively, and x_1 switches from '0' to '1'. The output, $NMAJ_3$, only goes down to level '0' when x_1 and x_3 are equal to '1'. Note that the output goes to low (reset) with the falling edge of the clocked bias.

Cascaded MOBILE gates can be operated in a pipelined fashion using a four phase overlapping clocking scheme. Second stage evaluates ($V_{ck,2}$ rising) while the first stage ($V_{ck,1}$) is in the hold phase ($V_{ck,1}$ high). Because of self-latching behavior, second stage is not affected by the reset of the first one. For a number of logic levels greater than three, four bias signals are required. It has been demonstrated that a network of MOBILE-based gates can be operated with a single clocked bias signal [17]. To achieve this operation, positive edge triggered (PET) gates and negative edge triggered (NET) gates are alternated and latches are added. In summary, each gate in a network constitutes a pipeline stage. A gate-level pipeline is implemented. In other words, network operation speed is independent of logic depth but is determined by the clock frequency at which single gates can be operated.

IV. Performance Measuring

The performance of several gates implemented with RTDs and commercial transistors has been compared with True Single Phase Clock (TSPC) CMOS realizations, since they also implement gate-level pipeline. For detailed functional description of TSPC refer to [18].

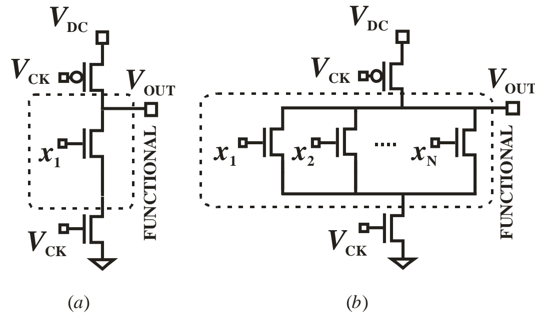
A. True Single Phase Clock Realizations

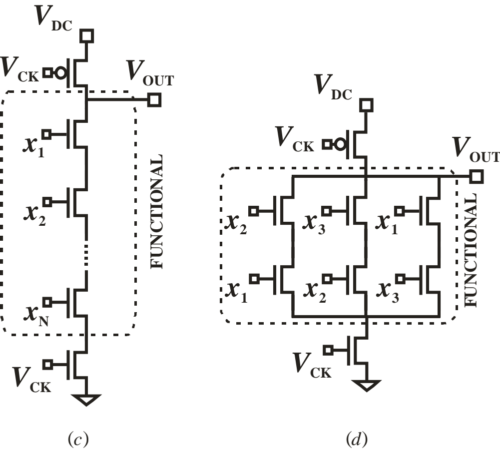
TSPC Network structures are based on the connection of *N*-type and *P*-type dynamic logic gates, placing latches between them. Figures 3*a*-3*d* depict the schematic diagram of a *N*-type realization of the binary inverter, the *n*-input NOR, the *n*-input NAND and the $NMAJ_3$ gates, where the marked area represents its functional part.

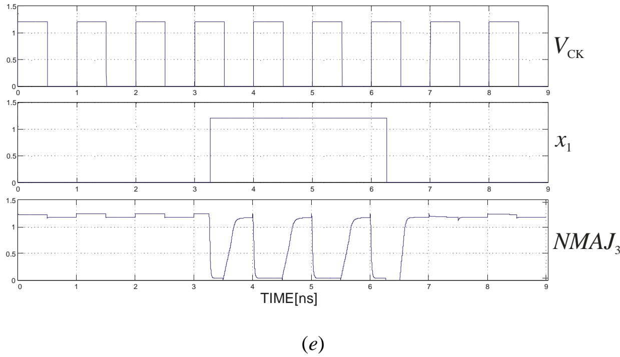
The *N*-type structures preload the output voltage, V_{OUT}, to V_{DC} when the clock voltage, V_{CK}, is low and evaluates when V_{CK}, is high. Figure 4*e* shows the waveforms associated to an $NMAJ_3$ gate test bench, where x_2 and x_3 are equal to '0' and '1', respectively, and x_1 switches from '0' to '1'.

B. Simulation set up

HSPICE© parametric simulations of the RTD-based and the TSPC gates have been carried out in order to explore their performance. For both structures, we have varied a set of some key parameters, taking a discrete number of samples of each one in a given range. We have simulated the structures obtained after combining all the feasible values of the parameters. An automatic verification tool based on Matlab© has been developed to process the results provided by HSPICE© and determine which sets of parameters give structures that operate correctly. We have considered the *power-delay product* (PDP) as the figure of merit that will determine the efficiency of each design. The PDP is defined as the ratio between the average power consumption, P_{AV}, and







(e)

Figure 3. N-type TSPC circuit diagrams (*a*) Binary inverter (*b*) *n*-input NOR gate (*c*) *n*-input NAND gate (*d*) $NMAJ_3$ (e) $NMAJ_3$ simulation results.

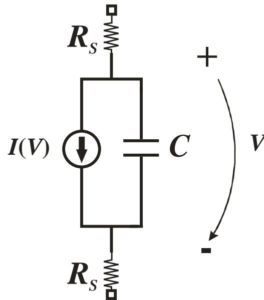


Figure 4. Model of the RTD.

the operation frequency in which it has been measured, $f_{PDP,MIN}$.

We have taken a discrete set of parameters for both structures according to the description given below.

a) RTD-based circuits: For this structures, we have varied the operation frequency and the area factor of the RTD, f_x. Since standard process models for the NMOS transistors and LOCOM models for the RTDs are used, an agreement between their areas is neccesary in order to verify that the order of magnitude of the current associated to both devices are similar. For our analysis, we have considered variations of operation frequency from 1/(3.5·*FO4*) to 1/*FO*4, where *FO4* is the FO4-inverter delay of the technology. The values of f_x between have been varied from 0.01 and 0.04, where the mimimum area factor of the RTDs gives a peak current equal to 20.96μA. Minimum gate-length transistor have been used and transistor widths have been set to the minimum value associated to the technology (0.16μm) since the current level supplied is larger enough to allow the operation of the transistor as a switch for the analyzed values of f_x.

b) TSPC circuits: We have varied the operation frequency and the widths of the MOS transistors, *W*. Minimum gate-length transistor are also used These structures have been sized considering that the PMOS transistor width is $K·W$ (K=3.5 for this technology), and when *N* NMOS transistors are connected in series their widths are set to $N·W$ (*W* has been varied from 0.16μm to 3.2μm). The operation frequency has been changed also from 1/(3.5·*FO4*) to 1/*FO4*.

Now we will describe the comparison and simulation conditions that we will use.

1) Technologhy choice: Simulations results are given for an standard 0.13μm CMOS process. For the RTDs we have used models from LOCOM[19]. The model of the RTD used for simulation is depicted in Fig. 4. Each RTD is modeled by its intrinsic capacitor and resistance, and a paralell-connected voltage controlled current source that represents the *I-V* characteristic of the RTD.

2) Power supply scaling: Power supply has been independtly scaled for the RTD-based circuits and the TSPC structures. We have considered a supply voltage of 1.2*V* for the TSPC structures since it is the standard voltage value of the technology. For the RTD-based structure, a supply voltage of 0.75*V* has been used, which better suits the available RTD *I-V* characteristic.

TABLE I. TSPC CIRCUITS SIMULATION RESULTS

TSPC	One latch load		Two latches load		Three latches load	
	PDP$_{min}$ (fJ)	f_{NORM}	PDP$_{min}$ (fJ)	f_{NORM}	PDP$_{min}$ (fJ)	f_{NORM}
INVERTER	2.05	0.58	2.89	0.43	3.90	0.31
NAND-2	3.01	0.43	4.02	0.31	5.66	0.34
NOR-2	2.35	0.55	3.22	0.40	4.15	0.31
NOR-3	2.72	0.49	3.59	0.37	4.59	0.28
NOR-4	3.12	0.43	3.94	0.34	4.80	0.28
NMAJ-3	4.40	0.34	5.37	0.28	7.91	0.28

TABLE II. RTD-BASED CIRCUITS SIMULATION RESULTS

RTD	One latch load		Two latches load		Three latches load	
	PDP$_{min}$ (fJ)	f_{NORM}	PDP$_{min}$ (fJ)	f_{NORM}	PDP$_{min}$ (fJ)	f_{NORM}
INVERTER	0.85	0.5	1.56	0.32	2.27	0.26
NAND-2	1.01	0.5	1.71	0.28	2.33	0.25
NOR-2	0.92	0.39	1.15	0.39	2.11	0.27
NOR-3	1.04	0.36	1.65	0.28	2.24	0.20
NOR-4	1.18	0.40	1.80	0.24	2.29	0.23
NMAJ-3	1.44	0.34	2.03	0.39	2.71	0.25

3) Fan-out load: For all the structures, we have considered that they have been loaded with one, two and three minimum-sized *N*-type TSPC latches.

4) Mismatch: Standard mismatch models from the technology have been used with the MOS transistors. Since there are no mismatch models available for the LOCOM technology and no information about variability, a set of critical parameters has been chosen and associated to gaussian distributions (for each device). Particulary, we have considered the peak voltage and the area of the RTD. The absolute error, modelled for each parameter and device is determined by a relative error, *E*, and its size. The absolute error of the areas of the RTDs is given by $aer = E \cdot A_{\min} \cdot \sqrt{A_{\min} / A}$, where *A* is the area of the RTD (A_{min} is the minimum feasible area of the RTD). On the other side, the absolute error of the peak voltages is given by $aev = E \cdot V_p$.

C. Simulation results

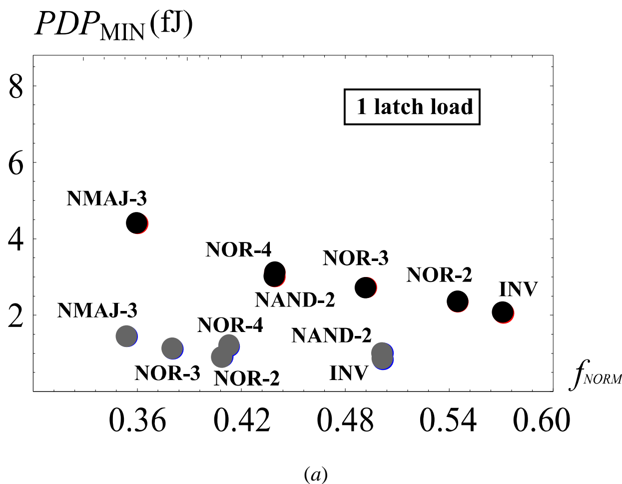
Tables I and II depicts the performance (PDP and operating frequency) of the structures exhibiting the smallest PDP among those that have been simulated in the design space exploration experiment above described. Results for the inverter, two-input NAND gate; two, three and four input NOR gates and the three-input inverted majority gate, with the three load conditions analyzed are shown The operation frequency is given in terms of the FO4-inverter delay of the technology, $f_{NORM}= FO4 \cdot f_{PDP,MIN,}$. These results have been plotted in Figure 5, where the gray and black points represent the PDP RTD-based and TSPC structures, respectively. From these figures, it can be clearly observed that the proposed RTD-based gates improve the PDP performance over the TSPC designs. Gray points are in all cases well under the black ones. In addition, PDP of TSPC structures increases more with gate functionality than RTD ones.

Note that there are some results that require additional comments since they might seem "rare". First, simpler gates do not always exhibit the highest frequency (for example INV and NMAJ-3 using RTDs and fanout two, or INV and NAND-2 using TSPC and fanout three). Secondly, there are significant differences between the relative performances (in terms of the operation frequency) when we change the output load. For instance, when the RTD-based structures are charged by one latch, the NMAJ$_{-3}$ gate frequency is lower than the other gates. On the contrary, when the structure is loaded by two latches the NMAJ$_3$ gate works at the highest frequency. Note that in the experiment carried out, for each gate, a set of differently sized structures are evaluated at several frequencies. Among the working ones, the one with the smallest PDP has been selected and represented in the frequency-PDP design evaluation space. That is, it should not be interpreted that the maximum operating frequency but the one at which the minimum PDP is achieved is being represented. In other words, RTD-NMAJ$_{-3}$ gate with fan out 2 needs to operate at higher frequencies than the other RTD-gates to have a minimum PDP.

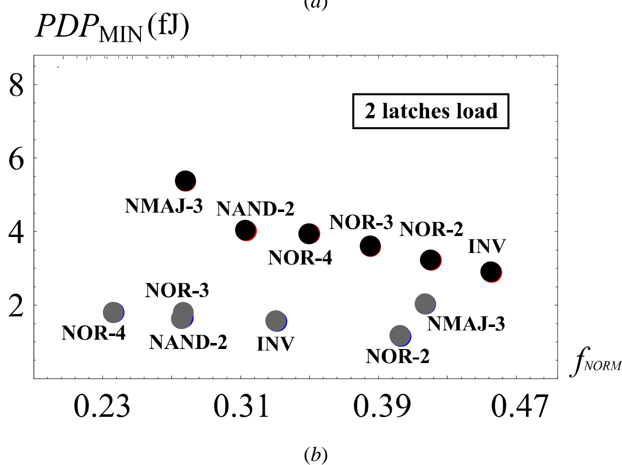
The efficiency of the RTD-CMOS structures over the TSPC designs is shown in Table III. We have measured the PDP of the RTD-CMOS circuits at their maximum operation frequency. If we compare these results with the ones given in Table I, we can conclude that even for higher operation frequencies, the RTD-CMOS structures are more efficient in terms of the PDP than the TSPC circuits. Figure 6 depicts the PDP vs frequency representation for the RTD-CMOS structures (in gray) and the TSPC circuits (in black), when they are loaded with a single *N*-type latch.

TABLE III. RTD-BASED CIRCUITS SIMULATION RESULTS

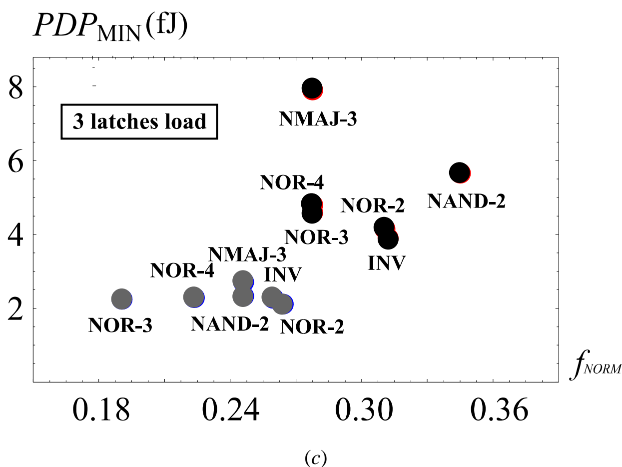
RTD	One latch load		Two latches load		Three latches load	
	PDP$_{min}$ (fJ)	$f_{MAX,NORM}$	PDP$_{min}$ (fJ)	$f_{MAX,NORM}$	PDP$_{min}$ (fJ)	$f_{MAX,NORM}$
INVERTER	0.88	0.76	1.72	0.48	2.38	0.33
NAND-2	1.01	0.50	1.78	0.39	2.37	0.33
NOR-2	0.94	0.51	1.68	0.47	2.28	0.33
NOR-3	0.83	0.56	1.67	0.47	2.26	0.33
NOR-4	1.28	0.57	1.96	0.39	2.51	0.29
NMAJ-3	1.41	0.52	2.08	0.39	2.73	0.29



(*a*)



(*b*)



(*c*)

Figure 5. Minimum PDP vs frequency representation for the proposed structures (RTD-CMOS in gray and TSPC in black) when they are loaded with (*a*) one minimum TSPC latch, (*b*) two minimum TSPC latches and (*c*) three minimum TSPC latches .

We have also verified that setting up the power supply voltage of the TSPC structures to 0.75*V* causes a marked reduction of the maximum operating frequency without improving the PDP performance with regard to the RTD-based structure.

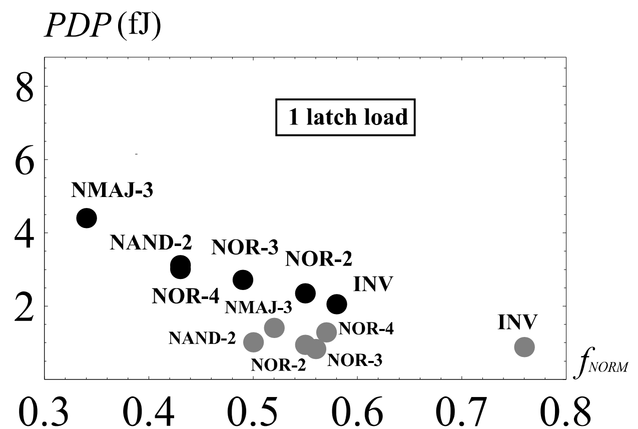


Figure 6. PDP vs frequency plot for the TSPC (in black) and RTD-CMOS (in gray) loaded with one *N*-type latch.

Mismatch analyses (3-sigma) have been performed to check the robustness of the design. We have verified the correct operation of the structures with relative errors on the mismatch model of the RTD up to 8%.

V. Conclusions

Realizations of RTD-CMOS logic gates working of the basis of the MOBILE operating principle have been introduced. A comparison to only transistor implementations using TSPC logic style, well suitable for gate level pipelined like the proposed RTD structures, has been carried out. An experiment of design space exploration has been described which shows the efficiency of the RTD-CMOS design over the CMOS TSPC structures in terms of PDP.

Acknowledgment

This work has been funded by the Spanish Government under project NDR, TEC2007-67245/MIC, and the Junta de Andalucía through the Proyecto de Excelencia TIC-2961.

References

[1] Mazumder, P. et al., “Digital circuit applications of resonant tunnelling devices”, *Proc. IEEE*, 86, Apr. 1998, pp. 664-686.

[2] Maezawa, K.S., Kishimoto, H., Mizutani, T., "100 GHz Operation of a Resonant Tunneling Logic Gate MOBILE Having a Symmetric Configuration". *Proc. Int. Conf. on Indium Phosphide and Related Materials*, pp. 46-49, 2006.

[3] Choi S., Jeong Y., Lee J., and Yang K., “A Novel High-Speed Multiplexing IC Based on Resonant Tunneling Diodes” Accepted for publication in IEEE Trans. on nanotechnology, already available on-line.

[4] S. V. Sudirgo, R. Nandgaonkar, R.P. Hirschman, S. Rommel, S. K. Kurinec, P.E. Thompson, J. Niu and P.R. Berger: "Overgrown Si/SiGe Resonant Interband Tunnel Diodes for Integration with

CMOS", *62nd Device Research Conf. Dig.,* Vol. 1, pp. 109-110, 2004.

[5] N. C. Jin, R. Yu, P.R. Berger, P. E. Thompson, "Improved Vertically Stacked Si/SiGe Resonant Interband Tunnel Diode Pair with Small Peak Voltage Shift and Unequal Peak Currents", *Electron. Lett.*, Vol. 40, pp. 1548-1550, 2004.

[6] Chung, S.-Y.Y., Jin, R., Park, N., Berger, S-Y., Thompson, P.E., "Si/SiGe resonant interband tunnel diode with f_{r0} 20.2 GHz and peak current density 218 kA/cm^2 for K-band mixed-signal applications". *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 364-367, 2006.

[7] P.E. Thompson, G.G. Jernigan, S.-Y. Park, R. Yu, R. Anisha, P.R. Berger, D. Pawlik, R. Krom and S.L. Rommel: "P and B doped Si Resonant Interband Tunnel Diodes with as-grown Negative Differential Resistance", *Electronics Letters,* Vol 45, no. 14, pp. 759-761, 2009.

[8] S.-Y. Park, R. Anisha, P. R. Berger, R. Loo, N. D. Nguyen, S. Takeuchi, and M. Caymax: "Si/SiGe Resonant Interband Tunneling Diodes Incorporating δ-Doping Layers Grown by Chemical Vapor Deposition", *IEEE Electron Devices Letters*, Vol. 30, no 11, pp. 1173-1175, Nov. 2009.

[9] Rommel, S.L. et al, "Record PVCR GaAs-based tunnel diodes fabricated on Si substrates using aspect ratio trapping*", IEEE International Electron Devices Meeting* (IEDM), 2008.

[10] D. Pawlik, S. Sieg, S.K. Kurinec, S.L. Rommel, Z. Cheng, J.-S. Park, J. Hydrick and A. Lochtefeld: "Alloyed Junction Ge Esaki Diodes on Si Substrates realised by Aspect Ratio Trapping Technique", *Electronics Letters*, Vol. 44, no. 15, pp. 930-931, July, 2008.

[11] L. Ding, and Pinaki Mazumder*: "*On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic*", IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, no. 9, pp. 919-925, Sept. 2004.

[12] K. Karda, J. Brockman, S. Sutar, A. Seabaugh, and J. Nahas: "One-Transistor Bistable-Body Tunnel SRAM", *IEEE International Conference on IC Design and Tecnology, ICICDT`09*, pp. 233 – 236, 2009.

[13] Seabaugh A., "Promise of Tunnel Diode Integrated Circuits", *Tunnel Diode and CMOS/HBT Integration Workshop*, December, 1999.

[14] Shriram Kulkarni and Pinaki Mazumder, "Edge-Triggered Flip-Flop Circuit Based on Resonant-Tunneling Diodes and MOSFETs" *European Conference on Circuit Theory and Design*, August, 2001.

[15] Hui Zhang, Pinaki Mazumder and Kyounghoon Yang*, "*Resonant unneling diode based qmos edge triggered flip-flop design", *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2004.

[16] Pacha, C., et al., "Threshold logic circuit design of parallel adders using resonant tunnelling devices", *IEEE Trans. VLSI Systems*, 2000, 8, (5), pp. 558–572.

[17] Pettenghi, H., et al.,: "Single phase clock scheme for MOBILE logic gates". *Electronics Letters*. 42. (24). pp. 1382-1383. Nov. 2006.

[18] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, pp. 62-70, Feb. 1989.

[19] W. Prost et al.: EU IST Report LOCOM no. 28 844 Dec. 2000