A 0.2pJ/conversion-step 6-bit 200MHz flash ADC with redundancy

Hala Darwish, Gildas Léger and Adoración Rueda
Consejo Superior de Investigaciones Científicas (CSIC) and Universidad de Sevilla
Av. Américo Vespucio s/n, 41092 Sevilla, Spain.
e-mail: hala@imse-cnm.csic.es

***Abstract*—In this paper, a 200MHz 6-bit Flash analog-to-digital converter (ADC) is presented. The principal objective is to obtain a digital-friendly converter. Hence, small and simple latched comparators are used and redundancy allows reducing the offset down to an acceptable level. This obviously requires calibration but reduces power consumption, since small size transistors can be used and the unused comparators are powered down. The proposed ADC is designed in UMC $0.18\mu m$ CMOS technology. Full electrical simulations show that the ADC reaches an effective number of bits (ENOB) of 5.3 associated to a signal-to-noise-and-distortion ratio (SNDR) is 33dB. The converter consumes only 1.56mW and has figure-of-merit (FoM) of 0.2 pJ / conversion step.**

I. Introduction

Analog-to-Digital Converter (ADC) can be considered as one of the main blocks in a lot of systems, since they are mandatory to make the link between the analog outside world and the evermore ubiquitous digital computer world. Flash architecture is the most popular converter for its simplicity and low latency. It is mostly used for high speed low resolution converters [1].

Reducing the product cost, and meeting time-to-market requirements are essential instruments in the competition between IC manufacturers. These demands force the designers to integrate the overall systems in the same die and digital-compatible analog designs are definitely an asset [2]. Ever-deeper submicron technology increases the relevance of process variability poses major challenges for analog circuit design. Though systematic variability can be handled with careful layout practices, random variability is unavoidable. To overcome this problem, transistor sizing is considered as the simplest solution [3] but it is expensive in terms of power consumption. Another option is to use offset cancellation method [4], [5]. Capacitors are used to store the offset voltages in one half cycle and cancel it in the other half cycle. Unfortunately, switched capacitor circuits face difficulties with modern technologies [6]. Auto-zeroing [7] and averaging [8] techniques are other available options. Recently, redundancy has been proposed as an alternative. The idea is to use comparators with minimal dimensions and thus large random offsets. If several of them are implemented for each trip-point of the converter, a suitable calibration algorithm allows selecting the closest one to the ideal trip-point. The unselected comparators can then be turned-off reducing power consumption.

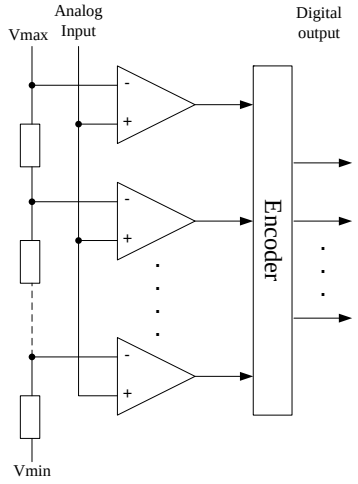

Fig. 1. block diagram of flash converter.

This paper is organized as follows: the ADC architecture is detailed in section II. Calibration choices are explained in section III. Section IV presents simulations results and section V closes the paper with concluding remarks.

II. ADC architecture

As known, flash converters divide the full-scale into fixed levels. each level has specific binary code. The conversion is done by determining the closest level for the analog signal at sampling instant. These levels are generated using reference ladder which can be implemented using capacitors [9] or resistors. A comparator array is then used to determine between which levels the analog signal is at the sampling time. Finally, the digital code is generated using encoder circuit. Figure 1 shows the block diagram of the Flash converter.

A. Comparator array

Latched comparator can be divided to three main groups as follows [10]:

- Static latched comparators. As it can be expected from the group name, the static consumption is large. Moreover, it is not suitable for high speed applications due to the slow regeneration process. On the other hand, it has good immunity to the kick-back noise. Some applications of this architecture can be found in references [11], [12].

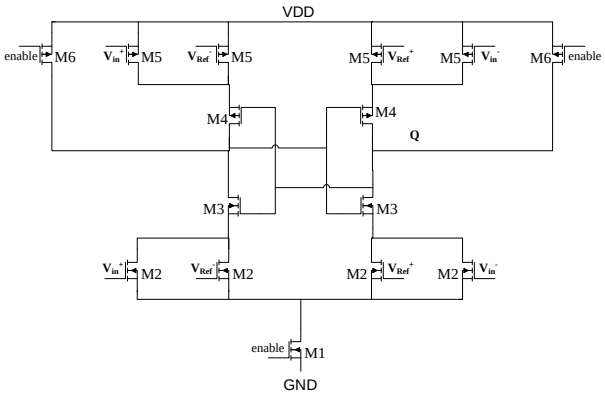

Fig. 2. schematic diagram of dynamic latch.

TABLE I
COMPARATOR DIMENSION

Transistor	number of fingers
M1	30
M2	1
M3	2
M4	4
M5	2
M6	1

- Class-AB latched comparators. This group improve the power efficiency and the speed of the regeneration process at the cost of higher kick-back noise. Examples of this architecture can be found in references [13]–[15]
- Dynamic latched comparators. In this group, static power consumption is approximately null (except that due to the leakage current). Power efficiency and speed are maximized. However, kickback noise can become a serious design issue. Different designs have been developed in the literature. The interested reader can find some of these architectures in references [16]–[18].

Comparator offset and kick-back noise are the main limitation to FLASH ADC performance. The offset, principally due to mismatch effects, affects the static non-linearity of the ADC. The converter trip-points are displaced, generating INL and DNL errors. Kickback noise, on the other hand, is a dynamic effect: The comparator decision – a fast switching mechanism – is fold back to the ADC input and the resistive reference ladder through capacitive coupling. We deal with comparator offset using redundancy, and try to minimize kickback by design reducing transistor sizes and optimizing the resistive ladder, as shown in the next subsection.

One of our objectives in this work is to simplify the design as much as possible to make it digital-friendly. So a simple latch architecture is implemented using standard transistors with minimum size fingers (240nm/180nm). No analog offset canceling techniques are used. Figure 2 shows the schematic diagram of the dynamic latch. The transistors used in the comparator circuit have dimensions shown in table I.

B. Reference ladder

The operation of the comparator circuit can be divided to two main phases. The first is the tracking/reset phase: both the input voltage and the reference are connected to the input transistors so the parasitic input capacitors are charged to the value to be compared. During this phase, the dynamic latch is disconnected such that it does not consume any current. The output nodes are tied to the power supply in order to avoid memory effects related to parasitic capacitors which could induce signal dependent comparison threshold. The second phase is the comparison phase in which the dynamic latch is enabled and performs the comparison between the input and the reference voltage. The switching between these two phases produces noise at the inputs of the comparator circuit through the coupling capacitance. This is known as kickback noise. Razavi defines the kickback noise as the power of the transient noise observed at the comparator input due to switching of the latch [19]. It generates a common-mode error but also a differential error that may corrupt the input signal if it is not taken into account during the circuit design. Kickback noise is particularly relevant for the reference voltage since it is generated from resistive ladder. Attempts to solve this problem already exist in the literature [10]. The simplest solution is to use low resistance value in the reference ladder. Another solution is to use preamplifier to isolate the input signals from the latch circuit. The circuit design will not be as simple as single stage comparator and other constrains must be taken into account. Using of class-AB comparator is an alternative in which the isolation is done using switches. This also increases the power consumption. Another way to isolate the input signal is to connect it to the comparator circuit through switches. These switches will be opened in the comparison phase and the signals to be compared are held on the input capacitors. Hence, this prevents the kickback noise from affecting the input signal but increases comparator offset due to charge injection mismatch. The main goal of this paper is to simplify the circuit as much as possible to save the design effort. We thus adopted the simplest solution for the kickback noise problem and maximized the ladder resistance value while keeping the kickback noise to an acceptable level. Fig. 3 shows the FoM of the ADC as a function in the resistance value of the reference ladder. The figure shows that for small resistance ladder value, the improvement in the kickback noise (which means improvement in ENOB of the ADC), will be canceled by the increase of the ladder power consumption. On the other hand, for the large resistance value the reduction in the power consumption will canceled by the significant kickback noise effect (reduction in ENOB of the ADC). The optimum value has been determined to be 206 ohm.

C. Encoder

Encoders have been studied in the literature. The most known encoder circuits are ROM based encoder, wallace-tree encoder, folded wallace-tree encoder, logic based encoder, multiplexer based encoder, fat-tree encoder, XOR based encoder, and priority look-ahead encoder. Since the sampling

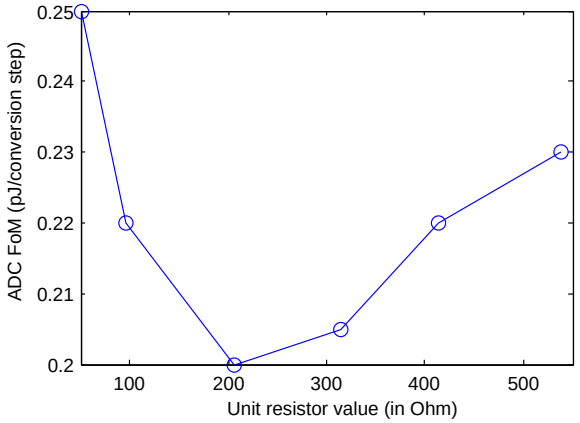

Fig. 3. Impact of the ladder unit resistor on the ADC Figure of Merit.

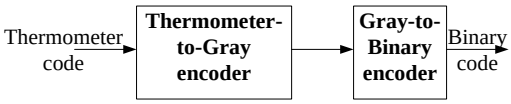

Fig. 4. logic based encoder block diagram.

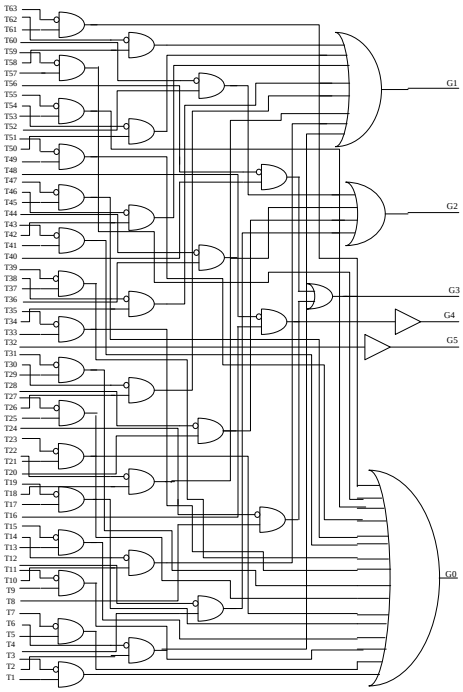

Fig. 5. Thermometer-to-Gray encoder.

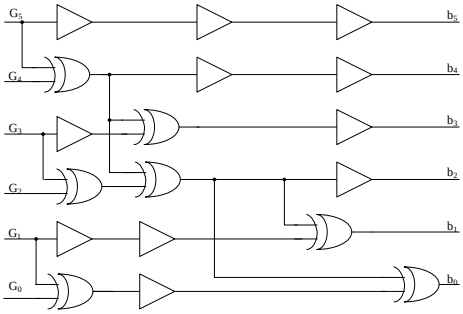

Fig. 6. Gray-to-Bainary encoder.

frequency of our converter is 200MHz, timing accuracy is not a very limiting factor as in designs like [8]. The main design criterion has thus been to minimize static power. According to reference [20], logic-based encoder is the most suitable type for lowering the overall power consumption. The encoding process is done in two steps [19]: a conversion from thermometer code to Gray code followed by a conversion from Gray code to binary code, as shown in Figure 4.

The Gray code minimizes the bubble error in the thermometer code [21], [22]. Schematic diagram of each block of this encoder are shown in Figure 5 and Figure 6, respectively. The encoder circuit has been optimized and synthesized using standard digital cells.

III. Calibration

As explained in previous section, we use a very simple dynamic latch structure for the comparators and almost minimum size transistors. This has great benefits in terms of compactness and power consumption, but the downside is obviously its sensitivity to offset. Instead of correcting each comparator offset – for instance using a look-up table – we opted to implement comparator redundancy as proposed in [6]. Several comparators are associated to each trip point. The external calibration algorithm measures the offset of each comparator and the one that is closer to the ideal trip-point is selected while the remaining ones are powered down. Notice that deviations in the reference voltages defined by the ladder are also corrected whenever the calibration relies on an independent reference. Typically, a static DAC with a resolution above 8bit should be sufficient. From a hardware viewpoint, a memory array is needed to store the proper comparator address for each trip-point. A straightforward implementation of redundancy consists in implementing a sufficient number of comparators at each trip point such that the standard deviation of the minimum offset is sufficiently reduced, as sketched in Fig. 7. This is the path followed in [23] and it makes sense when the comparator offset is relatively small. However, if it is large the amount of required redundancy greatly increases. In such a case the solution proposed in [6] is a better option. In this configuration, for a given trip point, the comparator can be selected not only among the comparators physically connected to that particular level but also among the adjacent levels, as shown in Fig. 8. For instance, a comparator with an offset of exactly -3 LSB would be perfect for the trip point that is located 3LSB below the one it was designed for. In our case, the standard deviation of the offset varies across the input range, but the worst case is in the order of $160mV$ which is much larger than an LSB. The straightforward redundancy implementation would require close to 128 comparators per level, which is clearly impractical. However, if we allow the comparators to be selected among 16 levels, we can reduce

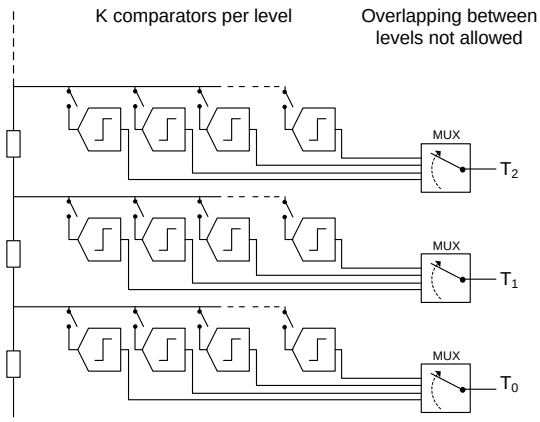

Fig. 7. Straightforward implementation of redundancy with K comparators per level.

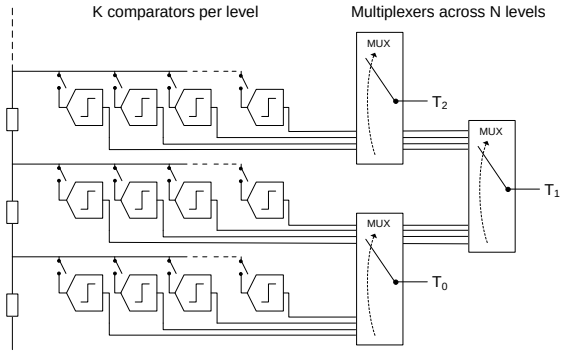

Fig. 8. Flexible implementation of redundancy with K comparators per level and an overlap allowed between N levels.

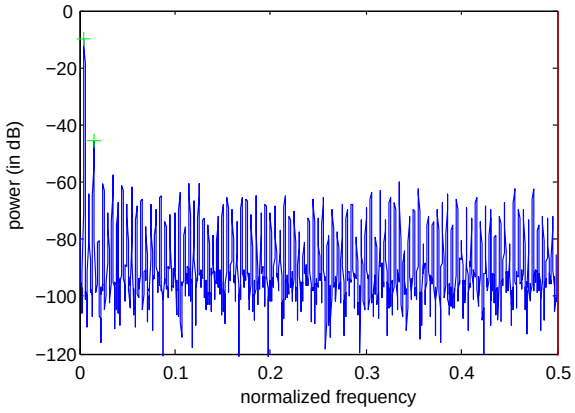

Fig. 9. Output power spectrum for a 1MHz full-scale input.

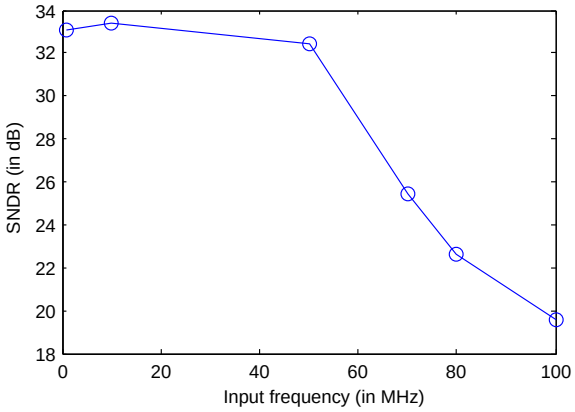

Fig. 10. SNDR of the ADC across the Nyquist bandwidth.

the required redundancy to a factor 8.

IV. Simulations Results

The ADC has been designed in UMC $0.18\mu m$ technology. All transistors used in this design are the nominal transistors (no special transistors used). Moreover, the supply voltage is 1.8V.

The complete ADC has been simulated, including the configuration switches that are mandatory to select the active comparators. However, electrical simulation of the calibration routine is still to be done and the results presented here do not include mismatch.

A 4000 samples FFT of the ADC output is performed to calculate the Signal to Noise and Distortion Ratio (SNDR) and deduce the Effective Number Of Bits (ENOB). For a full-scale 1MHz input sine-wave, the converter consumes only 1.56mW (1.37mW for the comparator array, 0.05mW for the reference ladder and 0.131mW for the encoder). Figure 9 shows the power spectrum of the output signal, that gives a SNDR of 33.1dB which corresponds to an ENOB of 5.3. Thus, the resulting FoM is 0.20 pJ/conversion step. Simulation of higher frequency sine-waves show little degradation up to 50MHz, as can bee seen in Fig. 10

Corner analysis considering a 5% variation of the supply voltage has also been done and table II gathers the obtained results. Performance degradation is most significant in the slow-slow corner. This is mainly due to the power supply reduction, since simulation at the same process corner but at nominal power supply voltage gives an ENOB of 5.1. The reason is that we have maximized the input range of the converter and the comparator input transistors are close to subthreshold operation in the extremities.

Although the converter is not in the state-of-art from speed point of view for FLASH converters, the FoM is quite competitive with other works, as can be seen in Table III. Provided that this result is obtained with a very simple digital-friendly comparator structure, it shows that digitally-assisted low precision flash ADCs can be a good candidate for integration in System-on-Chip (SoCs).

V. Conclusion

In this paper, 6-bit flash ADC has been implemented and simulated. Analog circuit design is relaxed by using comparator redundancy and calibration. In this way, a digital-friendly structure is obtained that relies on standard transistors with almost minimum size transistors. The ADC operates at a sampling frequency of 200MHz and reaches an ENOB of 5.3 for a power consumption of only 1.56mW. The obtained

TABLE II
CONVERTER CHARACTERISTICS AT PROCESS CORNERS

Process	typical	fast-fast	slow-slow	fast-N slow-P	slow-N fast-P
ENOB(bits)	5.3	4.9	4.75	5.17	4.8
SNDR(dB)	33.1	31.2	30.0	32.6	30.3
I_{ADC} (in μA)	764	845	668	781	698
I_{ladder} (in μA)	62	84	48	62	62

TABLE III
STATE-OF-ART

Reference	[24]	[25]	[26]	[2]	[27]	[28]	[29]	This work
Resolution (bits)	4	6	6	8	4	6	4	6
Technology (nm)	90	180	90	65	90	180	180	180
Supply voltage (V)	1.2	0.4	1.2	1	1.2		1.8	1.8
Power (mW)	30.2	0.00166	30	35	2.5	550	43	1.56
Area (mm2)	0.04	1.96		0.5	0.033	1.96	0.06	
ENOB (bits)	4	5.05	3.94	5.8	3.7	5.1	3.71	5.3
SNDR (dB)		32.5	25.5	37	23.8	32.5		33.1
INL (LSB)		0.72/ -0.9	0.54	1.32	$<$0.15	$<$1.1	-0.26	
DNL (LSB)		1.23/ -0.9	0.48	1.23	$<$0.2	$<$1	¡0.35	
DR (V)		0.110		1.06	0.2			1.6
Fin (MHz)	1	0.001526			640	7	10	1
Fs (GHz)	2.5	$4e^{-4}$	2.5	1.5	1.25	1	4	0.2
FoM (pJ/conv. Step)	0.76	0.125	0.79	0.42	0.16	16	0.82	0.2

Figure of Merit is 0.2 pJ/conversion step, which is within the state-of-the-art of FLASH converter efficiency.

ACKNOWLEDGMENT

This work has been partially funded by the Junta de Andalucia project P09-TIC-5386, the Ministerio de Economia y Competitividad project TEC2011-28302, both of them cofinanced by the FEDER program.

REFERENCES

[1] M. Gustavsson, J. J. Wikner, and N. Tan, *CMOS Data Converters for Communications*, 1st ed. Springer, Jan. 2011.

[2] G. Keskin, J. Proesel, J. Plouchart, and L. Pileggi, "Exploiting combinatorial redundancy for offset calibration in flash ADCs," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1904–1918, 2011.

[3] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[4] B. Razavi and B. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, 1992.

[5] K. Nagaraj, D. Martin, M. Wolfe, R. Chattopadhyay, S. Pavan, J. Cancio, and T. Viswanathan, "A 700M sample/s 6 b read channel A/D converter with 7 b servo mode," in *IEEE International Solid-State Circuits Conference*, 2000, pp. 426–427, 476.

[6] M. Flynn, C. Donovan, and L. Sattler, "Digital calibration incorporating redundancy of flash ADCs," *IEEE Transactions on Circuits and Systems II*, vol. 50, no. 5, pp. 205–213, 2003.

[7] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[8] M. Choi, J. Lee, J. Lee, and H. Son, "A 6-bit 5-GSample/s nyquist A/D converter in 65nm CMOS," in *IEEE Symposium on VLSI Circuits*, 2008, pp. 16–17.

[9] S. Chen and R. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, 2006.

[10] P. Figueiredo and J. Vital, "Kickback noise reduction techniques for CMOS latched comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 7, pp. 541 – 545, Jul. 2006.

[11] S. Lewis, H. Fetterman, G. Gross, R. Ramachandran, and T. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, 1992.

[12] B. Nauta and A. Venes, "A 70-MS/s 110-mW 8-b CMOS folding and interpolating A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1302–1308, 1995.

[13] H. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 4, pp. 509–515, 1994.

[14] G. Yin, F. Eynde, and W. Sansen, "A high-speed CMOS comparator with 8-b resolution," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 208–211, 1992.

[15] K. Uyttenhove and M. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1115–1122, 2003.

[16] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, 1993.

[17] T. Cho and P. Gray, "A 10 b, 20 msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, 1995.

[18] W. Song, H. Choi, S. Kwak, and B. Song, "A 10-b 20-Msample/s low-power CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 5, pp. 514–521, 1995.

[19] B. Razavi, *Principles of data conversion system design*. IEEE Press, 1995.

[20] G. Madhumati, K. Rao, and M. Madhavilatha, "Comparison of 5-bit Thermometer-to-Binary decoders in 1.8V, 0.18um CMOS technology for flash ADCs," in *2009 International Conference on Signal Processing Systems*, 2009, pp. 516–520.

[21] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 4-bit 5 GS/s flash A/D converter in 0.18um CMOS," in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2005, pp. 6138–6141 Vol. 6.

[22] P. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s flash ADC in 0.18-um CMOS using averaging termination," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1599–1609, 2002.

[23] M. Bichan and A. Carusone, "The effect of redundancy on mismatch-induced offset and random noise in a dynamic comparator," in *Research in Microelectronics and Electronics, 2009. PRIME 2009. Ph.D.*, 2009, pp. 180–183.

[24] T. Sundstrom and A. Alvandpour, "A 2.5-GS/s 30-mW 4-bit flash ADC in 90nm CMOS," in *NORCHIP*, 2008, pp. 264–267.

[25] D. Daly and A. Chandrakasan, "A 6-bit, 0.2 v to 0.9 v highly digital flash ADC with comparator redundancy," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3030–3038, 2009.

[26] T. Sundstrom and A. Alvandpour, "A 6-bit 2.5-GS/s flash ADC using comparator redundancy for low power in 90nm CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 215–222, 2009.

[27] G. Van der Plas, S. Decoutere, and S. Donnay, "A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm digital CMOS process," in *IEEE International Solid-State Circuits Conference, ISSCC*, 2006, p. 2310.

[28] C. Chang, C. Hsiao, and C. Yang, "A 1-GS/s CMOS 6-bit flash ADC with an offset calibrating method," in *IEEE International Symposium on VLSI Design, Automation and Test, VLSI-DAT*, 2008, pp. 232–235.

[29] S. Sheikhaei, S. Mirabbasi, and A. Ivanov, "A 43 mW single-channel 4GS/s 4-bit flash ADC in 0.18 um CMOS," in *IEEE Custom Integrated Circuits Conference, CICC*, 2007, pp. 333–336.