A 350 μW 2.3 GHz integer-N frequency synthesizer for Body Area Network applications

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***Abstract*— This paper presents a low power integer-N synthesizer with an output frequency of 2.3 GHz. The complete PLL has been integrated in a 90 nm CMOS technology and operates from a 1 V supply voltage. The synthesizer has been optimized for power consumption by employing an efficient quadrature VCO and a phase-switching prescaler. It achieves a phase noise of -121 dBc/Hz @3MHz while consuming only 350 μW in the PLL core. The typical reference spur level is about -40 dBc.**

I. Introduction

Body area networks (BAN) based on miniature wireless sensors are expected to allow for a lot of new applications. They range from entertainment and automation to health care or human interface devices. In many of these applications, the need for ultra-low power consumption is a priority because wireless sensor nodes are supplied by small batteries or even rely on autonomous energy scavenging techniques.

A power-hungry block in a wireless transceiver is the generation of quadrature LO signals. Therefore, BAN communication standards such as ZigBee or Bluetooth low energy specify a moderate phase noise performance. This leaves design space for optimizing the power consumption of this critical building block. In this paper a very low power frequency synthesizer is presented that is intended for application in a direct-conversion receiver. This receiver architecture is particularly suitable for low-power and low-cost applications [1].

The architecture and design of the frequency synthesizer is described in section II. Section III presents measurement results of the implemented synthesizer. It operates with a core power consumption of only 350 μW while achieving a phase noise performance of -121 dBc/Hz @3MHz. Finally, some concluding remarks are given in section IV.

II. Architecture and Circuit Design

Figure 1 shows the block diagram of the frequency synthesizer. It employs a conventional charge-pump PLL architecture using an integer-N division ratio. Due to the integer-N configuration the phase-frequency-detector (PFD), charge-pump (CP) and loop filter (LPF) operate at the low reference frequency of $\approx$2 MHz and hence consume very little power. Therefore, the power consumption of the PLL core is dominated by the blocks working at radio frequency, i.e. the quadrature voltage-controlled oscillator (QVCO) and the programmable divider.

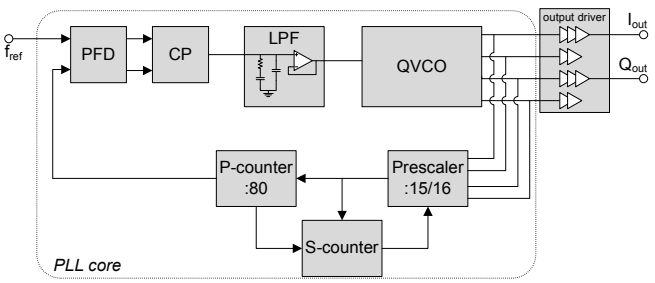

Fig. 1. Block diagram of the synthesizer

A. Quadrature VCO

In modern wireless transceivers quadrature LO signals are inevitable. The quadrature phases are often generated using an oscillator running at twice the LO frequency followed by a frequency divider-by-2 [2]. However, the doubled oscillation frequency and the frequency divider lead to an increased power consumption. A more power efficient alternative is the quadrature VCO using two LC oscillator cores that are coupled to each other in order to operate in quadrature [3].

The proposed quadrature VCO is shown in Fig. 2 (detailed description in [4]). It employs two LC oscillator cores with complementary NMOS and PMOS transconductance stages (Mx) that reuse the same bias current. Coarse frequency tuning to compensate process variations is achieved with a switched MOM-capacitor bank while PMOS varactors allow for fine frequency control through v_{ctrl}.

Apart from the current-reuse technique, the most important aspect for achieving low power consumption is the selection of the inductor. In order to minimize the parallel loss conductance of the LC tank, the inductor with the highest product of quality factor and inductance must be used. Based on this criterion a 7-turn differential 13.6 nH inductor has been selected.

The two cores are coupled to each other by means of parallel transistors MCx. This parallel coupling has the advantage that the required supply voltage is not increased by the coupling mechanism. Note that the coupling transistors MCx are connected through series resistors to the

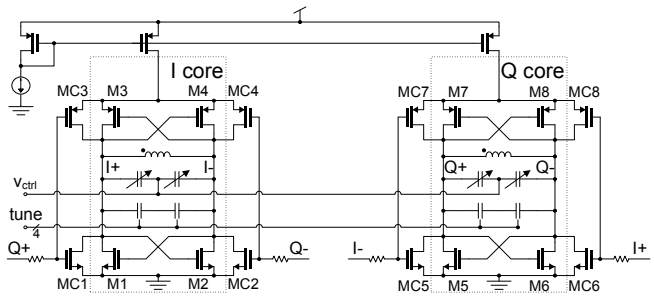

Fig. 2. Schematic of the quadrature VCO

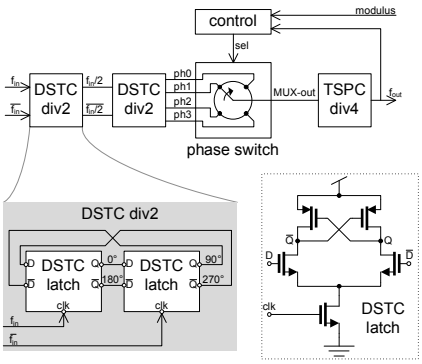

Fig. 3. Phase-switching prescaler (modulo 15/16)

oscillating output nodes of the other core. These resistors together with the gate capacitance of MCx form an RC phase shifter that reduce the phase difference between the core transistors Mx and the corresponding coupling transistor MCx. It has been shown that reducing this phase difference to ideally 0° decreases the 1/f-noise contribution of the coupling transistors and also assures that the QVCO has only one stable mode of operation [5].

B. Divider

The power consumption of high-speed frequency dividers is mainly defined by the sub-blocks that operate at the highest frequency, i.e. the input frequency. Consequently, the phase-switching prescaler architecture can achieve very low power consumption because only one asynchronous divider-by-2 is operated at the high input frequency and all subsequent blocks already operate at divided frequencies [6]. Figure 3 shows the implemented 15/16-prescaler.

The two cascaded divide-by-2 blocks at the input of the prescaler consist of dynamic single-transistor-clocked latches (DSTC) in a master-slave flip-flop configuration [7]. The DSTC-based divider-by-2 (DSTC div2 in Fig. 3) achieve low power consumption thanks to their low parasitic capacitance.

The phase switch is implemented using 4 tri-state buffers, where only one is activated at the same time. After the phase switch only single-ended signals are required, and hence the following divider-by-4 uses two cascaded true-single-phase-clocked flip-flops [8]. Upon rising output edges of the prescaler, the phase switch is rotated towards the preceding phase which leads to a division by 15 if the modulo input is set accordingly. Otherwise the phase switch stays unchanged leading to a division by 16.

The divider is completed by an asynchronous pulse counter and a synchronous programmable swallow counter (P- and S-counter in Fig. 1). The overall division factor can be programmed to all integer values from 1200 to 1263.

C. Baseband section

The baseband section of the PLL comprises a phase-frequency-detector (PFD) based on TSPC flip-flops and a charge-pump with a nominal output current of 10 μA.

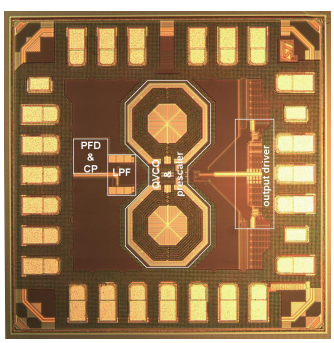

Fig. 4. Die photo of the test chip (die size is 1-by-1 mm)

When no current is injected into the loop filter the current mirrors at the output of the charge-pump are switched off completely, i.e. no current-steering is employed. This reduces the static current consumption of the charge-pump at the expense of an increased dynamic mismatch between high-side and low-side current which eventually leads to higher reference spurs.

The loop filter sets the loop bandwidth to nominally 100 kHz. In order to make the loop characteristic independent of the nonlinear input-capacitance of the QVCO a buffering stage is included in the loop filter. Thanks to its operation in weak inversion it hardly reduces the usable output swing of the baseband section.

III. Measurement Results

The presented frequency synthesizer, shown in Fig. 4, has been implemented in a 90 nm CMOS process with 7 metal layers (2 thick top layers). The active area of the PLL core is approximately 0.25 mm², which is mainly occupied by the two large inductors of the QVCO. The test chip has been encapsulated in a QFN-28 package and measurements have been performed using an Agilent E4440A PSA spectrum analyzer. The supply voltage for the complete test chip has been set to 1 V while the reference frequency was 1.86 MHz.

The measured current consumption of the PLL core is 350 μA while the output drivers require about 3 mA. Within the core of the PLL the QVCO is supplied in-

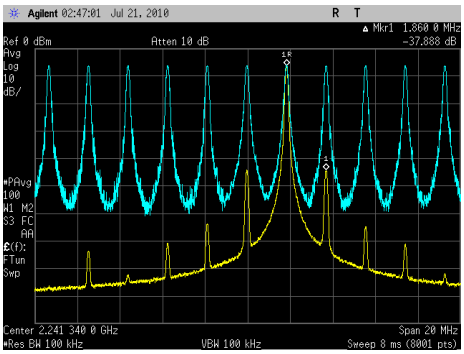

Fig. 5. Measured output spectrum of the synthesizer: channel 6 spectrum (yellow) and max-hold superposition of channel sweep (blue)

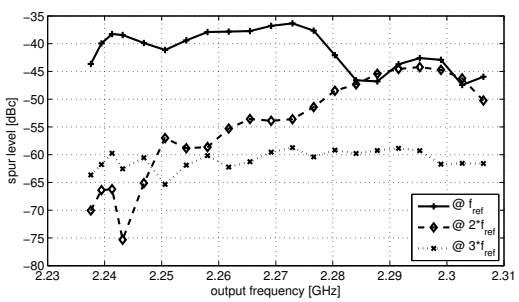

Fig. 6. Measured reference spur level (upper sideband)

dividually and draws 210 μA. The remaining PLL blocks consume altogether 140 μA. The test setup does not allow further measurements on the supply current break down. However, from post-layout simulations can be concluded that about 120 μA must be dissipated by the phase-switching prescaler, 14 μA by P- and S-counter while the baseband section requires only 6 μA supply current.

Figure 5 shows the output spectrum of the synthesizer for channel 6 (N=1200+6) and a composite spectrum (max-hold) of a sweep through the channels 0 to 10. The spectra show the typical integer-N characteristic where both channel spacings and spur locations are directly defined by the reference frequency.

The spur level at the reference frequency and at the first harmonics thereof are shown in Fig. 6 versus the output frequency of the synthesizer. The most dominant spur is the one at the reference frequency f_{ref} with about -40 dBc. This reference spur is mainly caused by mismatch of the charge-pump current pulses. The minimum reference spur level at 2.285 GHz reflects the best matching of the current pulses. This frequency translates into a charge-pump output voltage of approximately 0.3 V. At almost the same frequency the spur level at $2f_{ref}$ reaches its maximum due to the high VCO gain in this range.

In order to evaluate the phase noise performance of the synthesizer, the recorded spectra have been normalized to the center frequency and scaled to a resolution bandwidth of 1 Hz. Figure 7 depicts the phase noise performance

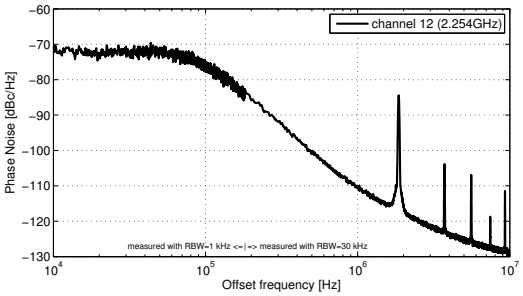

Fig. 7. Measured phase noise performance of the synthesizer (upper sideband)

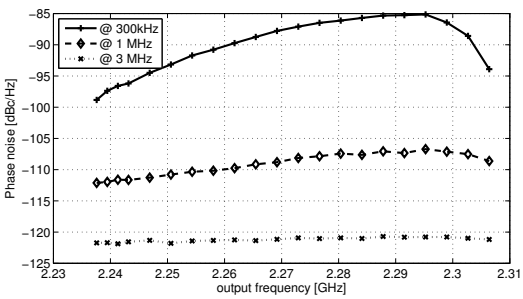

Fig. 8. Measured phase noise (upper sideband)

of channel 12 showing a loop bandwidth of the PLL of ≈100 kHz.

The phase noise performance versus output frequency of the PLL is shown in Fig. 8. At an offset of 3 MHz the phase noise is almost constant around -121 dBc/Hz. However, as the offset frequency decreases the dependency on the VCO gain gets clearer. At 2.29 GHz (v_{ctrl} ≈0.25V) the VCO gain reaches its maximum and hence increases the loop bandwidth. This leads to an increased phase noise level especially at 300 kHz offset.

The settling behavior of the PLL after applying the reference signal is depicted in Fig. 9. The plot shows a settling time of the QVCO control voltage v_{ctrl} of about 55 μs. During the first 25 μs the PLL aligns the phase of reference and feedback signal while in the remaining 30 μs the frequencies are balanced.

The most important parameters of the presented frequency synthesizer are summarized in Table I. Due to the lack of a single-sideband mixer in the experimental setup, the quadrature error of the QVCO could not be measured accurately. Oscilloscope measurements at the I- and Q-outputs confirm quadrature operation but with a phase error that is dominated by the output buffers and the test setup. The I/Q-imbalance obtained from post-layout Monte-Carlo simulations is below 5°, which is sufficient for a direct conversion receivers [1].

Table II compares the presented quadrature PLL to recently published frequency synthesizers in the same frequency range. This work achieves by far the lowest power consumption while achieving a slightly inferior phase noise performance.

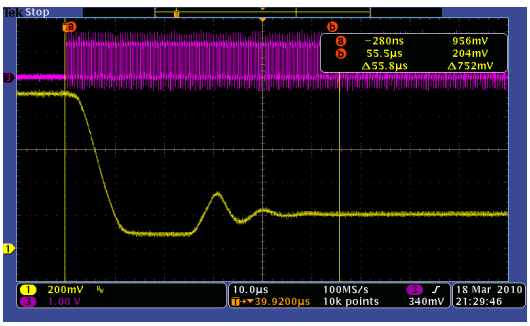

Fig. 9. Measured settling behavior of the PLL: QVCO control voltage (yellow) and reference frequency input (purple)

TABLE I
PERFORMANCE SUMMARY OF THE SYNTHESIZER

Design details	
Technology	ST 90 nm 1P7M CMOS
Active area	0.25 mm²
Supply voltage	1 V
Reference frequency	1.86 MHz
Output frequency	2.24 – 2.31 GHz
Loop bandwidth	70 – 150 kHz
Measured current consumption	
QVCO	210 μA
Divider, PFD, CP, LPF	140 μA
Driver for 50Ω-load	3 mA
Measured noise and spur performance	
Integrated phase error (50 – 500 kHz)	< 8°
Phase Noise @ 1 MHz	< -107 dBc/Hz
Phase Noise @ 3 MHz	< -121 dBc/Hz
Reference spur level	< -36 dBc
Timing	
Settling time	< 60 μs

IV. CONCLUSIONS

A very low power frequency synthesizer with quadrature outputs has been presented. A power consumption of only 350 μW is achieved by using a very efficient quadrature VCO employing large inductors and a phase-switching prescaler with dynamic logic. The quadrature VCO employs an RC phase shifter to couple the two cores to each other. This passive technique reduces the phase noise contribution of the QVCO without increasing power consumption.

The presented PLL shows that a simple charge-pump without current-steering can achieve a reference spur level of approximately -40 dBc. The phase noise level of -121 dBc/Hz @3MHz offset is similar to state-of-the-art frequency synthesizers intended for BAN applications. The overall performance is compatible with the Bluetooth low energy standard which operates in the 2.4 GHz ISM band except for a required re-centering of the VCO tuning range [12].

TABLE II
PERFORMANCE COMPARISON TO RECENT FREQUENCY SYNTHESIZERS

	[9]	[10]	[11]	[2]	this work
CMOS Process (nm)	180	90	130	90	90
Architecture	int-N	int-N	frac-N[1]	frac-N	int-N
Supply voltage (V)	1.2	0.5/0.65	1.2	0.6	1.0
Frequency (GHz)	2.4	2.5	2.4	2.5	2.3
Power (mW)	4.2	6	3.2	12.5	0.35
Phase Noise (dBc/Hz @Hz)	-116.5 @1M	-123 @3M	-121 @2M	-127.1 @3M	-121 @3M
close-in Phase Noise (dBc/Hz @Hz)	N/A	-68 @10k	-85 @10k	-75 @10k	-72 @10k
quadrature outputs	no	no	no	yes	yes

[1] offset PLL

ACKNOWLEDGMENT

This work has been supported by the Spanish Ministry of Science & Innovation under grant TEC2009-08447, the Junta de Andalucía under grant TIC-02818 and the 2007-2013 FEDER Program.

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