# 2.4 GHz Single-ended Input Low-Power Low-voltage Active Front-end for ZigBee Applications in 90 nm CMOS

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***Abstract*—A 2.4-GHz CMOS single ended-input differential-output front-end built with a common source low noise amplifier (CS-LNA) and a switched transconductor mixer (SW-MIX) is presented. The circuit is designed and optimized to work in a ZigBee receiver. Since this is a low power consumption standard, a single-ended LNA is preferred over a fully-differential topology because it leads to lower cost in area and power consumption. Also, moderate and weak inversions regions were selected for the operation of the principal transistors. The front-end prototype has been implemented in a 90 nm RF process and occupies a chip area of 0.74 mm$^2$ including on-chip inductors. Very competitive results are observed: a maximum conversion gain (CG) of 30 dB, a DSB noise figure of 7.5 dB, a maximum IIP3 of -12.8 dBm and IIP2 of 14.4 dBm while it consumes 4.7 mW from a 1.2 V supply.**

***Index Terms*—Active front-end, CS-LNA, switched-transconductor mixers, ZigBee, low power, low voltage, 90 nm RF CMOS, weak inversion, moderate inversion.**

## I. Introduction

Low power radiofrequency (RF) applications as ZigBee or Bluetooth Low Energy are taking the market areas of short range and low rate communications. Typical applications of these standards include wireless sensor networks, and industrial and personal uses running on just button cells or batteries; all of them claiming for low-cost chip solutions. The work presented in this paper contributes to these low-cost solutions by providing simple but efficient RF front-end design for low-power low-voltage ZigBee receivers.

In this sense, a single-ended LNA instead of a differential one is used, hence discarding the need of an input balun, reducing to a half the power consumption, and diminishing considerably the occupied silicon area because a gate inductor and a drain inductor are unnecessary. In addition, transistors are biased in moderate or weak inversion regions; so that a considerable reduction in power consumption and voltage supply under one volt are feasible.

The designed RF front-end complies with the specifications of a 2.4 GHz ZigBee receiver, comprising a single-ended common source low-noise amplifier (CS-LNA) and a differential switched transconductor mixer (SW-MIX). The system uses a 2.5 MHz intermediate frequency (IF) because of its good trade-off between image rejection requirements and specifications of the channel selection filter in a receiver.

RF design with MOS transistors working in moderate and weak inversion is proven to be efficient [1], but it, together with low voltage supply impose the search of adequate circuit architectures and design decisions. In the rest of the paper, details on how we have faced these challenges are given.

The paper is organized as follows. Section II presents the design approach of the front-end and of each of its blocks, as well as the obtained simulation results. Next, Section III exposes the experimental measurements made on the implemented system. Finally, Section IV summarizes the main contributions of this work.

## II. Design Implementation

The schematic of the intended front-end is shown in Fig. 1. The initial specifications of CS-LNA and SW-MIX blocks are set to comply with the specifications of the ZigBee standard, considering the existence of a band filter before the LNA with a loss of -3 dB. The system is designed to be tested with RF microprobes, which means that the CS-LNA input impedances and the SW-MIX clock port impedances were set to 50 Ω. Because both blocks have been also implemented and tested separately from the front-end, their output and input impedances are, respectively, fixed to 50 Ω.

A discrete gain control has been included in the current source of the CS-LNA to implement two levels of gain in this block. Choosing the low level permits to prevent the saturation of the SW-MIX when high level input signals arrive to the front-end.

To distribute, according to the ZigBee standard, the power consumption, noise figure and gain of each block in the receiver (off-chip input band filter, the proposed front-end and an IF back-end), an optimization process which considers the design trade-offs was followed. In this way, the imposed specifications to the front-end were: voltage conversion gain (CG) higher than 25 dB, noise figure lower than 12 dB, and finally the 1dB compresion point (P1dB) should be higher than -23dBm (to handle correctly the maximum signal at receiver input: a ZigBee signal with an interferer). Considering that P1dB is around 10 dB less than IIP3 point, specification value for IIP3 when front-end is in low-gain mode, has to be over -13dBm.

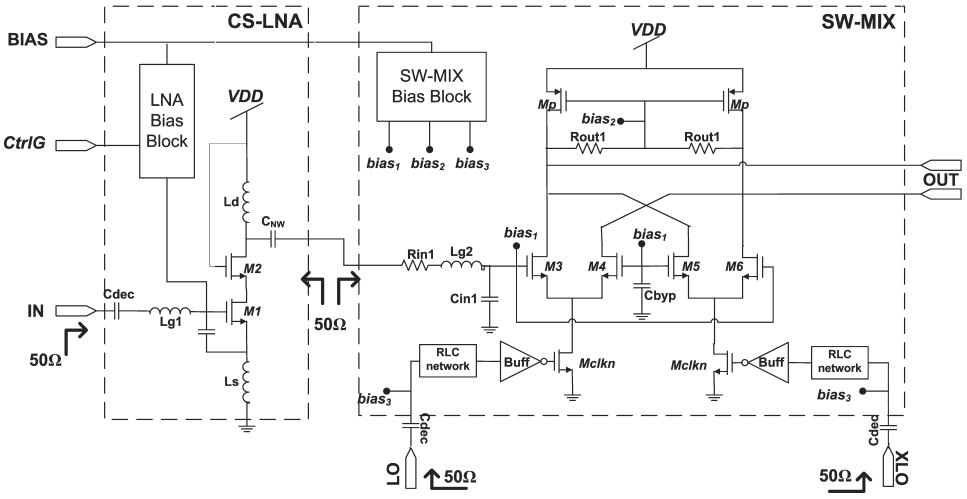


Figure 1. RF front-end schematic.

In next subsections a brief description of the blocks topologies, the initial requirements to comply with the general specifications, as well as the simulated characteristics of each of them are presented. Finally, post-layout simulation results of the whole system are provided.

### A. LNA design

The single-ended inductive source degenerated CS-LNA is designed under a trade-off between power consumption and noise figure without spoiling the power gain. As previously stated, both input and output impedances are fixed to be real and equal to 50 Ω, so input and output matching networks are implemented. The LNA design optimization methodology followed is presented in [2], where the $g_m/I_D$ tool for RF circuits is described. Amplification transistor $M_1$ of Fig. 1 is biased in moderate inversion reducing LNA consumption and leaving open the possibility of lowering the supply voltage. A cascoded transistor $M_2$ is added to improve the isolation between blocks, especially with the interfering RF signals generated at the input of the SW-MIX by its clocks. Inductors $L_s$ and $L_{g1}$ are adjusted to reach the required input impedance. An extra capacitor between gate and source terminals of $M_1$ is added to decouple noise and consumption [3]. Inductor $L_d$ is chosen to obtain the highest available gain.

A control bit, *CtrlG*, is included in the bias circuit of the CS-LNA to switch between a high gain (hg) and a low gain (lg). A current branch of the current generation circuit is switched on/off with this control, modifying the final bias current of the LNA. The low gain is used when the CS-LNA input signal is high enough to generate high amplitude levels in the SW-MIX inputs which degrade its linearity.

The LNA initial specifications were: gain (hg) greater than 10 dB with a noise figure lower than 5 dB and an IIP3$>$0 dBm. Electrical simulations with SpectreRF show a final design with a high/low gain of 12.4/9 dB, noise figure of 3.66/4.1 dB (hg/lg), an IIP3 of -1.24 dBm and a power consumption of 1.44/0.92 mW (hg/lg) for 1.2 V supply.

### B. MIXER design

The differential switched transconductor mixer, based on [4], is presented in Fig. 1. It is composed by the mixer core and two clock buffers. Transistors $M_3$ to $M_6$ form the mixer transconductance stage; they are designed to work in weak inversion to open the possibility of using a low supply voltage in conjunction with a large output swing. Their aspect ratio is chosen carefully to minimize their flicker noise and consequently not degrading the noise figure of the block. Resistors $R_{out1}$ perform the current-to-voltage conversion. To maximize the output swing, pMOS load transistors, $M_p$, with the bias voltage, $bias2$, shift the common mode output voltage near to $V_{DD}/2$. Transistors $M_{clkn}$ turn on/off the current of the active pairs since they serve as switches when they are driven by two anti-phase square clocks. The sizing of these transistors is chosen to improve the conversion gain reducing the switching time until we can consider the mixing operation is performed with square wave clocks. Because it is necessary to obtain the square clocks from external sine or quasi-sine wave signals applied to LO, XLO ports, RLC matching networks and a two level regenerative CMOS buffer (Buff) have been designed.

Similarly, to achieve an input impedance of 50 Ω, input matching network ($R_{in1}$, $L_{g2}$, $C_{in1}$) has been implemented.

The complete SW-MIX design methodology follows the guidelines in [5] with the following specifications: conversion gain higher than 15 dB, DSB noise figure lower than 17 dB and IIP3 greater than -5 dBm. From electrical simulations, the final design shows a conversion gain of 20 dB, a noise figure of 15.1 dB, an IIP3 of -3.5 dBm and a power consumption of 3.24 mW including the last level of the regenerative buffer and 5.9 mW considering whole.

### C. Front-end post-layout simulations.

The complete system characteristics under post-layout simulations are presented in the second column of Table I. Moreover, noise figure and conversion gain in the range of

Table I
POST-LAYOUT SIMULATION AND EXPERIMENTAL RESULTS OF THE FRONT-END.

| Parameter | Simulated Value | Measured Value |
|---|---|---|
| Current consumption (hg/lg) | 3.9/3.47 mA | 3.9/3.47 mA[a] |
| CG @ 2.5 MHz (hg/lg) | 32.5 dB /30 dB | 30 dB /28 dB |
| NF @ 2.5 MHz (hg) | 8.5 dB | 7.5 dB |
| NF @ 2.5 MHz (lg) | 9.3 dB | 9.6 dB |
| IIP3 (hg) | -12.8 dBm | -16.2±1.0 dBm |
| IIP3 (lg) | -9.8 dBm | -12.8±1.5 dBm |
| IIP2 (hg) | - | 14.4±1.0 dBm |
| $Z_{in}$ @ 2.445GHz | 44.7 Ω | 47 Ω |
| $S_{11}$ of *In* port @ 2.445GHz | -24 dB | -21 dB |

[a] Inferred from the total measured current of 6.9/6.47 mA (hg/lg) minus the simulated current of 3.0 mA of the first level clock buffers.

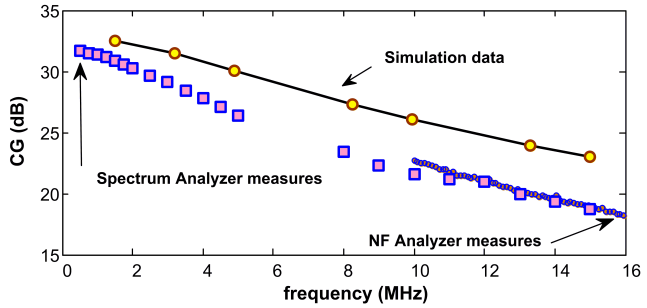


Figure 2. Measured conversion gain of the integrated Front-end compared with the simulated results (high gain case).

[1.5, 15] MHz are shown in the continuous lines of Figures 2 and 3, respectively.

## III. EXPERIMENTAL RESULTS

The microphotograph of the implemented front-end is shown in the inset of Fig. 5. The layout is not optimized because the same integration has served to several alternative experiments. The circuit occupies a net area of 0.74 mm$^2$, where 45 % is the mixer area and its two thirds are occuppied by the inductors of the matching networks of the clock ports. In order to properly join the LNA and the MIXER, adjustments in the matching networks were performed iteratively through post-layout simulations. This way, we adjusted the blocks impedances, maintaining the initial blocks performances especially in terms of conversion gain.

The measurements were done in an RF microprobe station. S-parameter measurements of the front-end input port were performed with the Agilent N5230 Network Analyzer. Conversion gain, IIP2 and IIP3 and low-frequency (<5 MHz) Noise Figure values were measured with the Agilent E4440A Spectrum Analyzer; noise figure for frequencies greater than 10 MHz were made with the Agilent N8974A Noise Figure Analyzer. Because the mentioned equipment only couples with single-ended ports, we loaded a buffer at the SW-MIX output to transform the differential signal OUT to a single-ended one. The anti-phase clocks in LO, XLO ports were band-pass filtered signals originated at the HP81134A Pulse Pattern Generator with frequency $f_{LO} = 2.4425$ GHz and amplitude 1.5 V peak-to-peak, for all measurements. The measured front-end characteristics are listed in the third column of Table I.

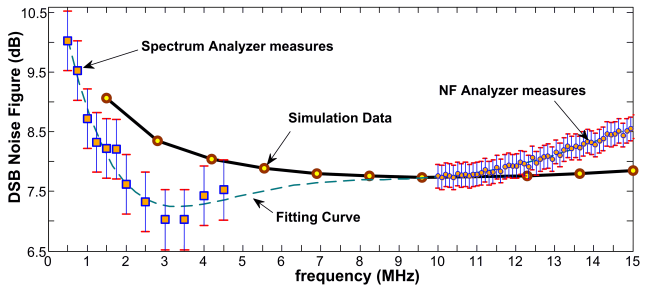


Figure 3. Measured noise figure of the integrated Front-end compared with the simulated results (high gain case).

Conversion gain was obtained using a -35-dBm single tone input signal with frequency in the range $f_{RF}$=$f_{LO}$+[1.0, 20] MHz. The difference of approximately 3 dB between simulated and measured conversion gain is attributed to technology variations and parasitics not considered in the post layout extraction.

IIP3 and IIP2 values were obtained using a two tone input signal. Frequencies of $f_{RF1}$=$f_{LO}$+$f_{IF}$-0.3 MHz and $f_{RF2}$=$f_{LO}$+$f_{IF}$+0.3 MHz have been used for the in-band IIP3 test. From the obtained data, the high gain P1dB point is about -26 dBm, then we infer that the high gain mode should be used up to an input of -30 dBm (considering a margin of -4 dB); for higher inputs (up to the -20 dBm) it is utilized the low gain mode. Fig. 4 shows the curves corresponding to the fundamental tone appearing at 2.2 MHz and the third order intermodulation spur at 1.6 MHz. Similarly, an IIP2 two-tone test with frequencies of $f_{RF1}$=$f_{LO}$+10 MHz and $f_{RF2}$=$f_{LO}$+12.5 MHz have been used; doing the intermodulation, spur falls in 2.5 MHz and the down-converted input signals in 10 MHz and 12.5 MHz. The measured value was 14.4 dBm.

As it has already stated, the DSB noise figure was measured with two different equipment because the Noise Figure Analyzer only measures above 10 MHz. In Fig. 3 these measures are presented together with the simulation results.

The measured values of the specifications are also consistent with the estimated values through chain expressions of cascaded stages (Friis' formula-wise) [13], particularized in this case for the CS-LNA and the SW-MIX blocks. The parameters of each one were obtained on independent integrations that the presented here. Their respective values were: gains: 9.6 dB(lg) and 20.0 dB; noise figure: 4.3 dB and 14.0 dB; IIP3: -4.5 dBm and -3.7 dBm; and finally, IIP2: 30.5 dBm and 25.4 dBm.

The OQPSK output spectrum is shown in Fig.5 for an input power of -35 dBm measured with a bandwidth resolution of 130 kHz.

Table II compares the results of our design with similar front-ends using only active mixers , utilizing the figure of merit presented in [14], $FOM = (G \cdot IIP3 \cdot f)/((F-1) \cdot P)$; where $G$ is the voltage gain in $V/V$, $IIP_3$ is expressed in mW, $f$ is the working frequency, $F$ is the noise factor, and $P$ is the total power in mW. Since the proposed circuit has been designed to be included in an IEEE 802.15.4 standard

Table II
COMPARISON BETWEEN THE PRESENTED FRONT-END DESIGN AND OTHER WORKS.

| Ref. | techno | CG (dB) | NF (dB) | IIP3 (dBm) | Power (mW) | f (GHz) | FoM (MHz) | Comments |
|---|---|---|---|---|---|---|---|---|
| This work (lg) | 90nm | 28 | 9.6 | -12.8 | 4.68 | 2.445 | 95.4 | - |
| This work (hg) | 90nm | 30 | 7.5 | -16.2 | 4.68 | 2.445 | 85.7 | IIP2=14.4dBm |
| [6] | 180nm | 22 | 9 | -15 | 5.4 | 2.445 | 25.9 | dual band |
| [7] | SiGe-350nm | 26 | 8.7 | -13 | 8.6 | 2.445 | 44.3 | - |
| [8] | 180nm | 31.5 | 11.8 | NA | 0.5 | 2.4 | - | NF @ 10MHz |
| [9] | 130nm | 14.5 | 24.5 | -21 | 1.68 | 2.445 | 0.2 | out-of-band IIP3 |
| [10] | 180nm | 19 | 11 | -9 | 4.25 | 2.445 | 55.7 | IF=480 MHz |
| [11] | 130nm | 23.4 | 5.8 | -4.8 | 24 | 2.3 | 167.5 | for 802.11b-g |
| [12] | 180nm | 21.4 | 13.9 | -10 | 6.48 | 2.445 | 18.8 | IF=2 MHz |

receiver, the front-end was carried out to optimize the overall performance of the receiver. As it is shown in Table II, the proposed design presents a very good compromise in terms of noise, linearity and power consumption, if it is compared with other active front-ends, especially with the most recently reported as [6] or [7].

## IV. CONCLUSIONS

The design and implementation of a receiver front-end comprising a single-ended LNA and a differential switched transistor mixer has been realized in a CMOS 90 nm technology with 1.2 V voltage supply. The single-ended input reduces the external chip components as well as the area occupied by the LNA inductors and the power consumption. A control bit enables the LNA gain reduction to minimize the linearity degradation of the mixer. The system achieves a minimum measured noise figure of 7.5 dB at 2.5 MHz, a voltage conversion high gain of 30 dB, a maximum IIP3 of -12.8 dBm, an IIP2 of 14.4 dBm with a low power consumption of 4.7 mW.

## V. ACKNOWLEDGEMENTS

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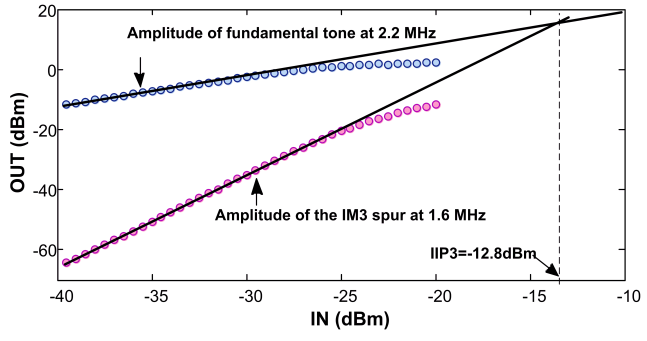


Figure 4. IIP3 of the fabricated circuit for the low gain case.

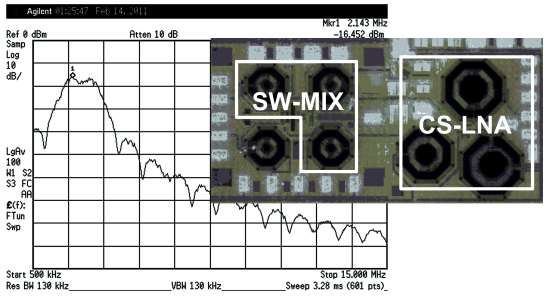


Figure 5. Output power spectrum for an OQPSK modulated input signal and front-end microphotograph.

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