A 55 μW programmable gain amplifier with constant bandwidth for a direct conversion receiver

Jens Masuch and Manuel Delgado-Restituto

Institute of Microelectronics of Seville (IMSE-CNM-CSIC), Avda. Américo Vespucio s/n, 41092-Seville, SPAIN

ABSTRACT

A fully differential programmable gain amplifier (PGA) with constant transfer characteristic and very low power consumption is proposed and implemented in a 130 nm CMOS technology. The PGA features a gain range of 4 dB to 55 dB with a step size of 6 dB and a constant bandwidth of 10–550 kHz. It employs two stages of variable amplification with an intermediate 2nd order low-pass channel filter.

The first stage is a capacitive feedback OTA using current-reuse achieving a low input noise density of 16.7 nV/$\sqrt{\text{Hz}}$. This stage sets the overall high-pass cutoff frequency to approximately 10 kHz. For all gain settings the high-pass cutoff frequency variation is within ±5%.

The low-pass channel filter is merged with a second amplifying stage forming a Sallen-Key structure. In order to maintain a constant transfer characteristic versus gain, the Sallen-Key feedback is taken from different taps of the load resistance. Using this new approach, the low-pass cutoff frequency stays between 440 kHz and 590 kHz for all gain settings (±14%). Finally, an offset cancelation loop reduces the output offset of the PGA to less than 5 mV (3σ).

The PGA occupies an area of approximately 0.06 mm^2 and achieves a post-layout power consumption of 55 μW from a 1V-supply. For the maximum gain setting the integrated input referred noise is 14.4 μV$_{\text{RMS}}$ while the total harmonic distortion is 0.7 % for a differential output amplitude of 0.5 V.

Keywords: Programmable gain amplifier, Sallen-Key filter, offset cancelation

1. INTRODUCTION

In wireless communication systems the receiver has to handle input signals with a wide dynamic range. Therefore, the input signals are usually equalized in their amplitudes using a programmable gain amplifier (PGA) to obtain a constant signal level for the demodulator.[1,2] Such PGAs are often combined with a preceeding filtering stage that prevent interferers from getting amplified too much. Also offsets have to been taken into account as they also can cause the amplifier output to saturate if the gain is large.

In this paper we present a PGA with channel filtering and offset cancelation for a direct conversion receiver for the Bluetooth low energy standard.[3] This standard uses frequency shift keying (FSK) with a modulation index of 0.5 at a data rate of 1 Mbps.[4] Therefore, an input signal with the bandwidth from 10 kHz to 500 kHz has to be amplified and filtered by the PGA.

In order to maximize the battery life time of the transceiver the power consumption of the PGA has to be kept as low as possible. The paper is organized as follows. Section 2 describes the architecture of the PGA while section 3 presents the proposed PGA in detail. Finally, in section 4 post-layout simulation results are presented and concluding remakrs are given in section 5.

Further author information:
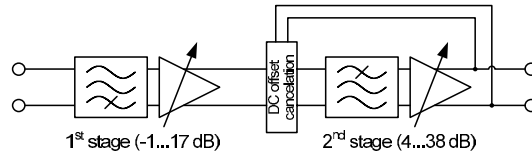E-mail: masuch@imse-cnm.csic.es, Telephone: +34 954 466 667
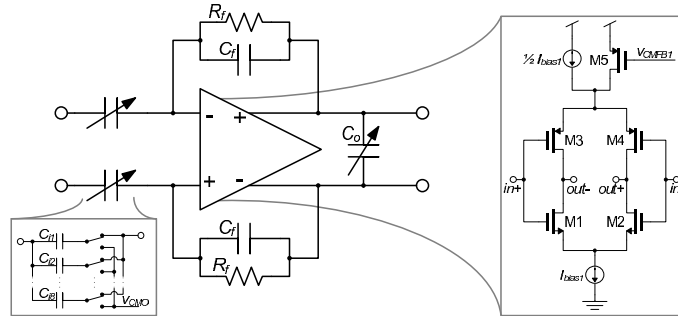
Figure 1. Architecture of the PGA

Figure 2. Simplified schematic of the first PGA stage

2. ARCHITECTURE

In order to obtain the required total gain of approximately 50 dB the PGA is splitted into two stages, as shown in Fig. 1. Cascading moderate gain stages together is a commonly used architecture.[5–9] This allows not only for independent optimization of the stages but also provides flexibility in the gain distribution. For example, the amplification of an input signal with a strong interferer can delayed to the second stage where the interferer is already filtered out. On the other hand, a signal without low interference level would be amplified as much as possible in the input stage to reduce the noise contribution of the following stages.

The first stage is optimized for low input noise and provides up to 17 dB amplification. This moderate amplification helps to keep the power consumption of this stage low. The AC coupled input of the first stage also sets the overall high-pass corner independent of the gain to approximately 10 kHz.

At the second stage a higher input noise level can be tolerated thanks to the the amplification of the first stage. Therefore, this stage is optimized for large amplification of up to 38 dB. In order to prevent adjacent channel interferers from being amplified by this stage and potentially causing linearity issues the 2nd order channel filter is placed at the input of the second stage. The channel filter sets the overall 3-dB corner frequency of the PGA to approximately 550 kHz.

The DC offset errors of both the first and second stage are canceled by means of an offset cancelation loop. This loop senses the overall output offset at the output of the PGA and corrects it at the DC coupling of the two stages. The offset cancelation loop adds a second zero in the transfer function of the overall PGA. Although this zero shifts with the amplification of the second stage it stays non-dominant for all gain settings.

3. CIRCUIT DESIGN

3.1 First stage

The first stage, shown in Fig 2, is based on capacitive feedback to set the amplification in the passband according to the capacitance ratio C_i/C_f. Programmability is obtained by implementing the input capacitance C_i as an array of 8 capacitances. Since all the capacitances $C_{i1...8}$ and C_f are identical metal-insulator-metal (MIM) capacitors, the voltage gain can be programmed in 6dB-steps from nominally 0 to 18 dB.

The feedback resistor R_f sets the high-pass corner frequency to 10 kHz independently of the gain because the feedback capacitance C_f is constant. On the other hand, the low-pass corner frequency of the first stage is kept at roughly 2 MHz by means of the variable output capacitance C_O. However, as this will be a non-dominant pole in the overall PGA the output capacitance is implemented as area-efficient MOS capacitors.

Table 1. Important component dimensions of the first PGA stage.

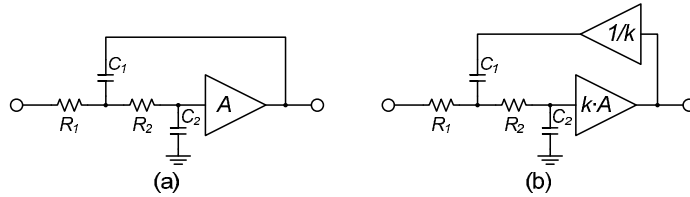| I_{bias1}	W/L M1, M2	W/L M3, M4	R_f	C_f	$C_{i1...8}$
10 μA	100/1 μm	100/0.4 μm	6 MΩ	2.4 pF	2.4 pF

Figure 3. Sallen-Key filter: (a) basic configuration with gain A, (b) configuration with variable gain $k \cdot A$

In order to achieve both low input noise and low power consumption the active part of the first stage is implemented as a complementary transconductance stage, shown in the inset of Fig 2. In this configuration the NMOS and PMOS transconductors re-use the same bias current and so reduce the input-refered noise by a factor of two.[10] Thanks to the low required output swing the gates of the NMOS and PMOS transistors M1/M3 and M2/M4 can be directly tied together.

3.2 Second stage

The second stage of the PGA also serves as the channel selection filter. A simple 2nd order low-pass filter with a 3dB corner frequency of 550 kHz is sufficient to meet the interference blocking requirements together with the non-dominant poles of the first stage and preceeding mixer output. The Sallen-Key filter is a commonly used filter structure because it offers a second order function with a single operational amplifier.[11] Figure 3(a) shows the basic single-ended structure of this filter with a fixed gain A. In order to use this structure with programmable gain we propose to compensate the programmabilty factor k using an attenuator in the feedback path, as shown in Fig. 3(b). Using this approach, the passives R_1, R_2, C_1 and C_2 do not have to be changed for different gain factors k which leads to a very constant corner frequency.

The circuit level implementation of this programmable gain filter in a fully differential configuration is shown in Fig 4 and the most important dimensions are summarized in Table 2. The programmable gain cell is based on a g_m-boosted differential pair with source degeneration.[12] In this configuration the gain is defined by the ratio of output resistor R_o to degeneration resistor R_d. The asymmetric mirrors M3/M5 and M4/M6 (ratio 4:1) allow to reduce the current in the output branches and the nominal gain of the second stage calculates as

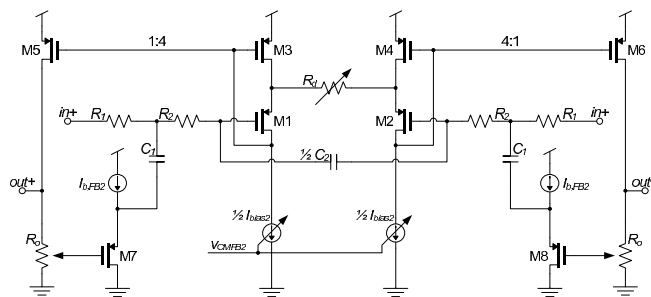$$A_{2nom} = \frac{R_L}{4R_d/2} = \frac{R_L}{2R_d}. \tag{1}$$

Figure 4. Simplified schematic of the second PGA stage

Table 2. Important component dimensions of the second PGA stage.

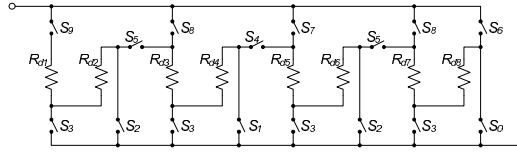| I_{bias2}	W/L M1, M2	R_o	R_1	R_2	C_1	$C_2/2$
10 μA	120/0.8 μm	400 kΩ	20 kΩ	10 kΩ	7 pF	3.7 pF

Figure 5. Implementation of the degeneration resistor R_d

The gain is programmed by switching the resistor R_d. As R_d is only connected to internal nodes of the amplifier both input and output nodes are hardly affected by the switching. This also helps to keep the poles of the transfer function constant. In order to obtain a large programming range of almost two orders of magnitude the degeneration resistor is implemented as shown in Fig. 5. The eight 12.5 kΩ unit resistors (R_{d1} to R_{d8}) can be connected in series or in parallel to each other using 16 PMOS switches. As a consequence the resulting degeneration resistance can vary from one eighth to eight times the unit resistance in logarithmic steps of a factor of 2. Table 3 shows the control signals corresponding to the different gain settings and the resulting degeneration resistance. Note that always at least 4 unit resistors are used in order to maintain good matching.

The output resistance R_o is constant for all gain settings and is implemented as a series connection 64 unit 6.25 kΩ resistors . Using this array of 64 resistors the compensation of the programmability factor in the feedback can be performed by tapping different internal nodes of the array. The tapped voltage is buffered by the source follower M7/M8 and appplied to the feedback capacitor of the Sallen-Key filter C_1.

3.3 DC offset cancelation

DC Offset cancelation (DOC) is inevitable in amplifier chains with a large total gain in order to prevent the output from saturating due to small input offsets. In the literature different strategies can be found such as local DOC around each stage in the chain[5, 13] or global DOC around various stages.[9, 14]

The most significant source of offset errors in the presented PGA is the second stage, namely the differential input pair, the current mirrors and the output resistors. The input refered offset can be as large as 2 mV (3σ) which would lead to a large error at the output at high gain. Due to the fact that no DC current can flow across the feedback resistor of the first stage R_f the output offset of this amplifier equals its input offset which is approximately 1 mV (3σ). Since at the interface of the two stages the offset errors are on the same order of magnitude they can be canceled here with a single compensation block that acts as a global DOC.

Table 3. Control signals and configuration of the degeneration resistor R_d for different second stage gain settings G_{stg2} ($S[x]{=}1$ refers to a closed switch).

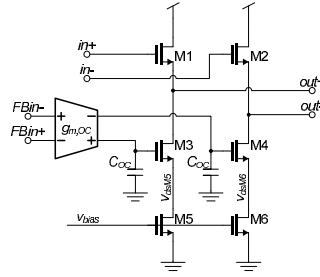| G_{stg2}	$S[9:0]$	R_d configuration	R_d	nominal gain A_{2nom}
0	1000 11 0001	$\sum R_{d1\ldots8}$	100 kΩ	6 dB
1	1000 10 0010	$\sum R_{d1\ldots4}$	50 kΩ	12 dB
2	1010 10 0011	$\sum R_{d1\ldots4}\|\sum R_{d5\ldots8}$	25 kΩ	18 dB
3	1010 00 0100	$\sum R_{d1/2}\|\sum R_{d5/6}$	12.5 kΩ	24 dB
4	1110 00 0111	$\sum R_{d1/2}\|\sum R_{d3/4}\|\sum R_{d5/6}\|\sum R_{d7/8}$	6.25 kΩ	30 dB
5	1110 00 1000	$R_{d1}\|R_{d3}\|R_{d5}\|R_{d7}$	3.125 kΩ	36 dB
6	1111 11 1000	$R_{d1}\|R_{d2}\|R_{d3}\|R_{d4}\|R_{d5}\|R_{d6}\|R_{d7}\|R_{d8}$	1.5625 kΩ	42 dB

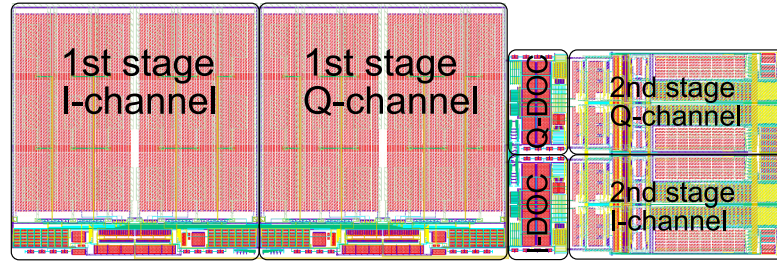Figure 6. DC offset cancelation block

Figure 7. Layout of the IQ-PGA (area shown is 0.6 mm by 0.2 mm)

The proposed compensation block is shown in Fig. 6. The NMOS source followers M1/M2 transfer the input to output with a gain slightly below unity and reduce the common mode voltage by the NMOS treshold voltage. The offset compensation of up to ±10 mV is done by unbalancing the bias currents of this source follower pair. This is achieved by operating the current sources M5/M6 at different drain voltages $v_{dsM5/6}$ through the cascode tansistors M3/M4. At the gates of the cascodes the output offset of the overall PGA is integrated by the transconductance $g_{m,OC}$ onto the capacitors $C_{OC1/2}$. A common mode control (not shown in Fig. 6) prevents that the cascode from cutting off the current sources.

4. POST-LAYOUT SIMULATION RESULTS

The two stage PGA has been implemented in a 0.13-μm CMOS technology with high-resistive Poly resistors and MIM-capacitors. As the PGA will be used in a direct donversion receiver the layout in Fig. 7 shows two identical PGAs for the I- and Q-paths. The total area occupation of the two PGAs is 0.12 mm^2 including the combinatorial logic to generate the control signals needed for gain programming. In order to reduce the occupied area the resistors and parts of the active circuitry have been placed below the MIM-capacitors.

The PGA has been simulated with extracted parasitics from the layout using a supply voltage of 1V±10%. The power consumption of the PGA is 55 μW including biasing and offset cancelation. Figure 8 shows the typical voltage gain of the PGA for all different gain settings. It can be observed that the bandwidth of the amplifier remains very constant while the in-band gain ranges varies from 4 dB to 55 dB. The attenuation of an interferer at 3 MHz offset is always at least 30 dB with respect to the pass-band.

In terms of noise performance the PGA achieves a spot noise of 16.7 nV/$\sqrt{\text{Hz}}$ at the maximum gain setting of 55 dB. For the intended output signal level of -6 dBV the signal-to-noise ratio is always larger than 35 dB. For the same output level setting the total harmonic distortion is less than -43 dB.

The output offset has been estimated to be within ±5 mV (3σ) using Monte-Carlo mismatch analysis with 200 runs. The most important parameters and simulation results are summarized in Table 4.

5. CONCLUSIONS

A low power two-stage PGA with a dynamic range of 51 dB and a step size of 6 dB has been presented. The first stage has been optimized for noise performance while the second one provides wide programmability. A
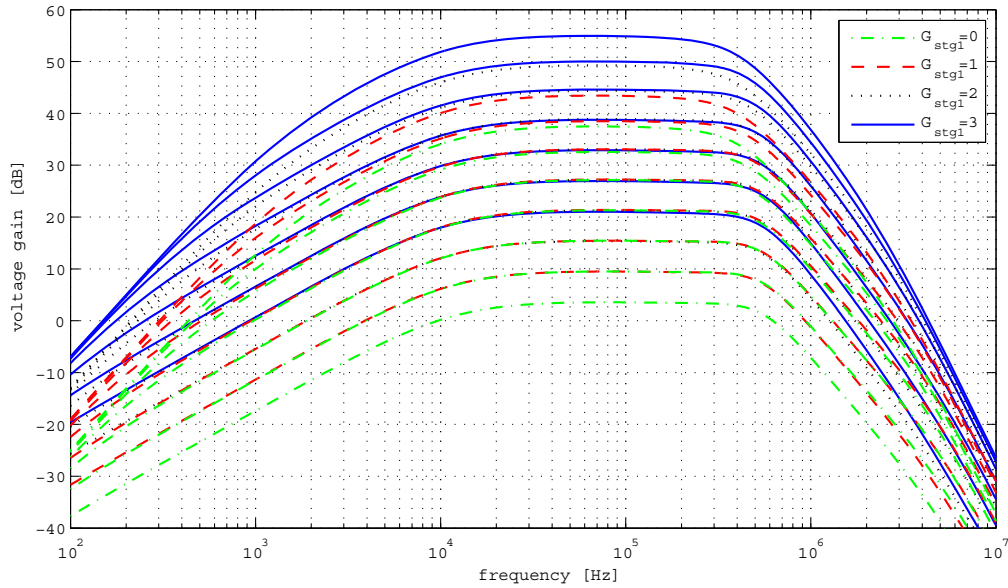
Figure 8. Voltage gain of the PGA for all possible gain settings

Table 4. Important design parameters and post-layout simulation results of the presented PGA

Parameter	Value
Process	0.13μm CMOS
Supply voltage	1.0 V
Power consumption	55 μW
Gain range	4–55 dB
Gain step size	6 dB
Bandwidth	10–550 kHz
Input refered noise @ max gain	16.7 nV/$\sqrt{\text{Hz}}$
Input refered integrated noise @ max gain	14.4 μV$_{\text{RMS}}$
Total harmonic distortion	<-43 dB
Occupied chip area	0.06 mm^2

constant bandwidth versus dynamic range is achieved using a Sallen-Key filter with gain compensation in the feedback path based on simple potentiometer tapping. The input-refered integrated noise voltage is 14.4 μV$_{\text{RMS}}$ and the output offset is kept below ±5 mV (3σ) by means of an offset cancelation loop.

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