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Algorithms and Circuits for Analog-Digital Hybrid Multibeam Arrays

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FLORIDA INTERNATIONAL UNIVERSITY

Miami, Florida

ALGORITHMS AND CIRCUITS FOR ANALOG-DIGITAL HYBRID
MULTIBEAM ARRAYS

A dissertation submitted in partial fulfillment of the
requirements for the degree of
DOCTOR OF PHILOSOPHY

in

ELECTRICAL AND COMPUTER ENGINEERING

by

Paboda Viduneth Ariyaratna, Beruwawela Pathiranage

2019

To: Dean John Volakis
College of Engineering and Computing

This dissertation, written by Paboda Viduneth Ariyaratna, Beruwawela Pathirana, and entitled Algorithms and Circuits for Analog-Digital Hybrid Multibeam Arrays, having been approved in respect to style and intellectual content, is referred to you for judgment.

We have read this dissertation and recommend that it be approved.

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Florida International University, 2019

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DEDICATION

To my dearest parents and loving wife...

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ABSTRACT OF THE DISSERTATION
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Paboda Viduneth Ariyaratna, Beruwawela Pathirana

Florida International University, 2019

Miami, Florida

Professor Arjuna Madanayake, Major Professor

Fifth generation (5G) and beyond wireless communication systems rely heavily on larger antenna arrays combined with beamforming to mitigate the high free-space path-loss that prevails in millimeter-wave (mmW) and above frequencies. Sharp beams that can support wide bandwidths are desired both at transmitter and the receiver to leverage the glut of bandwidth available at these frequency bands. Further, multiple simultaneous sharp beams are also imperative for such systems to exploit mmW/sub-THz wireless channels using multiple reflected paths simultaneously. Therefore, multibeam antenna arrays that can support wider bandwidths are a key enabler for 5G and beyond systems.

In general, N -beam systems using N -element antenna arrays will involve circuit complexities of the order of N^2 . This dissertation investigates new analog, digital and hybrid low complexity multibeam beamforming algorithms and circuits for reducing the associated high size, weight, and power (SWaP) in larger multibeam arrays. The research efforts on the digital beamforming aspect propose a new class of multibeam algorithms based on discrete Fourier transform (DFT) approximations that eliminate the need of digital multipliers in the beamforming circuitry. For this, 8-, 16- and 32-beam multiplierless multibeam algorithms have been proposed for uniform linear array applications. A 2.4 GHz 16-element array receiver setup and a

5.8 GHz 32-element array receiver system which use field programmable gate arrays (FPGAs) as digital backend have been built for real-time experimental verification of the digital multiplierless algorithms. The multiplierless algorithms have been experimentally verified by digitally measuring beams. It has been shown that the measured beams from the multiplierless algorithms are in well agreement with the exact counterpart algorithms.

Analog realizations of the proposed approximate DFT transforms have also been investigated leading to low-complex, high bandwidth circuits in CMOS. Further, a novel approach for reducing the circuit complexity of analog true-time delay (TTD) N -beam beamforming networks using N -element arrays has been proposed for wideband squint-free operation. A sparse factorization of the N -beam delay Vandermonde beamforming matrix is used to reduce the total amount of TTD elements that are needed for obtaining N number of beams in a wideband array. The wideband squint-free multibeam algorithm is also used to propose a new low-complexity hybrid beamforming architecture targeting future 5G mmW systems. Apart from that, the dissertation also explores multibeam beamforming architectures for uniform circular arrays (UCAs). An algorithm having $N \log N$ circuit complexity for simultaneous generation of N -beams in an N -element UCA is explored and verified.

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CHAPTER 1

INTRODUCTION

Wireless technologies have become heavily integrated to modern human lifestyles. The rapid development of wireless communication technologies have revolutionized the way people connect, share and access information and therefore, high-speed wireless connectivity today is an essential need. Moreover, the use of wireless technologies in the present day world extends beyond wireless communication systems to electronic warfare [5], tomography imaging [6], radio astronomy [7] to many more fields. All of these applications use different parts of the electromagnetic spectrum depending on the particular requirements of each application. Directional reception and/or transmission of electromagnetic waves which is also known as beamforming [8] is one of the critical requirements for most of these applications. Beamforming is considered a vital part of many wireless applications such as phased-array radar [5], which is to electronically scan, sense, detect and track targets; radio astronomy applications such as wide-field synthesis imaging [7], time-domain pulsar astrometry [9]; and more importantly in wireless communication for massive multiple-input multiple-output (MIMO) [10,11] and emerging 5G technologies [12,13] as well as for various other scientific activities such as study of ionosphere, weather, and deep space communications. With the advent of 5G and beyond 5G wireless communication networks, beamforming has drawn a great deal of attention. High gain antenna arrays that can form multiple beams are required in order to utilize the complex urban wireless channels that suffer from occlusions, path loss, and multipath effects [12,14] at these frequencies. In fact, beamforming in large arrays and the ability to form multiple simultaneous beams are key enabling technologies for millimeter wave (mmW)/sub-THz/THz communication systems [15]. Further, with the emerging mmW wireless technologies, applications relevant to defense systems

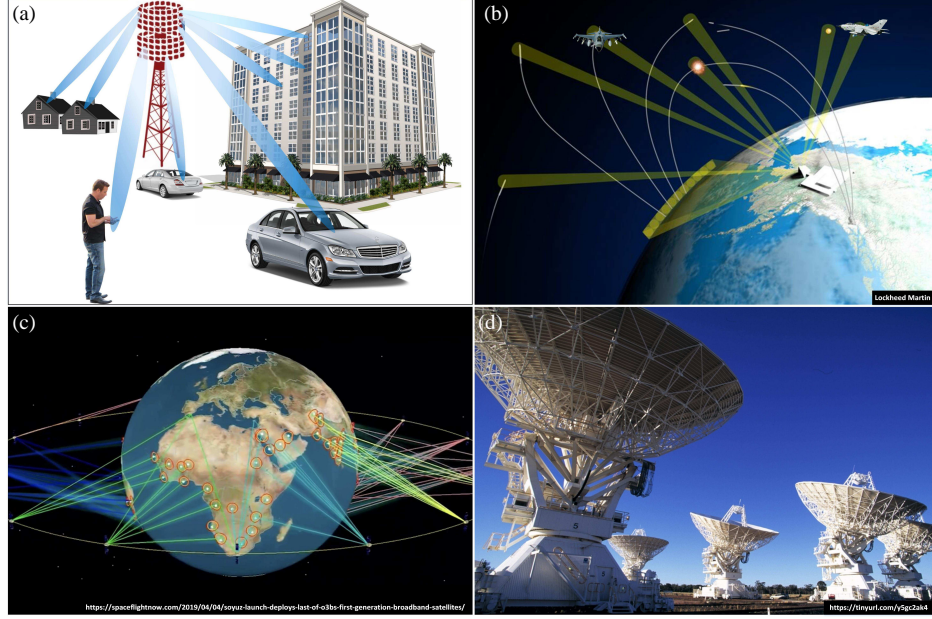


Figure 1.1: Applications of multibeam beamforming; (a) 5G wireless communication environment; (b) electronic warfare; (c) satellite based Internet access; (d) radio astronomy.

are flourishing, such as space-based mesh networks between low earth orbit satellites, cross-platform high-capacity data connectivity (air, space, land, and sea) and electronic warfare. As illustrated in Fig. 1.1, all these applications demand multi-beam beamforming networks that can deliver a massive number of high bandwidth beams. Recently, Defense Advanced Research Project Agency (DARPA) has also called a separate program that aims to create multi-beam networks at 18-50 GHz band to enhance secure communications between military platforms [16].

1.1 Motivation

Wireless communication has been one of the most vibrant and rapidly growing areas in the field of communication. A high surge in research activities has occurred in the past few decades in the area of wireless communication with advances in very-large-scale integration (VLSI) technologies that has enabled ultra high-speed data communication rates [17]. However, with the escalating growth in the use of smart-

phones and the demand for data services such as high-quality, low latency video and multimedia applications in the last decade have created enormous challenges in wireless systems due to the scarcity of bandwidth to cater to the ever increasing demands of data rates. All the mobile generations up to fourth generation (4G) mobile networks have been limited to carrier frequencies of sub-6 GHz range; thus, these networks have been facing global shortage of bandwidth, which is needed to cater the increasing demand of data rates due to the spectral crowding in the sub-6 GHz spectrum. This situation has motivated the exploration of mmW frequency spectrum, which is fairly under utilized, for future 5G wireless communication networks. As correctly pointed out in [12] back in 2013, mmW-enabled mobile communication is now at the verge of becoming reality: the initial commercial deployments are underway at the time of the writing of this dissertation.

Communication at mmW promises an unprecedented change in the wireless industry, where the wireless industry will move from today's scarcity of spectrum to a glut of spectrum. The spectrum above 6 GHz all the way up to sub-THz and THz frequencies brings in massive amount of spectral resources that can be leveraged in mobile communication towards an exponential increase in capacity and data rates with compared to today's systems. Channel capacity C as given by Shannon's law is expressed in (1.1).

$$C = \log_2(1 + SNR) \text{ bits/s/Hz.} \quad (1.1)$$

Dynamic spectral access (DSA), cognitive radio (CR) technologies, and full-duplex systems can yield improved capacity, but they do not provide an exponential increase in capacity. According to (1.1), the only method to achieve an exponential increase in the capacity is to have an exponential increase in the system bandwidth. The

exploration of the huge amount of spectrum available above 6 GHz can accommodate such increments [18–23].

The mmW communication channel encompasses a completely new radio propagation environment compared to sub-6 GHz radios as of today and, thus, would need completely redesigned transceiver front-end designs for the faster talking nodes. At mmW, most objects encountered are much larger than its wavelength and thus the mmW bands are dominated by occlusion effects from unpredictable obstructions (vehicles, people, buildings, etc.) as opposed to diffraction effects that dominate sub-6 GHz channels, as shown in Fig. 1.2(a). The other main challenge is the higher free-space path loss (FSPL) experienced by the signals at the mmW frequencies. As indicated by the Friis’s FSPL equation in (1.2), the received power P_r at a propagation distance d is given by

$$P_r = \frac{P_t G_t}{4\pi d^2} A_{eff} = \frac{P_t G_t G_r}{L} \left(\frac{\lambda}{4\pi d^2} \right)^2, \quad (1.2)$$

where P_t is the transmitted power; A_{eff} is the effective antenna aperture and G_t , G_r gain of the transmitting antenna and the receiving antenna, respectively; and where L is a loss factor accounting for the efficiencies of the antennas which is greater than one. As (1.2) implies, for the same distant d , the path loss increases with the frequency since A_{eff} becomes smaller as the frequency increases.

On the other hand, the maximum gain of any antenna is related to its effective area A_{eff} and the operating frequency as shown in [24]:

$$G_{max} = A_{eff} \left(\frac{4\pi}{\lambda^2} \right). \quad (1.3)$$

Because frequencies at the mmW region and beyond will lead to smaller wavelengths, the use of these frequencies would permit more antennas to be fitted into a smaller form factor. If the maximum length dimension of the antenna at a frequency corresponding to λ is D , then $G_{max} \propto D^2$. Therefore, as implied by (1.3),

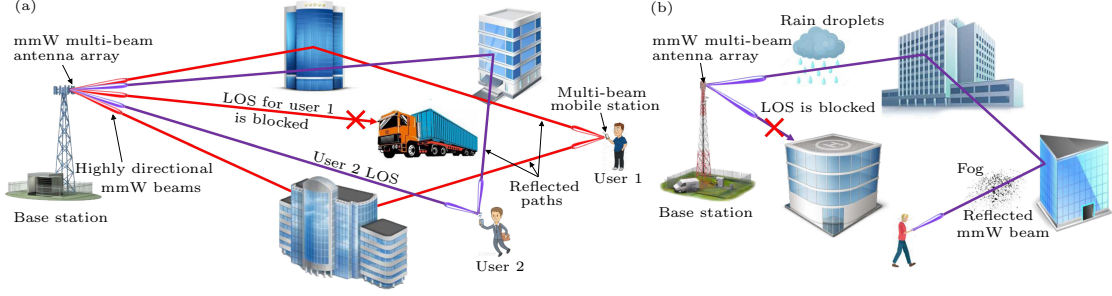


Figure 1.2: Examples of highly directional beam-like propagation in mmW wireless channels, which can suffer from obstructions in dynamically changing mobile environments and how the use of multi-beam arrays can overcome such scenarios.

using N -element antenna arrays with larger N , the antenna gain can be increased in the order of N^2 . The key here is to have more antenna elements in the array to maintain a constant aperture size with the increase of frequency. This can be seen as the only way to compensate for the high FSPL at these frequency. The situation can be improved by using higher gain antenna arrays at both the transmitter and the receiver which can in fact overcome the distance-dependent propagation path loss. Therefore, exploiting high gain steerable antennas enabled by beamforming technologies is a key aspect of future communication systems that use frequencies mmW and beyond [17].

In addition, with the use of high gain antenna arrays that can produce sharp beams, mmW channel can benefit from the environment to bounce energy off the objects by using different beams to form communication links. Such a scenario is illustrated in Fig. 1.2. Communication at these frequencies can also benefit from simultaneous beams in different directions to utilize the channel to send multiple streams in parallel to increase capacity [14, 17, 25]. Fig. 1.2 shows such a scenario, where multiple simultaneous beams use spatial multiplexing to serve different users. Thus, high gain multiple simultaneous beams will be the key in overcoming the 5G mmW channels. Moreover, large multibeam systems are beneficial by the 5G base

stations to reduce the time in best beam pair search [26] between the base station and the user. These aspects make a beamformer which can produce orthogonal multibeam a great candidate for 5G systems [27]. For these reasons, a large portion of work in this dissertation is directed towards reducing the associated hardware complexity in N -element arrays that can produce N orthogonal simultaneous beams.

Multibeam beamforming has many other applications apart from 5G and mmW systems in legacy sub-6 GHz arrays for MIMO communication. In [28] it has been shown that the pre-beamforming matrix for large ULAs can be set by blocks of columns of a unitary discrete Fourier transform (DFT) matrix for a joint spatial division and multiplexing (JSDM) scenario, which is a method to achieve multiuser MIMO downlinks by exploiting the structure of the channel correlations. The paper shows that for ULAs, a DFT-based pre-beamforming matrix is near-optimal, requiring only coarse information about the users' angles of arrival and angular spread [28]. It is further shown that the DFT pre-beamforming achieves very good performance in the absence of accurate estimation of the actual channel covariance matrix. The above fact also justifies research efforts (described in Chapters 3 and 4) to enable fully digital beamforming having orthogonal beams at much lower hardware complexity. Multibeam radars are also used for scanning through different directions at the same time and tracking multiple targets simultaneously [29, 30]. The radio astronomy community also uses multibeam-based scanning in specific radio telescopes with arrays of sensors [31, 32].

Although having a high number of simultaneous multibeam is advantageous, linear arrays that employ N -sensor elements demand an $\mathcal{O}(N^2)$ order of circuit complexity to enable beamforming that preserves full degrees of freedom for the array. For rectangular apertures, the circuit complexity of the beamforming networks (that does not eliminate spatial degrees of freedom) grows as $\mathcal{O}(N^3)$. Therefore,

the associated circuit complexity and power consumption are a limiting factor for realizing such massive MIMO networks. The work summarized in this dissertation address the associated huge complexity problem of such N -beam networks for larger array sizes in terms of algorithmic and circuit-level novelties. The research efforts are aimed towards exploring low-complexity implementations of multibeam arrays, targeting both analog and digital beamforming networks. The proposed research work also address the problem of achieving low-complexity wideband N -beam systems, eliminating the problem of beam squint and the resulting negative impacts on the wideband analog beamforming systems.

1.2 Contributions of this Dissertation

Future 5G and beyond wireless systems which will operate on the carrier frequencies ranging from mmW to THz frequencies will heavily depend on large beamforming antenna arrays that can generate multiple simultaneous beams that are narrow and supporting higher bandwidths. The aim of this dissertation is to explore algorithms and circuits that will enable low-complexity realizations of future mmW and THz sensor arrays. The specific algorithmic and implementation research contributions towards reducing the complexity of multibeam array synthesis are described below.

1. Fully digital multibeam beamformers based on approximate DFTs have been proposed for low-size-weight-power-and-cost (SWaPC) digital implementations. Narrowband orthogonal multibeam in theory can be achieved by employing a spatial DFT operation across a ULA antenna samples in receive-mode. The approximate DFT algorithms of 8- and 16-point sizes that are proposed for digital multibeam apertures are multiplierless and can be implemented using adder only digital circuits. The algorithms have been further

factorized to reduce the number of adders through the use of butterfly stages. The theoretical performance of the beams generated from the approximate discrete Fourier transforms (ADFTs) have been quantified and all beams fall exactly on top of the exact fast Fourier transform (FFT)'s beams unless there is a small (less than 2 dB) hit in the sidelobe performance. The proposed multi-beam algorithms have been implemented in digital. The hardware resource utilization has been compared against the corresponding fixed-point FFT implementations. A real-time 16-element antenna array setup that works at 2.4 GHz along with field-programmable gate array (FPGA) back-end for digital signal processing (DSP) has been built to experimentally verify the beams. The beams generated by the proposed low-complexity algorithms have been measured in an anechoic chamber and have been compared with the exact FFT-generated beams to verify that the ADFT-based multibeam beamformers can be used in place of the FFT-based multi beamformers in multibeam arrays.

2. A 32-beam low-complexity algorithm based on a 32-point ADFT has also been proposed and experimentally verified. The 32-beam system has been implemented using a 5.8 GHz 32-element antenna front-end with the aid of a Reconfigurable Open Architecture Computing Hardware Rev. 2 (ROACH-2) FPGA processing platform. The use of ADFT algorithms towards drastically reducing the complexity of 2D multibeam arrays has also been investigated. The proposed ADFT algorithms can be implemented without using multipliers and therefore, 2D DFT based multibeam apertures can be replaced with the ADFT digital cores to compute multibeam in digital implementations. An analysis was conducted to obtain beam patterns arising from a 32×32 array, which will produce ≈ 1024 simultaneous beams using the 32-point ADFT as

a building block. The actual 2D RF beams that would be generated in such a 32×32 system have been synthesized in simulation using the measured beams from the 1D 32-beam system.

3. A fully digital 4-beam beamformer using a 4-element array at 28 GHz has been implemented. The digital multibeam beamforming is accomplished using Xilinx radio-frequency system-on-chip (RFSoc) platform that can support 2 GSps sampling of 16 analog input channels. The digital beamforming supports 845 MHz of bandwidth and is performed in a polyphase manner. This is the first 28 GHz based fully digital beamforming system that has been reported that is capable of supporting a bandwidth over 800 MHz. Novel polyphase circuits have been proposed for calibration of the front-end in a polyphase sampling architecture.
4. The use of the same ADFT algorithms has been proposed for analog multi-beam realizations. Since the proposed ADFT matrices and their sparse factorization have small integer coefficients ($\{\pm 2, \pm 1, 0\}$), these matrices can be easily mapped to current-mode circuits in analog CMOS to realize circuits that approximates the DFT operation in continuous time. The matrix coefficients can be realized using simple current mirror circuits; thus, the overall circuit will have a much larger bandwidth compared to corresponding digital realizations. Analog DFT-based CMOS circuits are proposed for receive-mode and transmit-mode beamformers targeting high bandwidth operation. A novel approach is proposed to utilize the ADFT factorization in implementing the analog ADFT such that the overall current mirrors required for the entire circuit will be reduced to the order of N from N^2 , where N is the number of elements in the antenna array, saving circuit area and static power. A CMOS schematic level design has been designed in Cadence using 65-nm CMOS mod-

els and the circuits have been simulated and analyzed to verify the proposed methodology. A comprehensive analysis of the total power consumption of the proposed circuit was conducted and compared against the digital counterpart implementation to verify that the proposed analog multibeam circuits are power-efficient.

5. A novel methodology for obtaining wideband squint-free analog beams is proposed based on the factorization of the delay Vandermonde matrix (DVM). The proposed method reduces the number of TTD elements needed in analog wideband multibeam networks. The proposed method has been verified using measured all-pass filter (APF) response for an s-band array. It has been shown that for a 4-element array, the required number of APF blocks will be reduced by 60%; for an 8-element array, the percentage saving would be $\approx 78\%$. The proposed method is extended to adapt for the wideband analog IF/baseband beamforming case where the analog circuit complexity is reduced by the same percentage as in the RF case. A new hybrid beamforming architecture is also proposed using the DVM as the first level analog beamforming. A novel low-complexity wideband digital beamforming scheme based on Thiran APFs is also proposed for level-2 digital beamforming. The Thiran APF is an finite impulse response (IIR) filter that can generate the required TTD with much lower complexity (multipliers) than finite impulse response (FIR) implementations.
6. A novel low-complexity method for generating circular multi-beam that are steerable has also been proposed. A conventional approach that produces N narrowband beams in an N -element uniform circular array (UCA) would need N^2 order of multiplier complexity in the digital beamforming network. The proposed method achieves equi-spaced circular beams at a complexity

of order $N \log N$ by exploiting the circulant structure of the beamforming matrix. A new method for eliminating the mutual coupling in UCAs is also proposed. The proposed method also exploits the circulant structure of the coupling matrix of a UCA. It has also been shown that the elimination of mutual coupling can be achieved simultaneously with the circular multibeam generation without any increased complexity.

1.3 Publications

The research outcomes from this dissertation have been reported through five journal publications and twelve conference papers, which are included in the vita at the end of the dissertation.

1.4 Dissertation Outline

The remaining portion of the dissertation is organized as follows:

Chapter 2 presents a comprehensive review of multi-dimensional (MD) signal processing in view of space-time filters, including the spectral properties of the propagating electromagnetic (EM) plane-waves sampled in space. Section 2.1 reviews the mathematical representations of the propagating EM plane-waves in the 3D space and Sections 2.2 and 2.3 review the spectral properties of spatio-temporal (ST) plane waves (PWs) received by planar and linear arrays. The discussion in Section 2.4 introduces how the spectral properties of the spatially sampled waves are used to derive directional enhancement of signals, thereby leading to the discussion of beamforming topologies and techniques in Section 2.5. Section 2.6 reviews

the basics of multibeam realization and provides an overview of the implementation topologies.

Chapter 3 presents the work on producing low-complexity digital multibeam. A review of fully digital beamforming and its benefits are discussed in Section 3.1. The theory behind spatial DFT based multibeam generation is described in Section 3.2. In Section 3.3, different implementation methods for discrete transforms that are found in the literature are discussed. Section 3.4 describes a theoretical overview of the proposed DFT approximations for digital multibeam beamforming. An 8-point and a 16-point DFT approximation are introduced, targeting an 8-element and a 16-element radio-frequency (RF) aperture to achieve multiple simultaneous beams. The proposed ADFTs are compared to the exact DFT (ideal case) and are explored to evaluate the performance for RF beamforming applications. Section 3.6 describes the digital hardware implementation and the microwave setup for realizing the RF front-ends and antenna array for experimentally verifying the beams. In Section 3.6.4, anechoic chamber beam measurements are presented and compared to the beams from an ideal DFT.

Chapter 4 details the work on the multiplierless simultaneous 32-beam algorithm and its digital implementation using a 32-element array receiver at 5.8 GHz to realize a 1024-beam digital array. Section 4.3 presents the 32-beam low-complexity digital algorithm and its sparse factorization towards low-complexity multiplierless implementation of a 32-beam digital core. In Section 4.4 the details of the 5.8 GHz 32-element digital array receiver is given. Section 4.5 presents the 32-beam real-time beam measurements for the proposed algorithm and the fixed-point FFT counterpart. The Section also presents the synthesized 2D beams from the 32-beam linear array beam measurements at 5.8 GHz that would correspond to an equivalent 2D array made of similar 32, 32-element subarrays.

Chapter 5 describes work on a 4-element digital beamforming array at 28 GHz that supports 800 MHz of baseband bandwidth. Section 5.1 describes the details of the 28 GHz receiver array design starting from the antenna to the individual receiver chain. Section 5.2 describes the Xilinx RFSoc based high speed high bandwidth digital processing back-end. The Section also provides the details of the polyphase circuit architectures for beamforming the entire 800 MHz bandwidth. Section 5.3 details the 28 GHz real-time beam measuring setup and presents the experimental procedure along with the measured beam responses.

Chapter 6 discusses a novel method for realizing analog multibeam networks using the ADFT algorithms proposed in Chapters 3 and 4. Sections 6.1 and 6.2 discuss the RF system considerations and the need for analog multibeam beamforming front-ends in future mmW transceivers, emphasizing the need for low-power, energy-efficient multibeam solutions for mobile devices. Section 6.3 proposes the use of the sparse factorization stages of the ADFT algorithms to map them into analog current mirror-based CMOS circuits to low-complexity energy efficient multibeam circuit implementations. The Section also presents the schematic based CMOS (using the Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm process design kit (PDK)) designs proposed for realizing the 16-beam circuit that uses the 16-point ADFT algorithm. The simulated beam responses from the Cadence simulation are given in the same Section. Section 6.4 conducts a comparison of the metrics of the analog implementation and the corresponding digital implementation to prove that the proposed analog circuits are energy-efficient and feasible for future implementations.

In Chapter 7, a novel squint-free wideband beamforming architecture is proposed. The Sections 7.1 and 7.2 discuss the problem of beam squint in wideband beamforming and briefly describes how the conventional Butler matrix type analog

multibeam networks suffer from beam squint. In Section 7.3, an analog multibeam beamforming network model that does not suffer from beamforming is introduced, leading to the novel N -beam wideband beamforming algorithm described in Section 7.4. As a proof of concept of the proposed algorithm, Sections 7.5 and 7.6 present the circuit architectures and simulation verification of the proposed algorithm for a 4-beam network. Section 7.7 extends the algorithms in Section 7.4 for implementations in IF and Section 7.8 provides simulated verifications for proposed concepts.

The novel hybrid beamforming architecture is proposed for squint-free wideband beamforming in Chapter 8 using the analog algorithm proposed in Chapter 7 targeting mmW systems. The overall architecture of the proposed hybrid beamformer is discussed in Section 8.2. Section 8.3 discusses the level-1 beamforming simulated responses of the beamformer using a 28 GHz APF circuit response. Section 8.4 presents the level-2 wideband digital beamforming architecture proposed using low-complexity Thiran APFs along with the corresponding simulated hybrid array factors for the proposed architecture.

A new algorithm for generating circular symmetric multibeam using a circular geometrical array is proposed in Chapter 9. A brief review of beam synthesis in circular arrays is provided in Section 9.1. The proposed N -beam circular array processing system is then discussed in Section 9.2. The digital hardware realization architectures are also presented for realizing the proposed algorithm in Section 9.3, and the simulated verifications are given in Section 9.4. Moreover, a novel method is proposed to eliminate of the mutual coupling effect on the receive mode in Section 9.6, and it is further shown how the mutual coupling and uncoupling can be simultaneously achieved in the multibeam realization without any added complexity.

Finally, Chapter 10 summarizes all the research work carried out in this dissertation with the insights that can be gleaned from the conducted research.

1.5 Scientific Collaborators

The work performed in the research study of this dissertation was carried out with multiple collaborations. The work described in Chapters 3, 4 and 6 were mainly conducted in collaboration with Dr. Renato J. Cintra at Federal University of Pernambuco (UPFE) in Brazil and his student, Diego Coelho at the University of Calgary for the approximate matrix search part. Dr. Sirani Perera at Embry Riddle Aeronautical University collaborated for the work described in Chapters 7 and 8 by deriving the mathematical proofs for the proposed algorithms. Dr. Soumyajit Mandal from Case Western Reserve University Cleveland collaborated in several publications that were done around the work presented in Chapters 4, 6 and 7. Further, Dr. Leonid Belostotski from the University of Calgary, Canada collaborated in the work done related to analog beamformers in Chapters 6 and 7. Dr. Ted S. Rappaport at NYU WIRELESS, New York University also collaborated in several publications that were resulted in the works associated with Chapters 6, 4, and 5.

CHAPTER 2

REVIEW OF RF BEAMFORMING THEORY AND TECHNIQUES

This chapter presents a review the multi-dimensional perspective of propagating planar waves and their spectra as seen by the planar or linear antenna arrays in beamforming receivers. The concepts presented here will lay the platform for the discussion leading to beamforming and the generation of multiple simultaneous beams, which is the focus of this dissertation. Although the discussion is presented in the perspective of the receiver, the concepts and theories will be reciprocal to the transmit side as well.

2.1 Free Space Propagation of EM Waves

As illustrated in Fig. 2.1, the propagating electromagnetic waves can be considered to be approximately planar in the far-field. Far-field is generally considered to be at a distant d from the transmitter, where $d > 2D^2/\lambda$, where λ is the wavelength of the wave in the propagating medium, and where D is the aperture of the radiating antenna [33, p. 42]. Such a propagating wave is a four-dimensional (4D) spatio-temporal or a multi-dimensional signal that has a temporal dependence with one or more spatial dimensions over a finite region.

The transverse electric field or magnetic field of such far-field EM PWs in three-dimensional (3D) space $\{x, y, z\} \in \mathbb{R}^3$ can be represented in continuous domain as a 4D function in the form,

$$pw_{4D}(x, y, z, t) = s_{pw}(ct + d_x x + d_y y + d_z z), \quad (2.1)$$

where $\hat{\mathbf{d}} = [d_x \ d_y \ d_z]^\top$ is the unit vector that denotes the DoA of the signal in 3D space, c is the wave propagation speed, $t \in \mathbb{R}$ is the time, and $s_{pw}(\lambda), \forall \lambda = ct + d_x x + d_y y + d_z z \in \mathbb{R}$ is the function that defines the one-dimensional (1D)

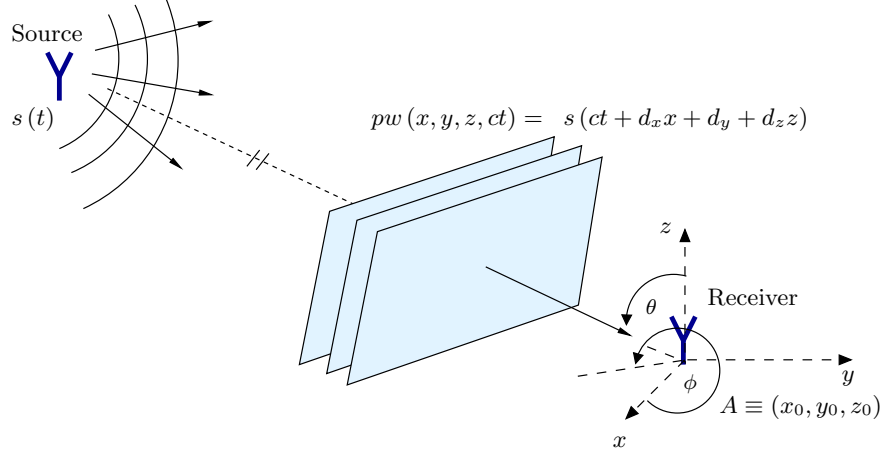


Figure 2.1: Signals emanated from a source can be treated as plane waves in the far-field.

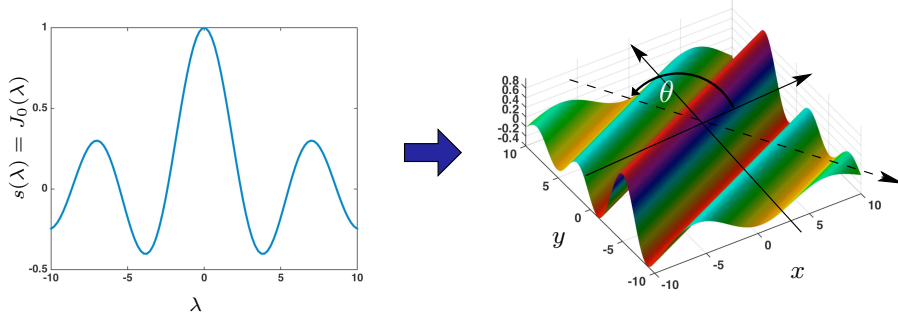


Figure 2.2: 2D temporal snapshot of the 3D plane wave function created using 1D to 3D mapping.

temporal signal (here, λ is merely a parameter and is not related to the wavelength of the signal). For each value of λ , $s(\lambda)$ corresponds to a 4D iso-surface in $\{x, y, z, ct\}$. Since vector $\hat{\mathbf{d}}$ denotes a unit vector, $d_x^2 + d_y^2 + d_z^2 = 1$. The unit vector $\hat{\mathbf{d}}$ can be expressed in terms of the elevation $\theta \in [0, \pi]$ and azimuthal angle $\phi \in [0, 2\pi]$ as

$$\hat{\mathbf{d}} \equiv [d_x \ d_y \ d_z]^\top = [\sin(\theta) \cos(\phi) \ \sin(\theta) \sin(\phi) \ \cos(\theta)]^\top. \quad (2.2)$$

For convenience, this discussion is limited to waves that represent the electric field or the magnetic field of the propagating waves by (2.1) on planar surfaces and straight lines.

For example, a waveform $s(\lambda)$ can be mapped as a 3D function using the parameterization $\lambda = g(x, y, ct)$, where $s(\lambda)$ is a 1D function, and $g(\cdot)$ defines the parametric relationship of $\{x, y, ct\}$. Fig. 2.2 shows a snapshot of a simulated plane wave in x - y 2D plane, propagating at an angle of ϕ to the x -axis, obtained using the parametric mapping $\lambda = x \cos \phi + y \sin \phi + ct$ in the 1D function $J_0(\lambda)$. The function $J_0(\cdot)$ here is the Bessel function of the first kind, which has been arbitrarily chosen for the illustration. The above mapping is the 2D version of (2.1) that can be obtained by setting $\theta = \pi/2$ in (2.2).

The ST PW signals received in a planar region can be expressed as in (2.3) by setting $z = 0$ in (2.1) without loss of generality.

$$pw_{3D}(x, y, t) = s_{pw}(d_x x + d_y y + ct). \quad (2.3)$$

Therefore, the 4D hyper planar iso-surfaces of constant λ in expression (2.1) simplify to 3D iso-planes for the case in (2.3) where the orientation of such iso-planes with respect to the ct axis will be given by the relationship $x \sin \theta \cos \phi + y \sin \theta \sin \phi + ct = \lambda$. In the 2D case, for which the signals are received in the x -axis (without loss of generality), constant λ surfaces become 2D iso-lines in $\{x, ct\} \in \mathbb{R}^2$ as given in (2.4).

$$pw_{2D}(x, ct) = s_{pw}(x \sin \theta \cos \phi + ct). \quad (2.4)$$

If the 2D ST PW is viewed in the x - y plane (making $\theta = \pi/2$), then the above relationship can be expressed as $pw_{2D}(x, ct) = s_{pw}(x \cos \phi + ct)$. For convenience, if the spatial DoA the ST PW is defined with respect to the y -axis as shown in Fig. 2.3(a), then the relationship in (2.4) can be rewritten w.r.t ψ as $pw_{2D}(x, ct) = s_{pw}(-x \sin \psi + ct)$. Thus, now the apparent DoA in space-time becomes ϑ , where ϑ is given by (2.5).

$$\vartheta = \tan^{-1}(\sin \psi). \quad (2.5)$$

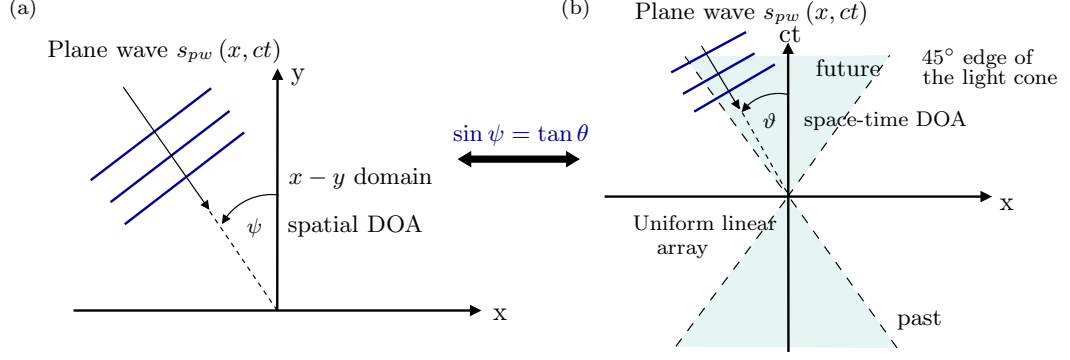


Figure 2.3: (a) Plane wave received on the x -axis; (b) the 2D spatio-temporal DoA in the $\{x, ct\}$ domain.

As illustrated in Fig. 2.3(b), the angle ϑ is constrained to $[-\pi/4, \pi/4]$ in the $x - ct$ domain where $|\vartheta|$ is maximum when $\psi = \pm\pi/2$ (i.e., $\phi = 0, \pi$ and $\theta = \pi/2$).

2.2 Spectral Properties of 2D/3D Spatio-Temporal PWs

Since the focus of this dissertation is limited to planar and linear arrays, this section will describe the analysis of the spectral properties of 2D/3D PW signals. The analysis will first be conducted on the continuous-domain (CD) case. In practical array processing and multi-dimensional signal processing applications, the signals encountered are spatially discretized signals where the temporal domain can be either continuous or discrete. This is because the spatial sampling of the signals is achieved using antennas that have a finite aperture size.

The general spectral properties of a 4D wave function can be analyzed by taking the 4D continuous-domain Fourier transform (FT) (CDFT) of (2.1). Equation (2.6) defines the 4D CDFT for the generalized 4D plane wave function

$$PW_{4D}(\Omega_x, \Omega_y, \Omega_z, \Omega_{ct}) \triangleq \int_{x,y,z,ct=-\infty}^{+\infty} pw_{4D}(x, y, z, ct) e^{-j(\Omega_x x + \Omega_y y + \Omega_z z + \Omega_{ct} ct)} dx dy dz dct, \quad (2.6)$$

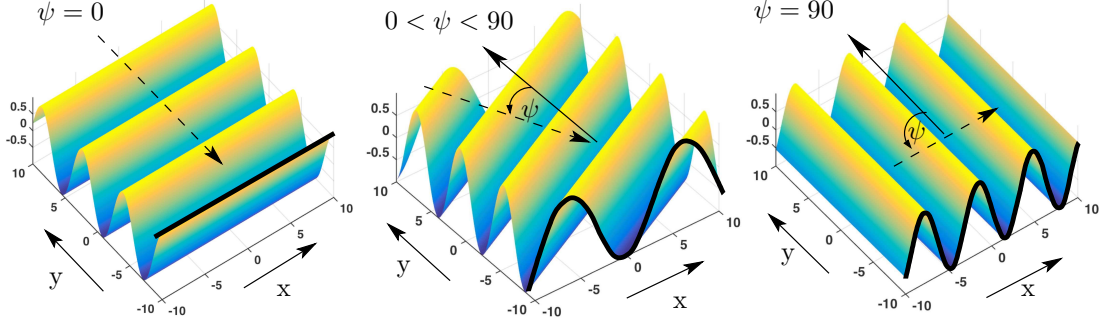


Figure 2.4: Different spatial frequencies observed by x -axis for a sinusoidal wave front impinging from different directions.

where $(\Omega_x, \Omega_y, \Omega_z, \Omega_{ct}) \in \mathbb{R}^4$ and $\Omega_k = 2\pi f_k$, $k \in \{x, y, z, ct\}$ are the angular frequencies with respect to each variable, and $f_{ct} = f_t/c$ (here, f_t denotes the temporal frequency of the signal). Fig. 2.4 provides an illustration to visualize the concept of spatial frequency and its relevance in beamforming. A 2D sinusoidal ST PW that is being received on the x -axis with different DoAs is depicted in Fig. 2.4. It can be seen that different DoAs results in different spatial frequencies to appear at the x -axis, giving rise to different Ω_x values. Therefore, the spectra of an impinging ST PW will be localized to a certain region in the MD frequency domain, depending on the directionality of the impinging ST PW. This is the basic phenomenon that is exploited in beamforming, which can be thought of as spatial filtering.

A detailed evaluation of the (2.6) can be found in [34] and, as shown in [34], the 4D CDF of $pw_{4D}(x, y, z, ct)$, $PW_{4D}(\Omega_x, \Omega_y, \Omega_z, \Omega_{ct})$ can be simplified to the expression given in (2.7),

$$PW_{4D}(\Omega_x, \Omega_y, \Omega_z, \Omega_{ct}) = S_{pw}c\Omega_{ct} \cdot \delta(d_x\Omega_{ct} - \Omega_x) \cdot \delta(d_y\Omega_{ct} - \Omega_y) \cdot \delta(d_z\Omega_{ct} - \Omega_z), \quad (2.7)$$

where $S_{pw}(\Omega_t)$ is the 1D continuous-time (CT) FT of the temporal signal $s_{pw}(t)$; i.e. $s_{pw}(t) \xrightarrow{\mathcal{F}} S_{pw}(\Omega_t)$. The function $\delta(\cdot)$ denotes the CD impulse function. According to (2.7), it can be seen that the region of support (RoS) of the spectrum of the PW

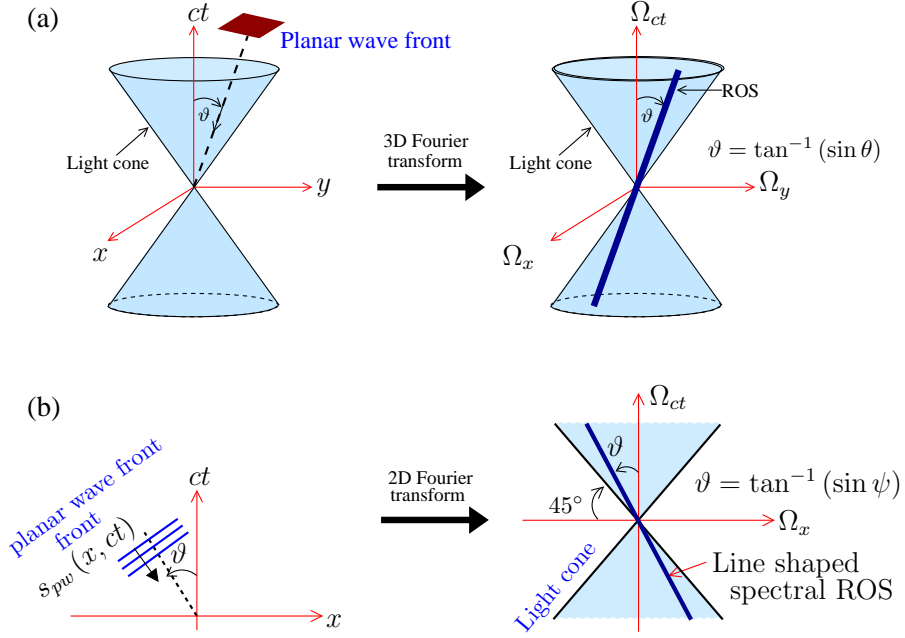


Figure 2.5: (a) The RoS of a 3D ST PW received by a planar surface in 3D space ($z = 0$) and its corresponding RoS in the 3D frequency domain; (b) the RoS of a 2D ST PW received by a line in 3D space ($z = 0$, $y = 0$).

is confined to a 4D hyper-line generated by the intersection of three 4D hyper-planes described by $d_x \Omega_{ct} - \Omega_x = 0$, $d_y \Omega_{ct} - \Omega_y = 0$, and $d_z \Omega_{ct} - \Omega_z = 0$.

For the specific cases that is of interest in this chapter, the 3D and 2D Fourier domain functions PW_{3D} and PW_{2D} for signals received on a plane and a line in the 3D space are given by (2.8) and (2.9), respectively. Equation (2.7) indicates the spectral analysis of the ST PW of interest and thus allows to design filters to filter out directional signals.

$$PW_{3D}(\Omega_x, \Omega_y, \Omega_{ct}) = S_{pw} c \Omega_{ct} \cdot \delta(d_x \Omega_{ct} - \Omega_x) \cdot \delta(d_y \Omega_{ct} - \Omega_y). \quad (2.8)$$

$$PW_{2D}(\Omega_x, \Omega_y, \Omega_{ct}) = S_{pw} c \Omega_{ct} \cdot \delta(d_x \Omega_{ct} - \Omega_x). \quad (2.9)$$

As described earlier, the RoSs of the spectrum in (2.8) and (2.9) are also confined to a line shaped region in the 3D and 2D frequency domains, respectively. Fig. 2.5(a)

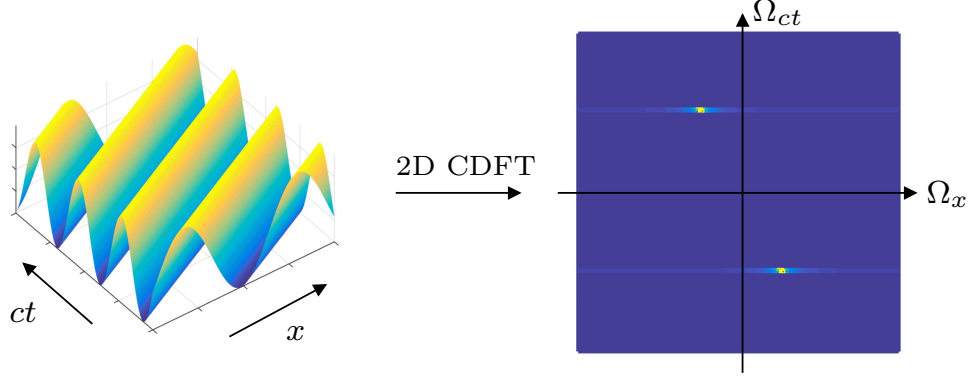


Figure 2.6: Illustration of 2D sinusoidal wave form and its corresponding 2D frequency spectrum.

and Fig. 2.5(b) depict the RoSs of the frequency domain spectrums for the 3D and 2D cases, respectively.

Fig. 2.6 shows the 2D frequency domain plot of a 2D ST PW having a sinusoidal wave front arriving at the x -axis at a DoA of ψ off broadside from the y -axis to the counterclockwise direction. It should be noted that for such sinusoidal wave front, the corresponding magnitude of the 2D frequency response should ideally contain two impulses on the line $-\sin \psi \Omega_{ct} - \Omega_x = 0$ (for the 1D case according to (2.9), $d_x = -\sin \psi$, where ψ is defined as above). It is noted that frequency domain plot in Fig. 2.6 suffers from spectral leakage of a rectangular windowing function applied on top of the 2D signal.

2.3 3D/2D ST PW Signals Received by Arrays of Antennas

Beamforming or spatial filtering of signals necessitates sensing of spatial variations of signals. EM waves are captured or sensed by EM antennas having a finite dimension that are designed to resonate at a particular RF bandwidth. Therefore, sensing ST PW signals in CD spatially is not possible. As a matter of fact, antenna arrays are used for beamforming or spatial filtering applications. Fig. 2.7 shows examples

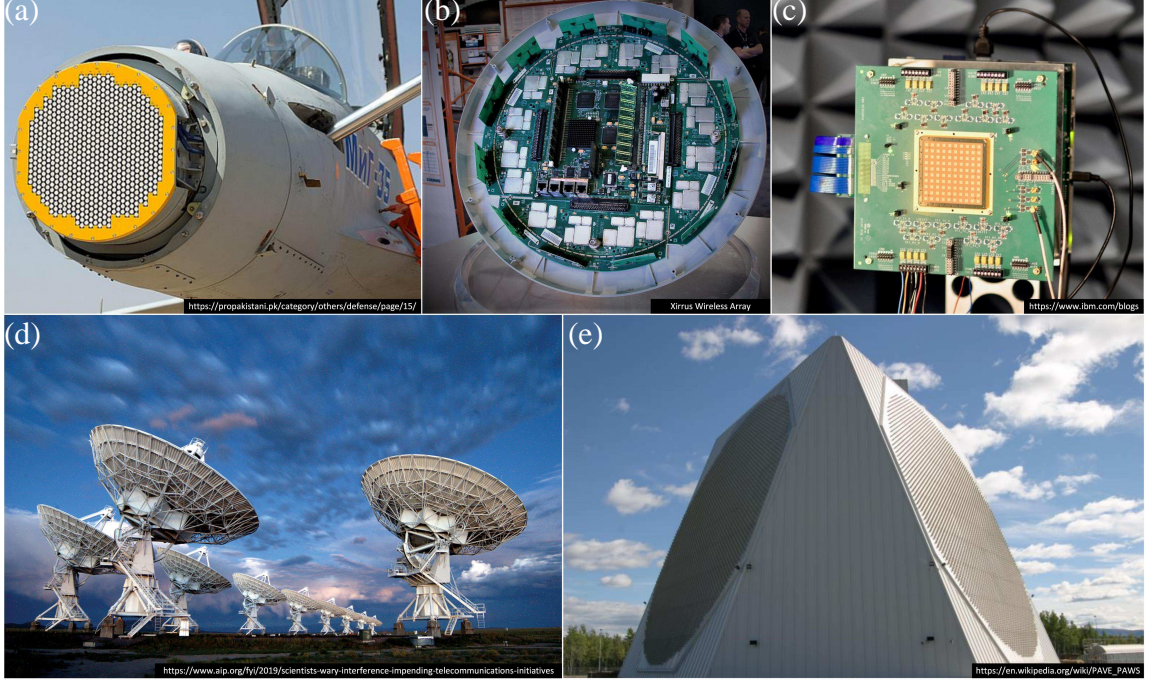


Figure 2.7: (a) 2D antenna array on a fighter jet nose; (b) circular antenna array inside a Wi-Fi access-point; (c) 64-element 28 GHz array developed by IBM and Ericsson [1]; (d) The National Radio Astronomy Observatory's Very Large Array in New Mexico [2] (e) Precision Acquisition Vehicle Entry Phased Array Warning System consisting of a crossed dipole element antenna array located at US Clear Air Force Base, Alaska.

of antenna arrays used in different applications. Different geometries of antenna arrays can be used for spatially sampling signals. Uniform rectangular and linear arrays are the most widely used geometries [35,36] and several other sampling grids like circular, hexagonal are also used [37]. Non-uniform geometries are also used in spatial sampling [38,39]. The discussion in this section will be limited to sampling of 3D and 2D signals with uniform planar and linear arrays, respectively. Uniform circular array sampling of 2D ST PWs is discussed in Chapter 9.

A similar frequency domain analysis that was done with the CD FT can be conducted for the spatially sampled 3D PWs received by the URAs. Let Δx and Δy be the inter antenna element spacing of the planar rectangular antenna array.

If we consider an 3D ST PW given by $pw_{3D}(x, y, ct)$, then the spatially sampled ideal signal will be given by $pw_{3D}(n_x\Delta x, n_y\Delta y, ct)$ where $n_x, n_y \in \mathbb{Z}$. Typically, mutual coupling is present in an actual antenna array and that effect will change the spatially sampled signals to deviate from the ideal expected sampled signal. There are different approaches for mitigating mutual coupling. Typically dummy-elements are added in the edges of rectangular and linear arrays to equalize the mutual coupling effect across the elements. Since mutual coupling and it's mitigation are much broader topics, a mutual coupling free antenna array will be assumed for the subsequent discussion. Another concern to notice in practical antennas is that the antennas have a finite pattern which will be directional and not omni. Therefore, the antenna patter depends on the DoA. Also, the finite antenna pattern will have a gain and phase response that is a function of the frequency of operation. Thus antenna pattern can be expressed as function $\Upsilon(\Omega_x, \Omega_y, \Omega_{ct})$. For simplicity of the subsequent analysis, antennas will be considered omni-directional and to have flat temporal frequency response across the bandwidth of operation.

To analyze the spectral content of a sampled MD signal, first an infinite spatial sampling grid will be assumed. The 3D mixed domain output of such a sampling grid where spatial variables are discrete and the temporal variable is continuous can be denoted as $a_{3D,m}(n_x, n_y, ct)$. Then the 3D mixed domain FT can be defined for the Fourier transform pair, $a_{3D}(n_x, n_y, ct) \xleftrightarrow{\mathcal{F}} A_{3D,M}(\omega_x, \omega_y, \Omega_{ct})$ as given in (2.10),

$$A_{3D,M}(\omega_x, \omega_y, \Omega_{ct}) = \int_{t=-\infty}^{t=+\infty} \sum_{n_x=-\infty}^{+\infty} \sum_{n_y=-\infty}^{+\infty} a_{3D,M}(n_x, n_y, ct) e^{-j\omega_x n_x} e^{-j\omega_y n_y} e^{-j\Omega_{ct} ct} dct, \quad (2.10)$$

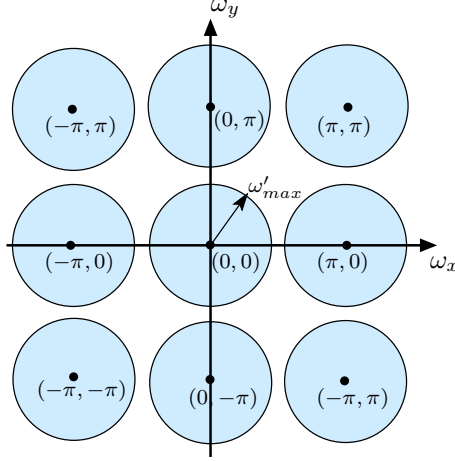


Figure 2.8: The top-view of the ROS of a 3D ST PW signals.

where, $\omega_x = \Omega_x \Delta x$, $\omega_y = \Omega_y \Delta y$. Following [35][chap. 1], (2.10) can be expressed as in (2.11),

$$A_{3D,M}(\omega_x, \omega_y, \Omega_{ct}) = \frac{1}{\Delta x \Delta y} \sum_{m_x=-\infty}^{+\infty} \sum_{m_y=-\infty}^{+\infty} PW_{3D} \left(\frac{\omega_x - 2\pi m_x}{\Delta x}, \frac{\omega_y - 2\pi m_y}{\Delta y}, \Omega_{ct} \right), \quad (2.11)$$

where $m_x, m_y \in \mathbb{Z}$. The function $PW_{3D}(\cdot)$ is the 3D-CDFT of the 3D CD received PW function. It is also noted that the spatially sampled signal now has an infinitely repeating spectrum pattern with a periodicity of 2π along both ω_x, ω_y .

Fig. 2.8 shows a diagram containing the repetition pattern of the spectrum in the ω_x, ω_y plane looking from the Ω_{ct} axis. For this illustration $\Delta x = \Delta y = \Delta$ is assumed. As shown in the figure, if $\omega'_{max} \geq \pi$, then spatial aliasing of signals occur in the spatial-frequency space. The condition for avoiding spatial aliasing is given by,

$$\omega' = \Omega_k \Delta \leq \pi, \quad (2.12)$$

where $k \in [x, y]$. For band limited signals where $\Omega_{ct} \leq c^{-1} \Omega_{t,max}$, $\Omega_{k,max} = c^{-1} \Omega_{t,max} \tan \vartheta_{max}$. Since $\tan \vartheta = \sin \theta$, $\Omega_{k,max} \cdot \Delta \leq \pi$ implies $c^{-1} \Omega_{t,max} \cdot \sin \theta_{max} \cdot$

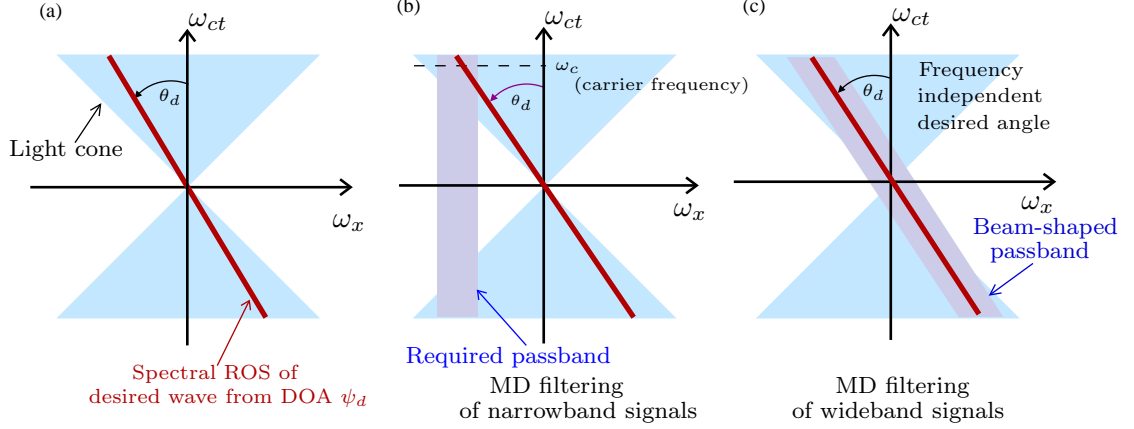


Figure 2.9: Cross section through $\omega_y = 0$ plane in the space-time frequency domain.

$\Delta \leq \pi$ and thus the sampling criterion or the inter element spacing for avoiding spatial aliasing is given by (2.13),

$$\Delta \leq c / (2 \cdot f_{t,max} \cdot \sin(\theta_{max})), \quad (2.13)$$

where θ_{max} is the maximum DoA of the signal in the elevation plane. The same concept is valid when the signals are time-discrete. For such cases, the sampled signal spectrum will also repeat in the ω_t (or ω_{ct}) axis where $\omega_t = \Omega_t \Delta T$. ΔT here is the sampling period where temporal sampling frequency, $f_s = 1/\Delta T$.

2.4 Spatial Filtering of ST PWs viz. Beamforming

Selective enhancement of received plane waves along a particular DoA requires a multi-dimensional space-time filter having a passband aligned with the line-shaped spectrum oriented at the corresponding angle in the MD frequency domain. The diagrams shown in Fig. 2.9 illustrate cross sectional view of the RoS of a 3D ST PW along $\omega_y = 0$ and the figure depicts different passbands that can be employed to filter temporal signals having different bandwidths. Fig. 2.9(c) shows the ideal

passband of a wideband MD filter that should be employed for beamforming a wideband planar signal. Such a filter can be realized either in analog or in digital. Digital implementation would require going from direct RF to bits and therefore, the RF frequencies have to be relatively small when compared to ADC sampling rates of the digital back-end. Fig. 2.9(b) shows the passband of a MD filter that would filter a narrowband PW signal. This kind of passband can be generated either in analog or digital processing (again digital processing require RF to bits). Most phaseshifting based narrowband analog phased arrays produce such passbands in directional enhancement of waves. Beamforming that is achieved with such filtering that has a passband as shown in Fig. 2.9(b) is known to suffer from beam squinting (this phenomenon is discussed in Chapter 7.1). The effect of beam squinting is small for highly narrowband systems.

Fig. 2.9 specifically illustrates beamforming passbands at RF in MD frequency domain. Beamforming can be achieved in IF or baseband as well. In most communication systems, the RF is first downconverted to a low-IF or to baseband before digital processing. The Fig. 2.9 shows an illustration of the 2D spectral transformation of a 2D ST bandpass PW originally at RF to baseband. Fig. 2.10(a) emulates the spectrum of a signal that is at RF impinging on an ULAs at an angle of 60° . The Fig. 2.10(b) shows the temporally in-phase (I) quadrature (Q) downconverted 2D spectrum, which corresponds to the mathematical operation in (2.14) that obeys the modulation property of the MD Fourier Transform.

$$\begin{aligned} s(x, ct) &\xrightarrow{\mathcal{F}} S(\omega_x, \omega_{ct}), \\ s(x, ct)e^{-j\omega_0 ct} &\xrightarrow{\mathcal{F}} S(\omega_x, \omega_{ct} + \omega_0). \end{aligned} \quad (2.14)$$

Fig. 2.10(c) shows the ideal passband required for filtering such directional narrow-

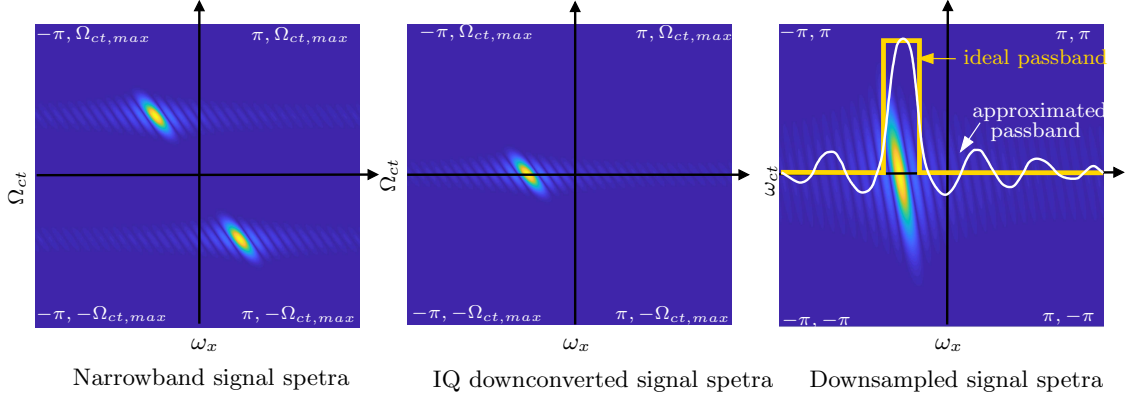


Figure 2.10: Frequency spectra of the 2D ST BP signal which is received by a ULA; (b) the downconverted spectrum; (c) spatial filtering to the received multi-dimensional signal.

band signals. This kind of passband is analogous to that is shown in Fig. 2.9(b) other than the fact that the signal is now at baseband than RF.

2.5 Different Spatial Filtering Approaches for ST Array Processing

This section will provide a brief overview on different beamforming implementations and their mathematical formulations. Although the 1D ULA configurations are used for the discussion to follow for the convenience, the mathematical formulations and the beamforming approaches can be extended to higher dimensional arrays without loss of generality. Beamforming algorithms, circuits and architectures can be categorized differently. Different categorizations exist based on hardware implementation approach, bandwidth of operation, pattern synthesis techniques and depending on the beams realized being fixed or adaptive. An abstract level categorization of the receive-mode beamforming topologies based on the hardware implementation approaches is shown in Fig. 2.11. An example of traditional phased array topology us-

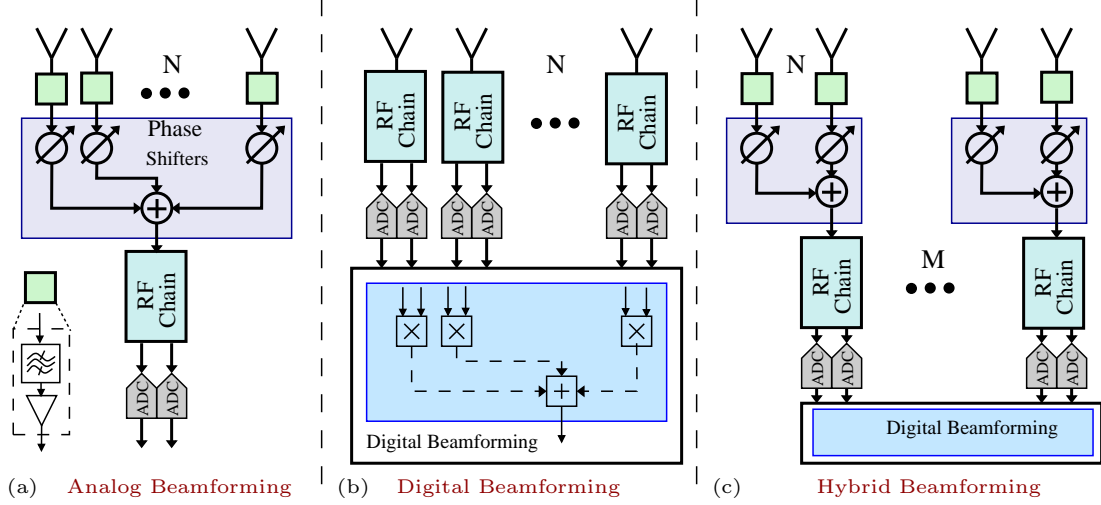


Figure 2.11: Beamforming topologies based on the hardware implementation; (a) analog beamforming, (b) digital beamforming, and (c) hybrid beamforming architectures.

ing analog electronics at RF (or IF) for phase manipulation is shown in Fig. 2.11(a). Digital multi-beam beamforming provides maximum flexibility, reliability, reconfigurability and maximal degrees of freedom for beam combination over traditional passive/active analog phased-array realizations. A generic hardware configuration of a digital beamforming setup is shown in Fig. 2.11(b). However, DBF requires one RF chain and two analog to digital converter (ADC)s per antenna element (assuming I Q downconversion), i.e., P RF chains and $2P$ ADCs for P antenna elements. This results in high power consumption, particularly with the utilization of large arrays that employ high number of ADCs (supporting large bandwidths, for e.g in mmW), which are usually the most power-hungry blocks [40]. In comparison, analog beamformers have the lowest power consumption among all topologies. Hybrid-beamforming addresses this challenge by combining low-dimensional digital beamformers (at baseband) with analog beamformers (at RF) [41]. Such architectures can achieve performance similar to fully-digital schemes at lower cost and power. They typically use RF phase-shifters, TTDs, or lenses for level-1 ana-

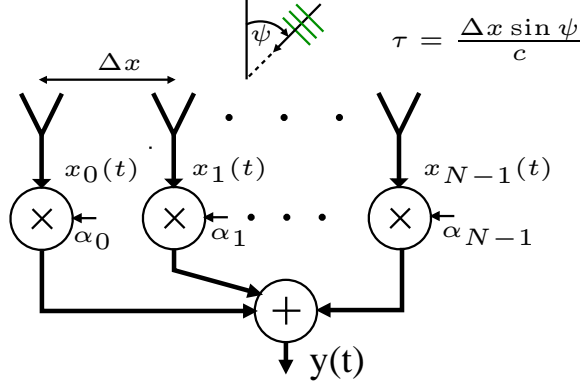


Figure 2.12: Receive mode model of an N -element phase array.

log beamforming [41–43] and baseband digital processing for level-2 beamforming. Having introduced realization methods of beamformers in hardware, the following section will review the basics of beamformer implementations with fixed weight-set.

Consider an N element uniform linear antenna with Nyquist element spacing Δx as shown in Fig. 2.12 where $\Delta x = \lambda_{\min}/2$ and λ_{\min} corresponds to the highest frequency of interest. Let $\mathbf{x} \in \mathbb{C}^{N \times 1}$ be the time continuous output signal vector from the array as given in (2.15) where $x_{n_x}(t) = a_{pw}(n_x, t)$ is the signal at n_x th spatial location and $a_{pw}(n_x, t)$ is the 2D signal from the array.

$$\mathbf{x} = [x_0(t), x_1(t), \dots, x_{N-1}(t)]^\top \quad (2.15)$$

Also, let $A_{pw,m}(n_x, j\Omega_t)$ be the mixed domain transfer representation (by taking the Fourier transform along time) of $a_{pw}(n_x, t)$. The $A_{pw,m}(n_x, j\Omega_t)$, the mixed domain output from the array can be denoted as a vector $\mathbf{a}_{pw,m}$ as shown in (2.16).

$$\mathbf{a}_{pw,m} = [A_{pw,m}(0, j\Omega_t), A_{pw,m}(1, j\Omega_t), \dots, A_{pw,m}(N-1, j\Omega_t)]^\top \quad (2.16)$$

If (2.17) denotes the weighting vector applied to the array signal \mathbf{x} where $\alpha_i \in \mathbb{C}$, $0 \leq i \leq N-1$, then the z -transform of such a spatial discrete ST PW filter is given by (2.18).

$$\mathbf{w} = [\alpha_0, \alpha_1, \dots, \alpha_{N-1}]^\top, \quad (2.17)$$

$$H(z_x) = \sum_{k=0}^{k=N-1} \alpha_k z_x^{-k} \quad (2.18)$$

The frequency response of the spatial filter can be therefore expressed as in (2.19) by replacing $z_x = e^{j\omega_x}$ where $\omega_x = \Delta_x \Omega_{ct} \sin \psi$.

$$H(e^{j\omega_x}) = \sum_{k=0}^{k=N-1} \alpha_k e^{-j\omega_x k} \quad (2.19)$$

The output response $Y_m(j\Omega_t)$ to a 2D input signal $w_{pw}(n_x, t)$ can be expressed in the Fourier domain as given in (2.20) where $Y_m(j\Omega_t)$ is the Fourier transform of $y(t)$: the beam output.

$$Y_m(j\Omega_t) = \mathbf{w} \cdot \mathbf{Z} \cdot \mathbf{a}_{pw,m}, \quad (2.20)$$

Here, $\mathbf{Z} = (\zeta_{i,j})$ with $\zeta_{i,i} = e^{j\omega_x \cdot i}, \forall i, j \in \{1, 2, \dots, N\}$ is a $N \times N$ diagonal matrix. For cases where α_i 's in \mathbf{w} are narrowband coefficients, then the coefficients essentially become complex constants and for such cases the beamformed time domain output $y(t)$ simplifies to the operation in (2.21),

$$y = \mathbf{w}^\top \mathbf{x}, \quad (2.21)$$

The produced beam pattern in the far field is a function of the weights α_i s and the complex beam pattern corresponding to \mathbf{w} is related to the discrete Fourier transform of the spatial weighting vector \mathbf{w} [44].

Setting $\alpha_i = e^{-j\Omega_t(i\tau)}$ where, $\tau = \frac{\Delta x \sin \psi}{c}$ or making \mathbf{w} as shown in (2.22) produces a broadband beam in the direction ψ .

$$\mathbf{w} = [1, e^{-j\Omega_t\tau}, \dots, e^{-j\Omega_t(N-1)\tau}]^\top, \quad (2.22)$$

c is the wave propagation speed and $\Omega_t = 2\pi f_t$ where f_t is the temporal frequency variable ($f_t \in [f_c - B, f_c + B]$ and B is the baseband bandwidth). The term $e^{-j\Omega_t\tau}$ is a complex frequency dependent weighting that realizes a TTD across the signal

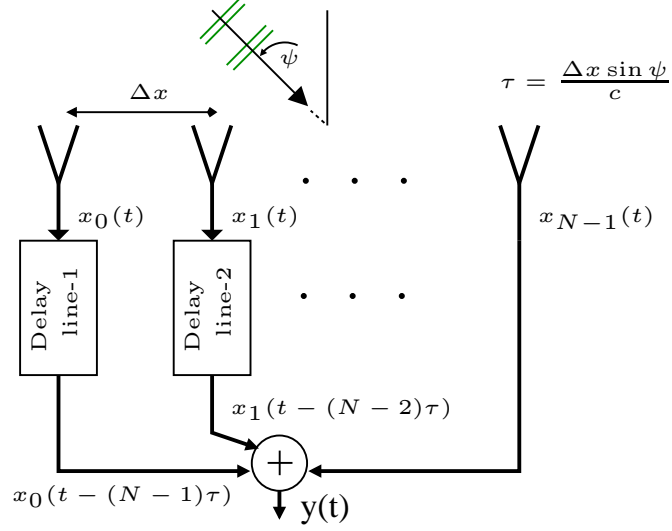


Figure 2.13: True-time delay-and-sum beamforming in a receive-mode N -element phase array.

bandwidth and such a weight set will ideally produce a wideband squint-free beam. Fig. 2.13 shows the overview architecture of such TTD based beamformer. In analog RF, this type of architecture can be realized by employing progressive transmission line delays [45], sensor delay lines [46], tunable spiral inductors [47] or using analog electronics that realizes APF responses to accurately synthesis the delays.

Wideband beamforming can be achieved in digital by employing digital filters that synthesizes the required wideband passband. Different digital filter architectures can be identified in the literature for achieving wideband beamforming. Most straight forward way of doing this is to implement the same architecture shown in Fig. 2.13 in digital using a higher order FIR interpolation or fractional delay filters as illustrated in Fig. 2.14(a) to approximate the required true-time delay at each antenna's signal path. Note that the $x_i[n], i \in [0, N - 1]$ inputs to the array processor coming from the i^{th} antenna is a complex signal; the signals present at the antennas are sampled in the spatial domain, amplified and filtered, down-converted to baseband and finally digitized by an ADC (or down-converted to an IF and then

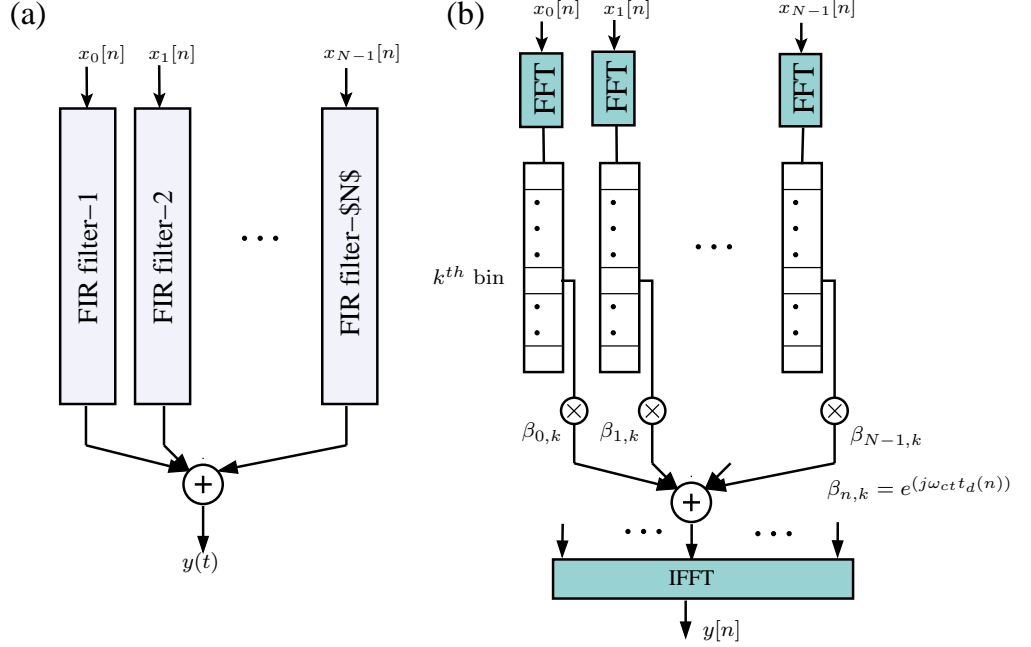


Figure 2.14: (a) Digital filter-and-sum beamforming architecture; (b) FFT-based frequency domain wideband beamforming in digital.

converted to baseband in digital). The process is achieved through mixing and can be modeled as multiplication by $e^{j2\pi fct}$ and leaves the spatial frequency components intact. Since the inputs to the filters are complex, two copies of the same FIR fractional/interpolation filter realizing the required delay at the i^{th} filter is needed.

Another method is to achieve the same idea in the frequency domain as illustrated in Fig. 2.14(b). This realizes the required TTD by utilizing frequency depended weightings. This is achieved by employing a FFT in each received path and decomposing the input signal to a set of narrowband outputs where a set of complex coefficients can be applied at each frequency bin of the signals for realizing the required delay in the frequency domain at each element. The phase aligned relatively narrowband outputs then are summed for beamforming. Each output corresponding to each frequency bin can then be converted to time domain using an IFFT operation.

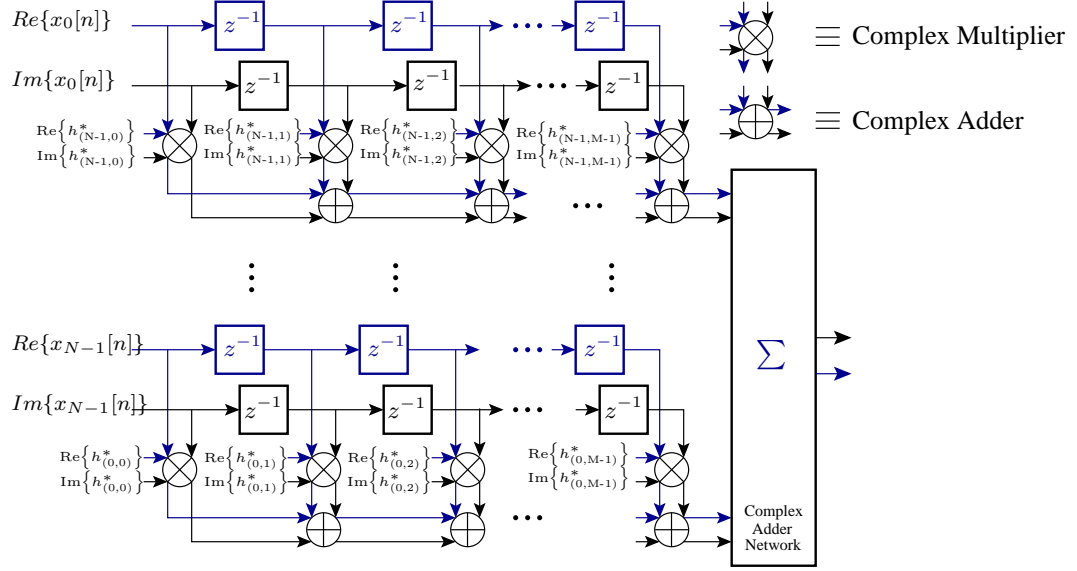


Figure 2.15: Digital architecture of a Frost beamformer.

Different other digital beamforming techniques based on 2D FIR also exist; but implementation wise all of them can be broadly categorized under Frost beamformers [48] which is similar to the filter-and-sum architecture shown in Fig. 2.14(a). This structure is widely used to realize different adaptive/non-adaptive 2D/3D passbands in digital [49–51]. Such filter responses at baseband would be complex valued and thus would require complex multiplier based FIR structure in implementations as shown in Fig. 2.15. 2D/3D network resonance based beamformers are also known for their low-complexity implementations [52]. These filters are realized as 2D/3D IIR filter structures. The IIR nature in the filters achieves the beamforming at lower hardware complexity [53].

For narrowband systems where temporal frequency spread around f_c is small, $\Omega \approx 2\pi f_c$ and the term $e^{-j2\pi f_c \tau}$ becomes a complex constant β_k . Therefore, a narrowband beam can be realized by replacing Ω with $2\pi f_c$ that gives rise to \mathbf{w} in (2.23)

$$\mathbf{w} = \left[1, e^{-j2\pi f_c \frac{\Delta x \sin \psi}{c}}, \dots, e^{-j2\pi f_c (N-1) \frac{\Delta x \sin \psi}{c}} \right]^\top. \quad (2.23)$$

2.6 Formation of Multiple Simultaneous Beams

The equation in (2.20) describes the multi-input single-output system for producing a single beam. Producing multibeam involves realizing more than one complex weighting vectors. The underline function of realizing p simultaneous beams involves implementing the linear system given in (2.24),

$$\mathbf{y}_m = \mathbf{W}_p \cdot \mathbf{Z} \cdot \mathbf{a}_{pw,m}, \quad (2.24)$$

where, \mathbf{y}_m is the Fourier domain vector of p RF beams with $\mathbf{y}_m = [y_m(0, j\Omega_t), y_m(1, j\Omega_t), \dots, y_m(p-1, j\Omega_t)]^\top$ and $\mathbf{W}_p \in \mathbb{C}^{p \times N}$ being the $p \times N$ matrix containing p beamforming vectors as given in (2.25).

$$\mathbf{W}_p = [\mathbf{w}_1, \mathbf{w}_2, \dots, \mathbf{w}_p]^\top, \text{ where } 2 \leq p \leq N-1. \quad (2.25)$$

\mathbf{W}_p is a $p \times N$ matrix which takes the form of a Vandermonde Matrix [54]. Here, each $\mathbf{w}_k = [1, e^{-j2\pi f \frac{\Delta x \sin \psi_k}{c}}, \dots, e^{-j2\pi f(N-1) \frac{\Delta x \sin \psi_k}{c}}]^\top$, $1 \leq k \leq p$, correspond to a steering weighting vector realizing a beam at an angle of ψ_k off broadside. \mathbf{w}_i in (2.25) should be linearly independent for maximizing the number of degrees of freedoms (DoFs). Picking $p = N$ here will capture all the DoFs from the array.

The Fig. 2.16 illustrates an overview of how multibeam beamforming can be achieved in different implementation approaches. Different other multibeam beamforming architectures can be found in literature. Realization of multiple beams can be achieved by using a Frost processor shown in Fig. 2.15 by setting the filter coefficient that achieves two or more passbands [34, 55]. A multibeam beamforming network realization method based on 2D network resonance concept is described in [56].

Picking $\mathbf{W}_{p=N}$ to be the N -point DFT matrix defines a Fourier basis for representing the array signal vector and produces N orthogonal RF beams for both

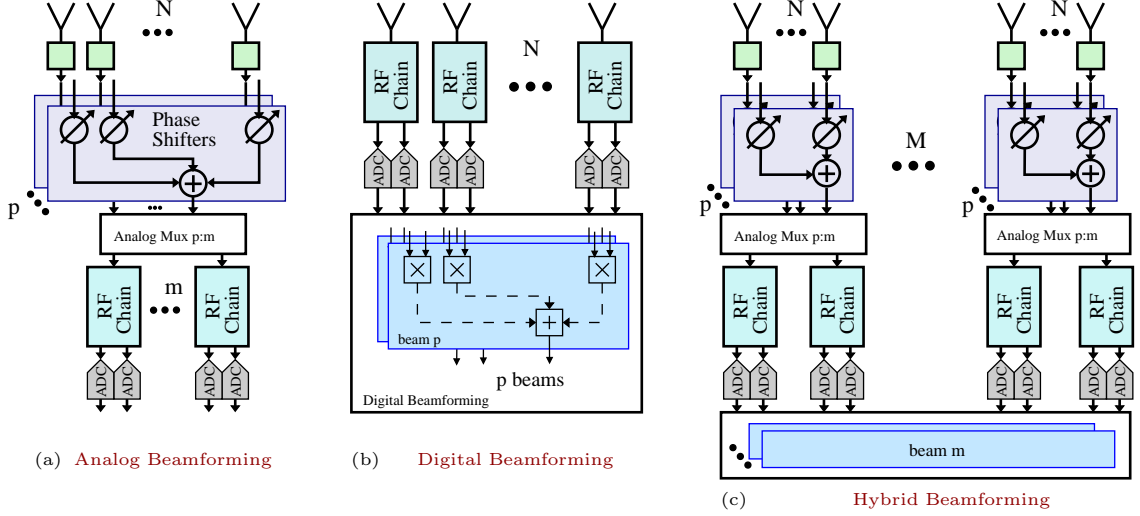


Figure 2.16: Overview of analog, digital and hybrid multibeam architectures.

transmit and receive multibeam applications. The DFT matrix is full ranked and thus captures all degrees of freedoms. The orthogonality property of the DFT ensures that there is no inter-beam interference. Since the DFT computation can be achieved in relatively reduced overhead using FFT implementations, the use of FFT across Nyquist sampled antenna arrays are quite popular. The analog FFT based ‘Butler matrix’ implementations are well known in microwave and antennas community to produce multiple simultaneous orthogonal beams [57, 58]. Deeper discussion of spatial FFT based beamforming is carried out in the next chapter.

The common problem in multibeam realization is the associated high computational/circuit complexity. For larger arrays, producing p beams by realizing \mathbf{W}_p in (2.25) require a hardware complexity in the order of $\mathcal{O}(pN)$ which can be prohibitively large in computational complexity or in terms of hardware electronics. Here, the notation $\mathcal{O}(\cdot)$ indicates the upper bound complexity [59]. The motive for the research explained in this dissertation is this huge complexity problem for the larger arrays which are demanded by the emerging mmW and sub-THz systems. Thus low hardware complexity implementations (2.25) is always desired. The

research work is focused on such low-complexity algorithms and circuits for implementing (2.25) with analog, digital and hybrid realizations.

CHAPTER 3

LOW-COMPLEXITY DIGITAL RF MULTIBEAMS USING MULTIPLIERLESS APPROXIMATE DISCRETE FOURIER TRANSFORMS

In this chapter, the use of DFT approximations are proposed for low-SWaPC implementations of digital multibeam RF apertures using ULAs. An 8-point DFT approximation and a 16-point DFT approximation is proposed for realizing real-time digital RF beams with low-complexity VLSI architectures and the proposed algorithms have been experimentally verified using a real-time phased-array setup. By using such DFT approximations the digital multiplicative complexity can be reduced to zero while having negligible repercussions in RF beam patterns compared to the corresponding fixed-point FFT based RF beams.

3.1 Multibeam and the Role of Fully Digital Beamforming

The efficient formation of far-field antenna patterns simultaneously across a multitude of directions is crucially important for the areas such as wireless communications, radio astronomy, imaging, radar, and electronic warfare. Multibeam beamforming has been usually achieved in the analog microwave domain using analog techniques (e.g., Rotman lenses [60] and Butler/Nolan matrices [57, 61]). Emerging mmW systems are considering hybrid multibeam beamforming due to its power efficiency and excellent performance for a reasonably small number of antenna elements and user streams [62, 63]. Although digital beamforming requires the control of each individual antenna element in an antenna array, it is promising for the future due to its many inherent advantages, which include [64]: i) maximum flexibility/reconfigurability; ii) easy system updates and support for new beamforming algorithms as they emerge; iii) precise control of both the gain and phase of in-

dividual antenna elements thus giving better control of the beams; iv) maximum degrees of freedom from a given array; and v) reduced maintenance and calibration requirements.

Element-wise digital beamforming requires a dedicated receiver (or a transmitter, in transmit mode) for each antenna element, which is usually a uniformly spaced linear or rectangular array of antennas. Multibeam can be generated by expanding the concept of a phased-array to multiple simultaneous directions by using the fact that each direction of propagation of a carrier wave is associated with two spatial frequencies $(\omega_x, \omega_y) \in \mathbb{R}^2$ across the two orthogonal coordinate axes of a rectangular array aperture. Multiple beam digital beamforming is desired at the lowest possible energy consumption for a given bandwidth, supply voltage, and technology node, which leads to domain-specific architectures that are optimized for low complexity and power consumption.

In this chapter, approximate computing-based algorithms and computing architectures that achieve quasi-orthogonal RF beams without using any digital multiplier circuits are proposed. The multiplierless nature of the digital computing architectures allow low chip area/size, weight, and power consumption (SWaP) and avoid the need for digital multipliers that have high circuit complexity (transistor count) and power consumption. This is likely to become more critical as wireless systems move to sub-terahertz frequencies and much wider channel bandwidths than that are used currently [65]. Algorithms that are multiplierless thus lead to substantially reduced SWaPC in real-time digital silicon implementations [65, 66].

Multibeam beamforming on linear/rectangular apertures is important for exploiting multi-directional channels in massive-MIMO systems, for example in 5G mm-wave wireless networks. Such systems rely on the combination of beamforming with MIMO theory [25, 62, 63, 65, 67, 68] and as frequencies move to THz ranges, the

need for providing thousands of simultaneous beams will emerge due to the small size of the wavelength and physical antenna aperture. Recent work has described different phased array architectures targeting 5G applications [69–75]. However, most of the literature has been focused either on hybrid beamforming systems or fully-analog architectures due to the prohibitive processing complexity of fully-digital beamforming. Other important applications for microwave and mm-wave digital multibeam beamformers include emerging defense applications such as space-based low earth orbit communications, mesh networks between micro satellites, space-based Internet distribution to densely populated areas, and multi-domain mosaic warfare where reliable high-speed wireless connectivity is needed across multiple platforms [65]. The demands of high-capacity wireless networks for such applications can be significantly more difficult to meet than commercial 5G standards [65]. Such demanding wireless channel conditions necessitate beamforming gain across wide bandwidths and narrow angles of propagation (i.e., sharp beams) to both thwart detection and also benefit from beamforming gain. Furthermore, 5G networks will eventually require digital beamforming to reduce the overhead associated with the current 3GPP beam search time in the 5G game structure—great reduction in beam pointing can be obtained by simultaneously searching the environment for the best pointing angle, but this is not yet supported in the 5G 3GPP standard [26].

Some recent work has focused on achieving element-wise fully-digital beamforming. The paper in [76] presents a low-power 8-element digital beamforming prototype based on bit-stream processing. The design uses a low-resolution $\Delta\Sigma$ architecture that replaces multipliers with multiplexers. This multiplexer-based architecture achieves lower power and smaller area than conventional digital beamformers, but the design is limited to a 20 MHz bandwidth with only two simultaneous output beams. Another recent paper [77] reports a 16-element 4-beam digital

beamformer targeting large scale MIMO for 5G communications systems. It uses a similar multiplexer-based approach as in [76] with an interleaved architecture to support a 100 MHz bandwidth. The work in [78, 79] also report experimental verification of fully digital multibeam beamforming schemes targeting MIMO-based 5G implementations. The paper [80] presents a spatial DFT-based digital multibeam beamforming implementation scheme for satellite communications.

3.2 Spatial DFT based Multibeams

As described in Chapter 2, picking $\mathbf{W}_{p=N}$ to be the N -point DFT matrix in the multibeam model of (2.25) defines a Fourier basis for representing the array signal vector and produces N orthogonal RF beams. This is equivalent to employing an N -point spatial DFT across the spatial samples of an N -element ULA. The outputs of such architecture produce N directionally-orthogonal simultaneous RF beams having unique look-directions. Fig. 3.1 shows the overview architecture of a so called a spatial DFT based multibeam RF aperture that employs a ULA. In a narrowband system, the above mentioned method of applying the DFT across the array receiver samples provides approximately non-squinting beams in digital. The array factors of the beams are related to the Fourier transform of the row vectors of the DFT matrix.

The N -point DFT of a finite duration sequence $\{\mathbf{x}_n\} \in \mathbb{C}^{N \times 1}$, of length N is defined as,

$$\mathbf{Y}_k = \sum_{n=0}^{N-1} \mathbf{x}_n e^{-j2\pi kn/N}; k \in [0, N-1], \quad (3.1)$$

where, $\{\mathbf{Y}_k\} \in \mathbb{C}^{N \times 1}$. An N -point DFT is an N^{th} order FIR perfect reconstruction filterbank with k^{th} bin's filter response having a peak at $\omega = \frac{2\pi k}{N}$ as shown in Fig. 3.2.

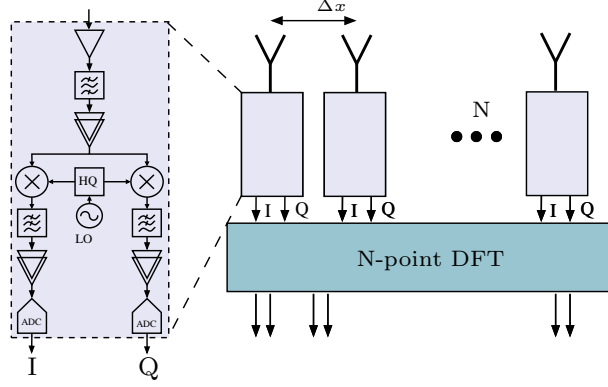


Figure 3.1: Overview architecture of DFT based multibeam RF aperture employing a ULA .

ω is the corresponding frequency variable in the frequency domain. When the N -point \mathbf{x} samples are derived from a ULA antenna outputs, then each output \mathbf{Y}_k corresponds to a beam with the peak directivity at $\omega_x = \frac{2\pi k}{N}$. In Chapter 2.2 it was shown that $\frac{\omega_x}{\Delta x} = -\frac{\Omega_t}{\sin \psi}$, thus, for a narrowband system at frequency f_c , the beam direction of each DFT output is given by,

$$\psi = \sin^{-1} \left(\frac{kc}{\Delta x f_c N} \right). \quad (3.2)$$

For a Nyquist spaced array, where $\Delta x = \lambda_c/2$, and $\lambda_c = c/f_c$, the above relation simplifies to,

$$\psi = \sin^{-1} \left(\frac{2k}{N} \right). \quad (3.3)$$

An intuitive illustration of the spatial filtering that takes place in a digital array is depicted in Fig. 3.2. The figure shows the 2D spectrum of a downconverted baseband plane-wave as seen by a ULA. The ideal filter passband that is required to filter this signal spatially can be approximated by an appropriate DFT filterbank response as shown in the Fig. 3.2.

The DFT computation at each time-step requires an N -point vector of complex-valued transceiver signals (i.e., I and Q samples) to be multiplied with the $N \times N$

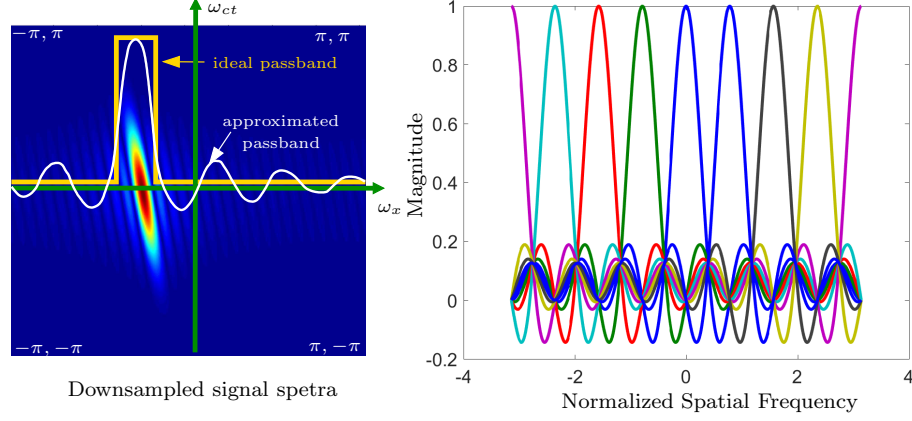


Figure 3.2: (a) Responses of a 8-point DFT filterbank; (b) illustration of the filtering of baseband 2D PW using a DFT filter response.

DFT matrix, where the brute-force computation involves a complexity of $\mathcal{O}(N^2)$ for real-time N -beam digital beamforming. The orthogonality property of the DFT ensures that the main lobe of a given beam falls into the nulls of the other $(N - 1)$ beams, in turn, ensuring no inter-beam interference (under the assumption of no mutual coupling between elements). In practice, N -point DFT is computed at a lower complexity $\mathcal{O}(N \log N)$ multiplications and additions per input frame, using sparse factorizations of the DFT matrix [81]. Such factorizations constitute a suite of algorithms collectively known as Fast Fourier Transforms (FFTs). Thus, formation of N -beams in narrowband digital is achieved by employing a digital N -point FFT on each of the complex I and Q (IQ) signal vector from the array at every time sample. A spatial FFT based digital multibeam beamformer is discussed in [80] and [79] describe a multibeam digital array for MIMO 5G wireless communications applications. More recent digital multibeam integrated circuits (IC) realizations on the same spatial FFT based multi beamforming can be found in [74, 82].

3.3 Discrete Transform Implementation Methods

The conventional approach for implementing DFT is to implement an appropriate FFT algorithm by using fixed-point truncated twiddle factors in the signal flow graph. The implementation of FFT/DFT in fixed-point digital hardware always leads to errors in representing the twiddle factors [83] which are mostly irrational. Owing to the fact that twiddle factors are represented in fixed-point precision in hardware, implementations of discrete transforms are in fact approximations because of the use of finite precision associated in digital arithmetic inside VLSI processors. Apart from the direct approach of fixed-point approximation of the twiddle-factors, several other approaches have been presented in literature towards low-complexity implementations of the DFT by various methods of approximations.

The work in [84] presents a method for implementing discrete transform where its coefficients are represented by integers that are additions of powers of two. Use of such approach allows one to implement the computation of discrete transform with only additions and bit-shifting operations. This method is in essence a successive application of the canonical signed digit representation to the transform coefficients [85].

Discrete transforms can be implemented using the coordinate rotation digital computer (CORDIC) [86,87]. In this approach, the discrete transform is computed with successive applications of rotations to the input signal coordinates. At the end of the process, one can obtain an output that is close to what would be the exact output. Closeness of the output of such methods to the ideal output depends on the application.

Another class of methods can be found that approximates the discrete transforms based on interpreting the rows of a discrete transform as the coefficients of a linear

filter. Using this methodology, several digital filter design techniques have been applied to the implementation of discrete transforms [88–91].

Different methods for relatively efficient computation of the exact DFT methods do exist [92–98]. Those methods are fundamentally different from approximating methods since they are aimed at problems requiring high precision or exact computation such as cryptography. The high precision or exact computation comes at the expense of higher area and resource consumption [96,97]. The work in [84] presents a method for high accuracy DFT approximation based on the approximation of trigonometric quantities by sum-of-powers-of-two (SOPOT). Those approximations are basically canonical signed digit representation, which is a well-known approach to the problem of reducing arithmetic complexity [99–102]. In general, due to the high accuracy that is sought in these methods, the resulting transforms possess an arithmetic complexity that consume much higher area and power consumption in digital VLSI implementations.

In contrast, the application at hand: using the DFT for generating multiple simultaneous beams is much robust to errors. Most beamforming applications can withstand the errors caused by precision limitations or the approximations of the filter bank responses of DFT filter bank responses.

In the work presented in this chapter, a new class of DFT approximations is explored for achieving multibeam beamforming. The beam responses, the performance deviations incurred, and the digital VLSI resource utilization due to the use of the approximated transformations are quantified with respect to the use of the ideal DFT. The main difference between the aforementioned fixed-point VLSI implementations when compared to the proposed architecture resides on how the discrete transforms of interest are approximated. The underlying mathematical basis of the approximation, with sparse factorization based on structured matrix theory, enables

new types of digital VLSI implementation that completely devoid power and area hungry multiplier circuits, while still achieving acceptable RF beams on the array aperture.

The difficulty in proposing DFT approximations for larger sequences rely on the hardness of the deriving efficient fast algorithms for generated approximations, simply because the approximate transforms may not preserve the same symmetries and mathematical properties that exist in the exact DFT matrix.

3.4 DFT Approximations through Parameterization

A class of DFT approximations based on the technique of parameterization of the DFT matrix is explored for generating multiple digital beams that are entirely based on additions and subtractions which approximates the beam responses of an ideal DFT very closely. For this approach, the primary focus is on the DFT block sizes of powers of two i.e., DFT approximations for systems front-end having N elements, where $N = 2^k$, and $k \in \mathbb{Z}^+$ are only explored. This is due to the nice symmetries associated with such structures. Moreover, in this chapter, DFT approximations to be used with an 8- and 16-element arrays are investigated. Chapter 4 will present a low-complexity implementation of a 32-beam system and design methodology towards a 1024-beam digital aperture targeting emerging 5G communication systems based on a 32-point DFT approximation.

The N -point DFT is represented by the $N \times N$ matrix \mathbf{F}_N whose entries are given by $[\mathbf{F}_N]_{k,n} = \omega_N^{nk}$, where $\omega_N = \exp(-2\pi j/N)$ is the N th root of unity, $j = \sqrt{-1}$, and $n, k = 0, 1, \dots, N-1$ [103].

Since, low-complexity implementations of the N -point DFT matrix is the target, the real and imaginary components of $[\mathbf{F}_N]_{k,n}$ coefficients of the matrix \mathbf{F}_N are pro-

posed to be approximated by small integer values \mathcal{P} where $\mathcal{P} = \{0, \pm 1, \pm 2, \pm 1/2\}$. The set \mathcal{P} is chosen such that the hardware implementation is reduced to trivial bit shifts and additions operations instead of involving multipliers. Such approach will produce a search space $\mathcal{Q} = \{z \in \mathbb{C} : \mathcal{R}\{z\} \in \mathcal{P} \wedge \mathcal{I}\{z\} \in \mathcal{P}\}$. Thus, set \mathcal{Q} defines the search space for the coefficients of the DFT approximation considered. Then, employing a parametric-based optimization method as described in [104], optimal low-complexity approximation $\hat{\mathbf{F}}_N$ for $N = 8, 16$ have been derived subjected to multiple constraints. *The parametric-based optimization work was conducted by the UPFE collaborators (Dr. R. J. Cintra and his students) to arrive at the approximated matrices.*

During the optimization process, the target approximations have been optimized for the (i) high proximity to the exact 16-point DFT matrix [105]; (ii) low complexity [106]; (iii) orthogonality or near-orthogonality [107–109]; and (iv) invertibility.

Proximity Measure

The norm of the relative difference between $\hat{\mathbf{F}}_N$ and \mathbf{F}_N assess the proximity of the resulting matrices relative to the exact N-point DFT as measured by Frobenius norm [110]. The proximity measure can be represented as follows.

$$d(\boldsymbol{\alpha}) = \frac{\left\| \hat{\mathbf{F}}_N - \mathbf{F}_N \right\|_{\text{F}}^2}{\left\| \mathbf{F}_N \right\|_{\text{F}}^2}, \quad (3.4)$$

where $\| \cdot \|_{\text{F}}$ denotes the Frobenius norm. Good DFT approximations are linked to small values of $d(\boldsymbol{\alpha})$.

Complexity

As mentioned, to ensure low complexity, the real and imaginary parts of the parameter values have been constrained to the set $\mathcal{P} = \{0, \pm 1, \pm 1/2, \pm 2\}$ as sug-

gested in [108]. Since these multiplicands can be trivially implemented in hardware, the particular constraint leads to hardware realizations with reduced area, higher throughput and operating frequency.

Orthogonality or Near-Orthogonality

Orthogonality is detected when $\hat{\mathbf{F}}_N^H \hat{\mathbf{F}}_N$ is an identity matrix, where the superscript ^H denoted Hermitian transposition. Near-orthogonality is a more general concept aimed at identifying matrices “almost” orthogonal. This can be computed by means of the deviation from orthogonality function $\phi(\cdot)$:

$$\phi(\hat{\mathbf{F}}_N) = 1 - \frac{\left\| \text{diag} \left(\hat{\mathbf{F}}_N \hat{\mathbf{F}}_N^H \right) \right\|_F}{\left\| \hat{\mathbf{F}}_N \hat{\mathbf{F}}_N^H \right\|_F}. \quad (3.5)$$

The function shown above is derived from the deviation from diagonality function [111]. From the DCT approximation theory, it has been noticed that a deviation from orthogonality smaller than 0.2 is sufficient to ascribe near-orthogonality [105]. Thus that threshold is adopted in the generation of approximations.

Invertibility

The matrix mapping based search process might lead to singular matrices. In order to allow for signal reconstruction a DFT approximation must (i) be a non-singular matrix with a low condition number and (ii) have a low-complexity inverse matrix. Mathematically, the above constraints are translated into non-null matrix determinant $\det(\hat{\mathbf{F}}_N) \neq 0$ and the entries of the inverse matrix $\hat{\mathbf{F}}_N^{-1}$ have real and imaginary parts in \mathcal{P} .

3.5 8- and 16-Point Approximate Transforms and Beam Response Analysis

The ADFT matrices were derived through search and optimization by the collaborators in UPFE for $N = 8$, and 16 in accordance with the criterion mentioned in Section 3.4. The derived approximate transforms have also been subjected to a sparse factorization which further reduces the adder complexity of the digital implementation of the approximate transforms. The subsequent sections will present the ADFTs for $N = 8, 16$ that have been derived in the matrix form, and then an analysis of the beam responses pertaining to each ADFT is conducted.

3.5.1 8-Point ADFT

The matrix form of the 8-point DFT approximation found is given in (3.6) [112].

$$\hat{\mathbf{F}}_8 = \frac{1}{2} \cdot \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \end{bmatrix} \quad (3.6)$$

It can be seen that $\hat{\mathbf{F}}_8$ has elements consisting only of $0, \pm 1, \pm 2$ which can be realized using only adder and bit-shift operations, implying the use of zero multipliers. The

$\hat{\mathbf{F}}_8$ is further factorized for reduce adder complexity implementation as in (3.7).

$$\hat{\mathbf{F}}_8 = \mathbf{P} \times \text{diag}(\mathbf{I}_2, \mathbf{A}_1, \mathbf{A}_3) \times \mathbf{D}_2 \times \text{diag}(\mathbf{B}_2, \mathbf{I}_2, \mathbf{A}_4) \times \mathbf{D}_1 \times \text{diag}(\mathbf{B}_4, \mathbf{A}_2) \times \mathbf{B}_8, \quad (3.7)$$

where, $\mathbf{B}_n = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \otimes \mathbf{I}_{n/2}$, I_n is the identity matrix of order n and \otimes denotes

the Kronecker product. $\mathbf{A}_1 = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}$, $\mathbf{A}_3 = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$, $\mathbf{A}_2 =$

$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix}$, $\mathbf{A}_4 = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix}$. $\mathbf{D}_1 = \text{diag}(1, 1, 1, 1, 1, 1/2, 1, 1/2)$, $\mathbf{D}_2 = \text{diag}(1, 1, 1, j, 1, j, j, 1)$, $\mathbf{P} = [e_1|e_5|e_3|e_6|e_2|e_8|e_4|e_7]^T$ where e_i is the 8-point column vector having a 1 at the i^{th} position and 0 elsewhere.

As emphasized earlier in the chapter, since the coefficients of $\hat{\mathbf{F}}_8$ are small integer coefficients, (3.6) can be implemented using adders only. The adders only signal flow graph for the 8-point ADFT is shown in Fig. 3.3. The frequency responses of each output bin of the 8-point ADFT was studied to compare them with the exact transform's beam responses. Numerically simulated beam patterns obtained using the 8-point ADFT algorithm and the 8-point DFT are shown in Fig. 3.4. The patterns are plotted against normalized angular frequency $\omega \in [\pi, \pi]$ which is equivalent to beam responses of Nyquist spaced narrowband array from $\psi \in [-90^\circ, +90^\circ]$ where ψ is the angle measured from the array broadside. Fig. 3.4(a) shows the exact DFT beams and Fig. 3.4(b) shows the beams obtained using the 8-point a-DFT.

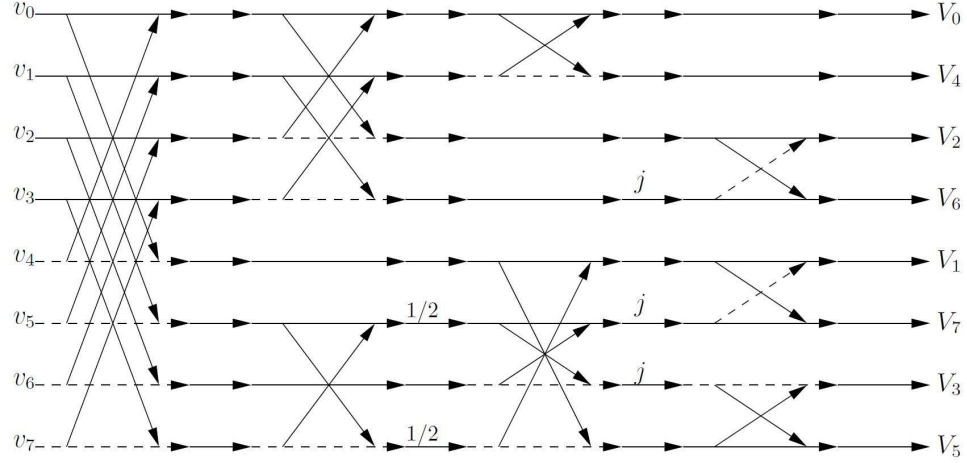


Figure 3.3: Signal flow graph of 8-point a-DFT.

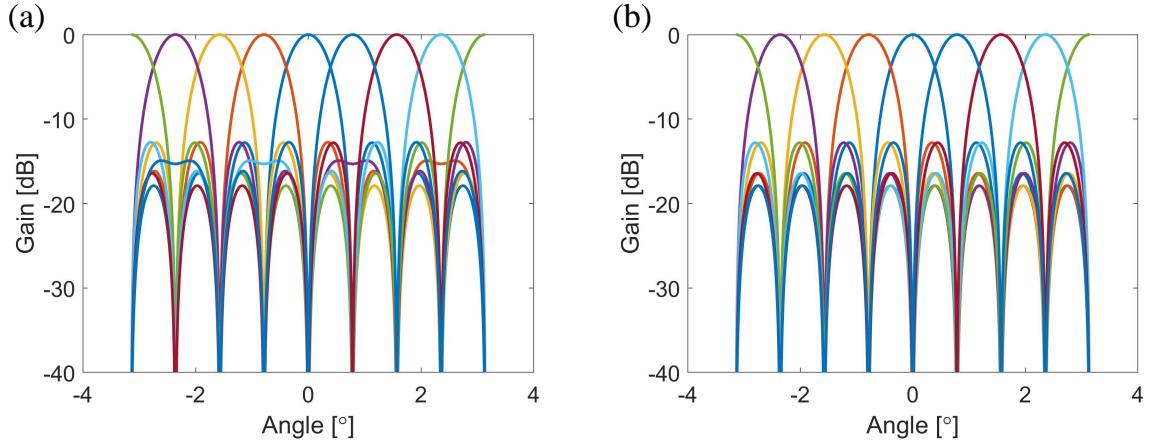


Figure 3.4: (a) Exact DFT beams; (b) beams obtained using the 8-point ADFT; (c) error between the two transforms.

3.5.2 16-Point ADFT

Considering above discussion, the problem of finding a good DFT approximation can be formalized as the following constrained nonlinear optimization problem:

$$\boldsymbol{\alpha}^* = \arg \min_{\boldsymbol{\alpha}} d(\boldsymbol{\alpha}), \quad (3.8)$$

subject to

1. $\Re\{\boldsymbol{\alpha}\} \in \mathcal{P}$ and $\Im\{\boldsymbol{\alpha}\} \in \mathcal{P}$;
2. $\det(\hat{\mathbf{F}}_{16}) \neq 0$;

$$3. \phi(\hat{\mathbf{F}}_{16}) \leq 0.2;$$

4. the inverse matrix must be of low-complexity.

The optimum solution for (3.8) was found to be

$$\boldsymbol{\alpha}^* = \frac{1}{2} \begin{bmatrix} 2j & 1-j & 1-2j \end{bmatrix}^\top,$$

with $d(\boldsymbol{\alpha}^*) = 8.58 \cdot 10^{-2}$ by the conducting an exhaustive search by our collaborators at UFPE. The derived 16-point ADFT matrix is given in (3.9), and is represented as 4 sub matrices for the convenience of presenting.

$$\hat{\mathbf{F}}_{16} = \frac{1}{2} \begin{bmatrix} \mathbf{A}_0 & \mathbf{A}_1 \\ \mathbf{A}_2 & \mathbf{A}_3 \end{bmatrix} \quad (3.9)$$

where \mathbf{A}_i , $i = 0, 1, 2, 3$, are 8×8 sub-matrices as follows:

$$\mathbf{A}_0 = \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 2-j & 1-j & 1-2j & -2j & -1-2j & -1-j & -2-j \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ 2 & 1-2j & -1-j & -2+j & 2j & 2+j & 1-j & -1-2j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ 2 & -1-2j & -1+j & 2+j & -2j & -2+j & 1+j & 1-2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ 2 & -2-j & 1+j & -1-2j & 2j & 1-2j & -1+j & -2-j \end{bmatrix}, \quad (3.10)$$

$$\mathbf{A}_1 = \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ -2 & -2+j & -1+j & -1+2j & 2j & 1+2j & 1+j & 2+j \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ -2 & -1+2j & 1+j & 2-j & -2j & -2-j & -1+j & 1+2j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ -2 & 1+2j & 1-j & -2-j & 2j & 2-j & -1-j & -1+2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ -2 & 2+j & -1-j & 1+2j & -2j & -1+2j & 1-j & -2+j \end{bmatrix}, \quad (3.11)$$

$$\mathbf{A}_2 = \begin{bmatrix} 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -2+j & 1-j & -1+2j & -2j & 1+2j & -1-j & 2+j \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ 2 & -1+2j & -1-j & 2-j & 2j & -2-j & 1-j & 1+2j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ 2 & 1+2j & -1+j & -2-j & -2j & 2-j & 1+j & -1+2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \\ 2 & 2+j & 1+j & 1+2j & 2j & -1+2j & -1+j & -2+j \end{bmatrix}, \quad (3.12)$$

$$\mathbf{A}_3 = \begin{bmatrix} 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ -2 & 2-j & -1+j & 1-2j & 2j & -1-2j & 1+j & -2-j \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ -2 & 1-2j & 1+j & -2+j & -2j & 2+j & -1+j & -1-2j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ -2 & -1-2j & 1-j & 2+j & 2j & -2+j & -1-j & 1-2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \\ -2 & -2-j & -1-j & -1-2j & -2j & 1-2j & 1-j & 2-j \end{bmatrix}. \quad (3.13)$$

The approximation in (3.9) only contains elements from the set $[1 \quad 1j \quad 1/2 - j/2 \quad 1/2 - j \quad j]$, and thus can be implemented in digital using only adders and bit

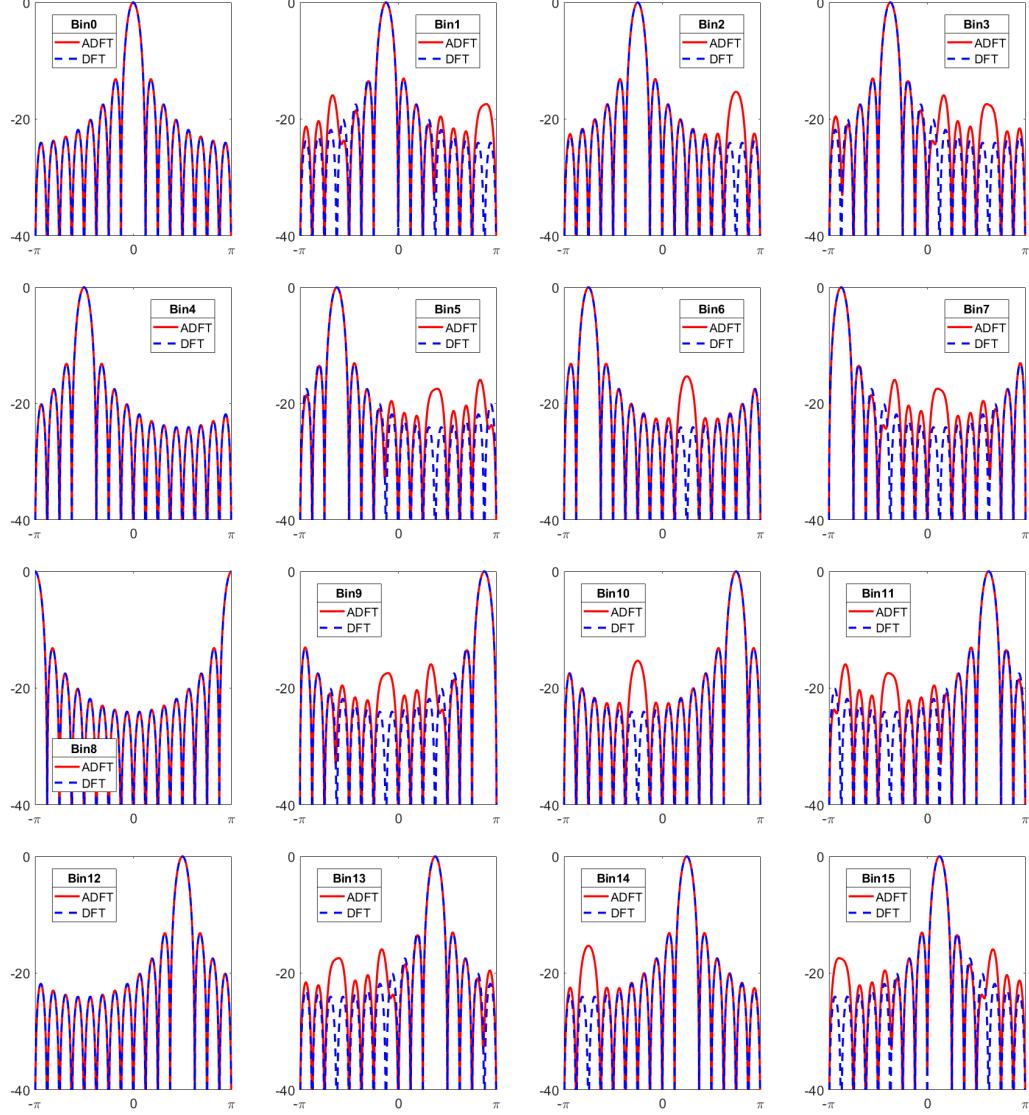


Figure 3.5: Frequency response comparison of the filterbanks of the proposed approximation and the DFT. The x-axis is the normalized frequency and y-axis corresponds to the magnitude in dB.

shifts. The frequency responses of each bin of the 16-point ADFT transform and the corresponding 16-point DFT bin responses are shown in Fig. 3.5.

The adder complexity of $\hat{\mathbf{F}}_{16}$ in (3.9) is reduced by factorizing the approximate transformation and implementing the factorization. The fast algorithm for the transform $\hat{\mathbf{F}}_{16}$ can be derived using factorization approaches related to the decimation-

$$\mathbf{B}_5 = \text{blkdiag} \left(2, \text{diag}(-1, -1, 1, -2, -1, 1, 1) \otimes \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \right), \quad (3.19)$$

$$\mathbf{P}_1 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (3.20)$$

$$\mathbf{P}_2 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad (3.21)$$

and $\mathbf{D} = \frac{1}{2} \text{diag}(1, 1, 1, 1, 1, 1, 1, 1, 1, j, j, j, j, j, j, j)$. The operator $\text{blkdiag}(\cdot)$ maps its arguments into a block diagonal matrix and the symbol \otimes denotes the Kronecker product [113]. Matrices \mathbf{B}_k , $k = 1, 2, 3, 4, 5$, represent butterfly sections. Matrices \mathbf{P}_1 and \mathbf{P}_2 are permutation matrices and the matrix \mathbf{D} is a diagonal matrix with trivial elements. Note that the nonzero entries of the above sparse matrices are in the set $\{\pm 1, \pm 2\}$. This means that the computation of the proposed DFT approximation requires only additions/subtractions and bit-shifting operations, which are efficiently performed in hardware. The signal-flow graph (SFG) of the above fast algorithm for the proposed 16-point DFT approximation is depicted in Fig. 3.6. The proposed fast algorithm is *multiplierless* and requires a total of 116 real additions and 54 bit-shifting operations. For comparison, the arithmetic complexities for performing 16-point DFT using different fast algorithms are listed in Table 3.1.

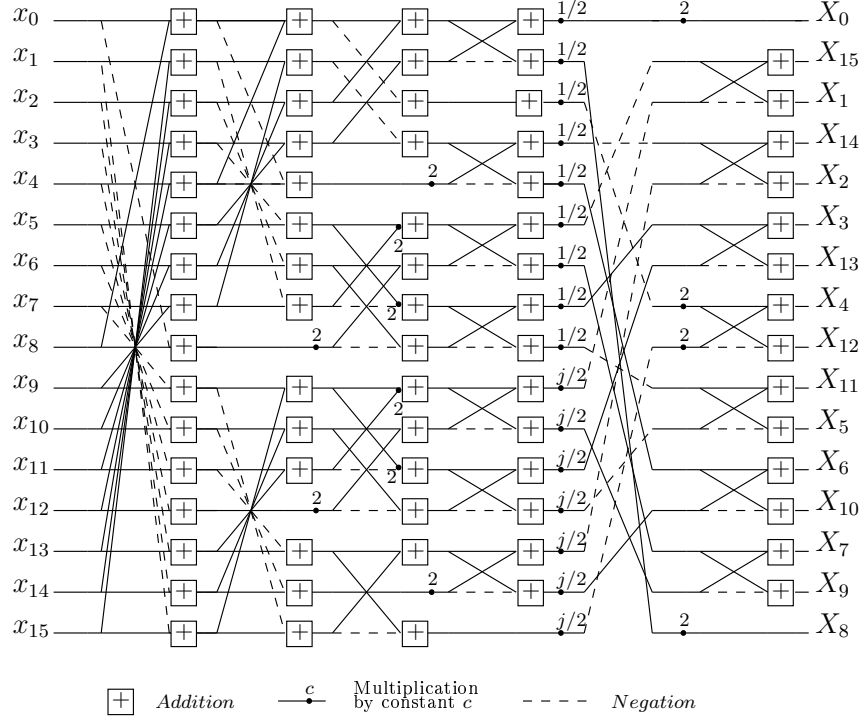


Figure 3.6: The SFG for the fast algorithm of the proposed DFT approximation.

Table 3.1: Comparison of arithmetic complexities for performing the 16-point DFT using different FFT algorithms

16-point FFT Algorithm	No. of real additions	No. of real multipliers
Radix-2 [81, p. 76]	152	24
Winograd [81, p. 102]	74	10
Radix-4 [81, p. 80]	148	20
Proposed	116	0

3.5.3 Error Analysis

An approximate matrix can be understood as a filter bank; each matrix row being a finite impulse response filter. Let $\mathbf{T} = [t_{k,n}]$, $n, k = 0, 1, \dots, N - 1$, be an $N \times N$ linear transform. The transfer function of each of its rows are given by the discrete-

time Fourier transform:

$$H_k(\omega; \mathbf{T}) = \sum_{n=0}^{N-1} t_{k,n} \cdot e^{-jn\omega}, \quad k = 0, 1, \dots, N-1,$$

where $\omega \in [0, \pi]$. The error energy [109] associated to each filter is

$$\epsilon_k = \int_0^\pi |H_k(\omega; \mathbf{F}_{16}) - H_k(\omega; \hat{\mathbf{F}}_{16})|^2 d\omega, \quad k = 0, 1, \dots, 15, \quad (3.22)$$

resulting the following values:

$$\begin{aligned} \epsilon_0 &= \epsilon_4 = \epsilon_8 = \epsilon_{12} = 0, \\ \epsilon_1 &= \epsilon_3 = \epsilon_5 = \epsilon_7 = \epsilon_9 = \epsilon_{11} = \epsilon_{13} = \epsilon_{15} = 1.57, \\ \epsilon_2 &= \epsilon_6 = \epsilon_{10} = \epsilon_{14} = 2.16. \end{aligned} \quad (3.23)$$

Therefore, the total energy error is $\sum_{i=0}^{15} \epsilon_i \approx 21.18$. This error is considered low when compared to other 16-point approximations. For instance, the total error energy from the approximations described in [114] and [115] are 30.32 and 41.00, respectively.

Figure 3.5 shows the frequency responses $H_k(\omega; \mathbf{F}_{16})$ and $H_k(\omega; \hat{\mathbf{F}}_{16})$ linked to the filters formed by the rows of the exact DFT and the proposed approximation, respectively. The deviations in the filter bank responses with respect to the DFT filter bank responses arise as a result of filter coefficients not being ideal valued (because they are approximated by small integers restricted to the set $\mathcal{P} = \{0, \pm 1, \pm 2\}$). Fig. 3.5 shows that the deviations in the filterbank responses occur in the deep stopband of the ADFT responses. These deviations do not exceed the highest side-lobe level. Since the beamformer performance is set by the largest side-lobe level, these deviations in the stopband will not degrade the performance of the phased array.

Table 3.2: Hardware resource consumption for the fixed-point FFT and approximate-DFT cores for a 16-bit input word length on the Xilinx Virtex-6 sx475t FPGA. The fixed-point FFT core uses 8-bit coefficient precision.

Figure of merit	Exact FFT (8-bit precision)	Approx. DFT (multiplierless)	Percent Savings
T_{CPD} (ns)	1.966	1.886	4.07%
Slice Registers	3,247	2,528	22.14%
LUTs	4,030	2,488	38.26%
Occupied Slices	1,338	809	39.54%
Flip-flops	4,543	2,765	39.13%

3.5.4 Digital Implementation of 16-point ADFT

The proposed fast algorithm for the 16-point approximate DFT and the 16-point Cooley-Tukey FFT algorithm were implemented as digital cores for comparing hardware resource utilization. Xilinx tools were used to implement the designs (targeting FPGA realization) in a fully parallel input-output architecture. The designed cores were synthesized and mapped to Xilinx Virtex-6 sx475t chip. The hardware resource comparison for an 16-bit input word length for the two digital cores is given in Table 3.2. Here, the twiddle factor word length for the fixed-point FFT design was fixed to 8 bits. As shown in Table 3.2, there is a considerable saving in the hardware utilization in the ADFT version which reflects as a reduction in area in an ASIC implementation. The critical path delay (T_{CPD}) is low for the approximate case as anticipated but percent saving is relatively low due to the low precision levels used in both.

3.6 Experimental Verification of the Low-Complexity Beams using ADFTs

A 2.4-GHz RF system with a digital processing-end was designed and implemented to physically measure and compare the beams from the 8-point and 16-point approximate DFT algorithms that are proposed for multibeam beamforming with the respective exact DFT's beam responses. The 2.4 GHz system was built with a 16-element antenna front-end so that both the 8-point and 16-point algorithms can be tested. Fig. 3.7 shows the overall system architecture of the digital 2.4 GHz array-receiver experimental setup.

As illustrated in Fig. 3.7, direct conversion in phase (I) and quadrature (Q) receiver chains were used with each antenna element in the setup. The obtained downconverted basedband signal is then processed using a digital hardware through analog-to-digital conversion (ADC). The DFT-based multi-beamforming is performed in digital hardware. Each beam output is then further processed to integrate and estimate the received beam energy for a specific antenna orientation to obtain the beam patterns. The next subsections details the major subsystems of the architecture shown in Fig. 3.7.

3.6.1 2.4 GHz Front-End Antenna Array

A 16-element array of patch antennas that work at 2.4 GHz was used. The design of the patch antenna has been discussed in [116]. A single patch antenna is shown in Fig. 3.8(a). The patch antenna is integrated with a low-noise amplifier. The measured $|S_{11}|$ of the fabricated single patch antenna is show in Fig. 3.8(b). Fig. 3.8(c) shows the measured power pattern of each patch antenna. The 16-element array

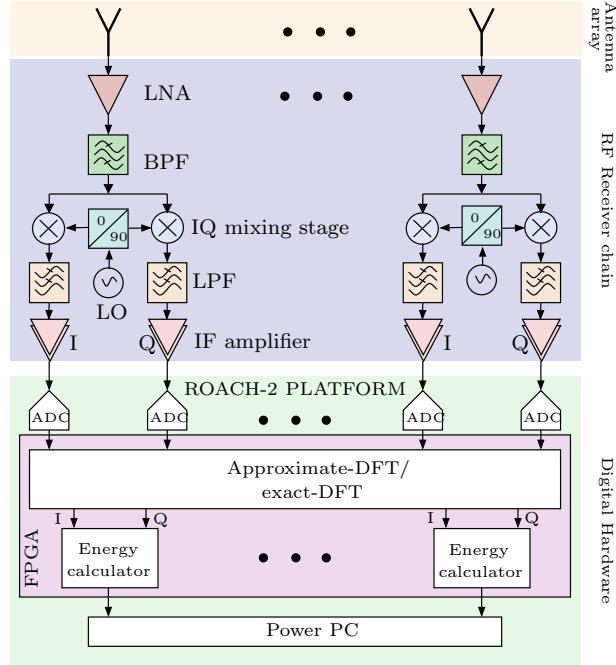


Figure 3.7: Overall system architecture of the 2.4 GHz array-receiver setup.

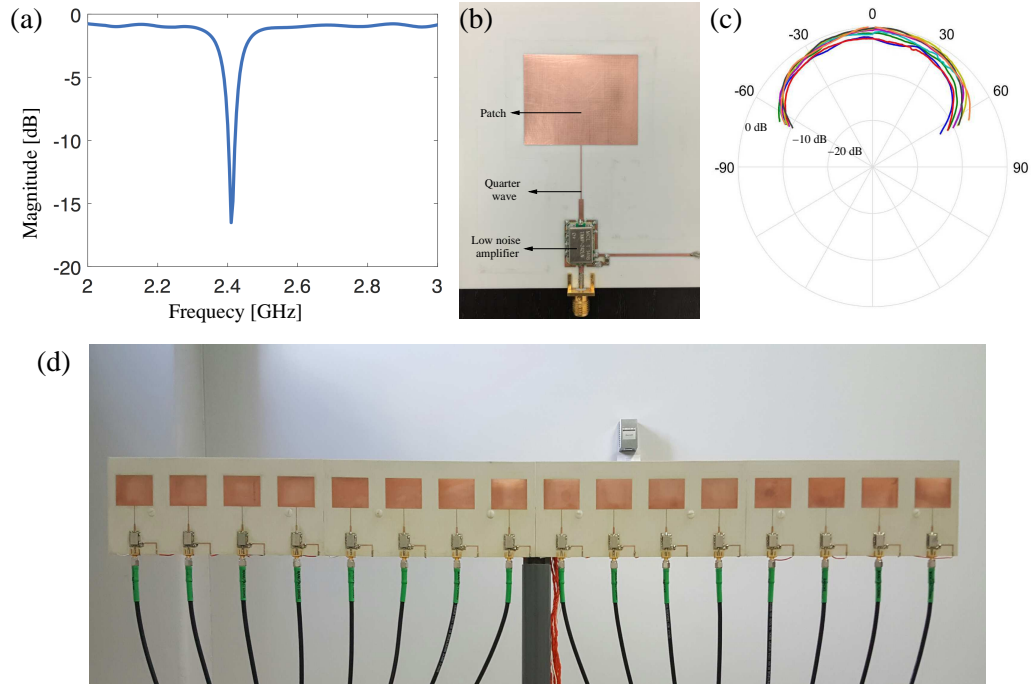


Figure 3.8: (a) Measured $|S_{11}|$ of a single patch antenna; (b) fabricated 2.4 GHz patch antenna element with the integrated LNA; (c) measured power patterns of each antenna element in the array. (d) full 16-element antenna array.

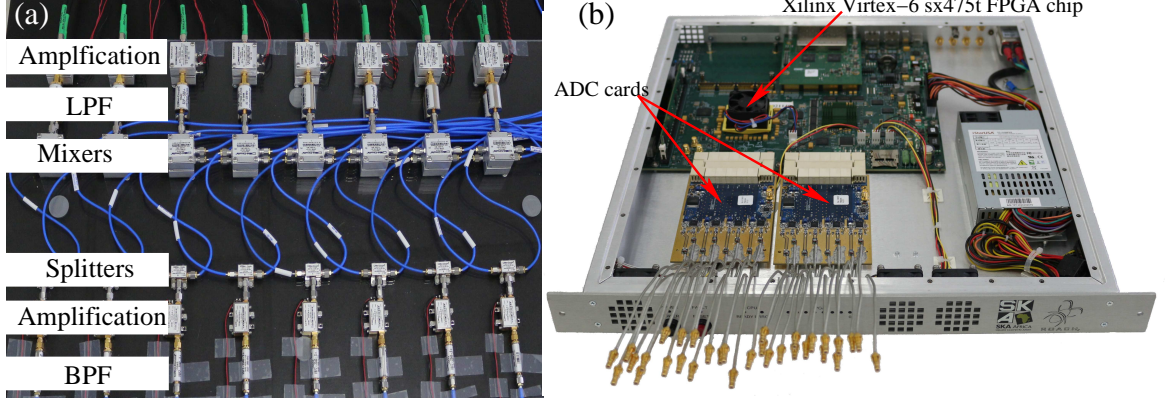


Figure 3.9: (a) RF receiver chains containing a bandpass filter, low-noise amplifier, splitter, mixers, low-pass filter, and an IF amplifier. (b) ROACH-2 platform

was constructed with the element spacing $\lambda/2 \approx 6\text{cm}$. The patch antenna array used in the system is depicted in Fig. 3.8(d).

3.6.2 Microwave Front-End

The outputs of the antennas were fed in to 16 direct-conversion IQ receivers for sampling and digital processing. IQ receiver chains were built using commercial off-the-shelf (COTS) components. The built receiver chains are shown in Fig. 3.9. Each chain was designed to have a low-noise amplification stage (10 dB) (total gain of 20 dB with the integrated LNA on the patch antenna) followed by band-pass filtering and a mixing stage. A centralized LO distribution network was used. The mixer outputs were low-pass filtered and amplified (10 dB gain) to obtain the downconverted IF signal.

3.6.3 Baseband Digital Processing Hardware and Circuits

Digital processing of sampled signals was performed using the ROACH-2 platform [117] which is shown in Fig. 3.9(b). The ROACH-2 platform provides a flexible

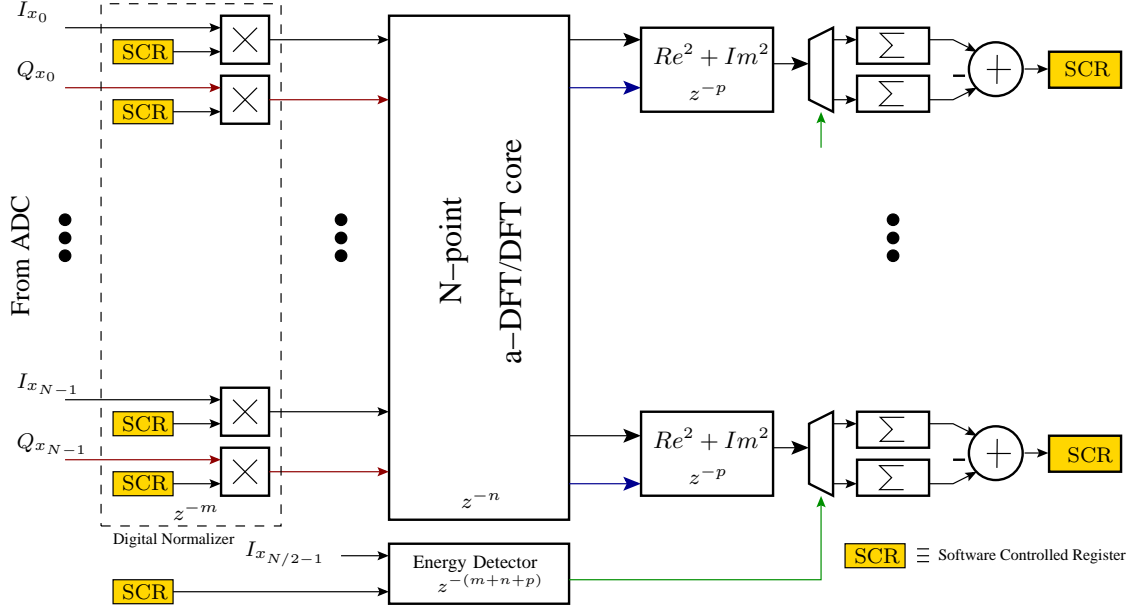


Figure 3.10: Architecture of the digital back-end that generates N -beams ($N = 8, 16$). The figure also shows the energy calculation circuits used for measuring the beam patterns in digital.

versatile hardware platform that comprises of a Virtex-6 sx475t FPGA along with 2-zDOK interfaces that connects to the FPGA which can be used to interface the analog to digital conversion (ADC) cards supporting up to 32 simultaneous channels. The sx475t device has 476,160 logic cells, 74,400 configuration logic blocks (CLBs) and 2016 DSP48 slices.

The “ADC16x250-8” daughter cards which have been build as a part of the CASPER hardware with compatibility to ROACH-2 boards were used in our setup for sampling. Each card can accommodate up to 16 analog inputs. The cards can be configured to achieve different sampling rates, i.e., 32 inputs up to 240 MHz, 16 inputs up to 480 MHz and 8 inputs up to 960 MHz. A picture of the ADC cards installed on the ROACH-2 platform is shown in Fig. 3.9(b). The two cards together provide 32 analog inputs enabling fully simultaneous sampling of the 32 IQ channels from the 16-element channels.

The generic digital architecture used for real-time measurements of the beams from 8-point and 16-point transforms (for both approximate and exact) is illustrated in Fig. 3.10. The digital cores for performing 8-/16-point ADFT and fixed-point FFT were designed targeting the ROACH-2's Virtex-6 FPGA. The input word lengths of the transform cores were set to be 8-bit. This was done since the ADC16x250-8 ADC cards used in the setup had an 8-bit output. The cores were pipelined so that they could be run at clock speeds up to 240 MHz. Fixed point FFT designs were configured with 8-bit precision twiddle factors to achieve a trade off versus precision and area. The beam energy per received direction was calculated digitally for all beam outputs. Separate energy calculation circuits were employed for this at each of the N complex outputs of the N -point transform.

The front portion of the digital architecture consists of the digital normalizing circuit, which is used to calibrate RF chains. The calibration procedure is described in next section. This stage consists of a set of multipliers (an N element design will need $2N$ multipliers in this stage) where one input of each multiplier is connected to a 32-bit software controllable register (SCR). The other input is the ADC channel. All these software configurable registers are first set to 1 to determine the calibration gains of each RF chain for a reference input. Once the calibration gains are determined for each channel, each SCR is overridden with the corresponding gain value.

After the digital normalizing stage, the signals are driven to the ADFT/FFT digital cores. The in-phase signals are fed to the real inputs of the core and the quadrature signals are input to the imaginary outputs. Next, the real and imaginary outputs of the corresponding output bin of the digital FFT core are sent for calculating the instantaneous power of the sample. This is achieved by performing $(Re\{Y_k\})^2 + (Im\{Y_k\})^2$ where $0 \leq k \leq N - 1$. This is implemented with two mul-

multipliers and one adder per channel. The word length of the input to this block will depend on the bit growth due to the ADFT/FFT core. The output from this block will be sent to an accumulator to integrate over a pre-specified time period. The time of integration is designed to be modifiable through software control.

The beam measurement was done by performing the functionality of a lock-in amplifier to filter out ambient 2.4-GHz radiation present in the environment. To achieve this, the transmitted signal will be switched on and off at a particular rate, and the energy level received when the transmitter is on and off are calculated separately. The transmitter design approach is discussed at the end of the Section 3.6.4. The digital circuit architecture shown in Fig. 3.10 has been designed to work with the lock-in amplifier setup. For this purpose, two integrators will be used for each channel and these integrators are activated depending on whether the transmitted signal is on or off. An energy detector is employed at the front of the circuit to achieve this functionality. The Boolean output from this block will be used as a select signal of a demultiplexer (or demux) that selects one of the integrators when the RF is on and the other when RF is off. Finally, the difference of the two integrator values is computed as the received energy of a particular bin. This eliminates the effect of any RF interference in the ambient. Computed values are updated in FPGA memory and then are read to the host server using the software routines.

Calibration

The circuits required calibration to achieve proper functionality prior to obtaining measurements. Calibration was essential at two main points. First, each RF receiver needed to be calibrated due to the mismatches present in amplification, mixing and filtering. In addition, calibration of the ADC chips integrated into the ROACH-2

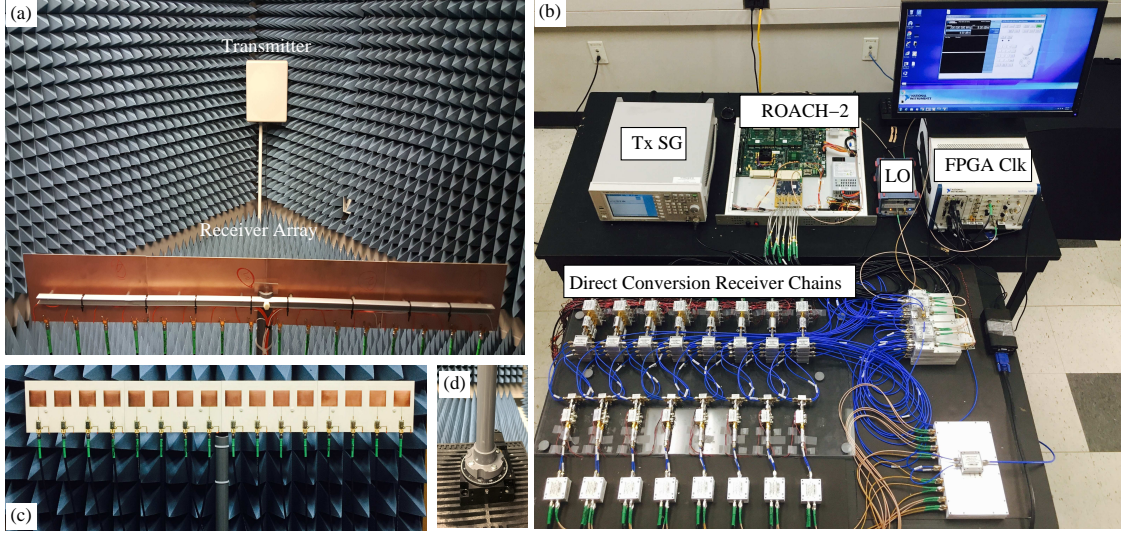


Figure 3.11: Experimental setup: (a) transmitter and receiver in the anechoic chamber, (b) receiver instrumentation setup including the RF receivers, (c) front-view of the antenna array, (d) rotation platform.

platform was required. Calibration of the ADC chips was performed with calibration scripts provided by CASPER [118]. These scripts facilitated calibration for a reference input signal of the same dynamic range as the actual input. A separate microwave circuit was included in the RF front end to achieve this and calibration of the RF front ends was achieved as well.

Due to mismatches of the 32 RF chains of the current setup, the chain outputs to a reference input signal were not uniform. Thus, the gain and phase variations of each channel with respect to a reference input were recorded and were used to calibrate each RF chain digitally as shown in Fig. 3.10 to equalize the outputs of all chains.

3.6.4 Experimental Setup and Beam Measurements

Fig. 3.11 shows the total experimental setup built for experimental verification of the low-complexity beams from the ADFTs. As shown in Fig. 3.11(a), the 16-element 2.4 GHz receiver array was placed inside an anechoic chamber. A 2.4-GHz transmitter antenna was employed at one end of the chamber to generate a plane wave tone. Transmitter and the receiver array were separated approximately by 3 meters to approximately put the receiver array in the far field of the transmitter. The transmitter was remained fixed and the receiver array was rotated around its center using a precision rotation platform controlled by software to take measurements of the received energy level for different angles. Fig. 3.11 (c) and (d) show a close up of the receiver array inside the anechoic chamber and the precision rotation platform used to rotate the array, respectively. The RF-chains, digital back-end, and other equipments are placed outside the anechoic chamber. The antenna array fed the receiver chains via coaxial cables. The LO was fixed at 2.39 GHz to generate an 10 MHz IF. The third oscillator was used to clock the ROACH-2 (FPGA) at 240 MHz and to perform the parallel sampling of all 16 IQ IF channels. Local oscillator signal was generated using a “NOISE XT SL” low jitter clock synthesizer to minimize the phase noise associated in the sampled channels. All oscillators were referenced to a 10 MHz reference clock to further minimize the effect of phase noise generated from oscillators. The ROACH-2 FPGA platform was connected to a host Linux server for software control of the measurement setup. The calculated energy measures (for each output bin of approximate/exact DFT) for each angle of reception were recorded in FPGA block RAMs and were read through software routines to generate the beam pattern. The measurements were conducted in 0.9° steps.

A fully Python based software controlled system has been developed to perform the beam measurement task in full automated manner on top of the software-to-

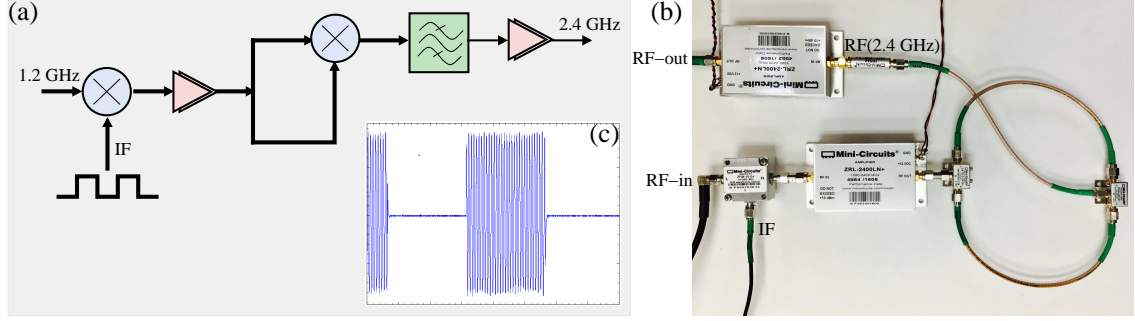


Figure 3.12: Lock-in amplifier design made for generating the transmitted signal with on-off keying..

hardware interface layer provided by the ROACH-2 platform. A sub Python routine was developed to control the motor for precise rotation of the array for beam angle measurements. The “8SMC4-USB” motor controlling platform [119] was used to issue commands from software routines to the platform via a virtual COM-port. ROACH-2 platform provides a middle layer to communicate between the FPGA hardware (block RAM memory) by connecting via the on-board Power PC computer. ROACH-2 is connected to the main host Linux server through an Ethernet connection. The main Python routine is programmed to access the ROACH-2 platform to perform control functions and read data from the FPGA memory while iteratively scanning through the angles. All together, this constitute a fully automated beam measurement setup, allowing all beam measurements to be performed in a single run.

Lock-in Amplifier Setup for Obtaining Measurements

The transmitter component of the test setup was modified to realize a lock-in amplifier behavior to improve the measurement from any potential reflections or ambient 2.4-GHz radiation present in the room environment. For this purpose, the transmitting signal was converted to a continuous on-off pulse of a 2.4-GHz signal. Fig.

3.12 (a) shows the block diagram of the hardware configuration used to generate such transmitted signal. Instead of directly using a 2.4-GHz signal input, a 1.2-GHz signal was used. This signal was modulated to on-off keying by using an IF signal generated from another FPGA board (Xilinx Xtreme DSP kit 4 [120]) via its digital to analog converter (DAC). This signal was then split, mixed, and bandpass filtered to obtain the 2.4-GHz continuous pulse signal. Fig. 3.12(b) shows the COTS component realization of the transmitted signal generation circuit using commercially available mixers and amplifiers. The energy detector block shown in the digital circuit architecture in Fig. 3.10 was used to detect the presence of the carrier. Fig. 3.12 (c) shows a capture of samples from FPGA corresponding to such transmission.

3.6.5 Measured Beams

8-Point Beam Measurements

The center 8-elements of the 16-element array were used to test and measure the beams obtained using the 8-point approximate transform. The digital design architecture shown in Fig. 3.10 was used with the 8-point ADFT/FFT digital cores. The precision rotor stage was used to obtain the received energy for a resolution of 1° ranging from -65° s to $+65^\circ$ s of array broadside. Once the array is moved to a new position, all the integrators were reset and integration was started on all the beam output signals simultaneously to a fixed amount of time (5s). The computed values were then stored in the BRAMs of the FPGA. The recorded values were communicated to the host PC through Python routines.

The process was repeated for each angle according to the rotation resolution used, and the stored values were plotted in Matlab to generate the beam patterns. Same procedure is repeated using both ADFT and DFT cores for comparison.

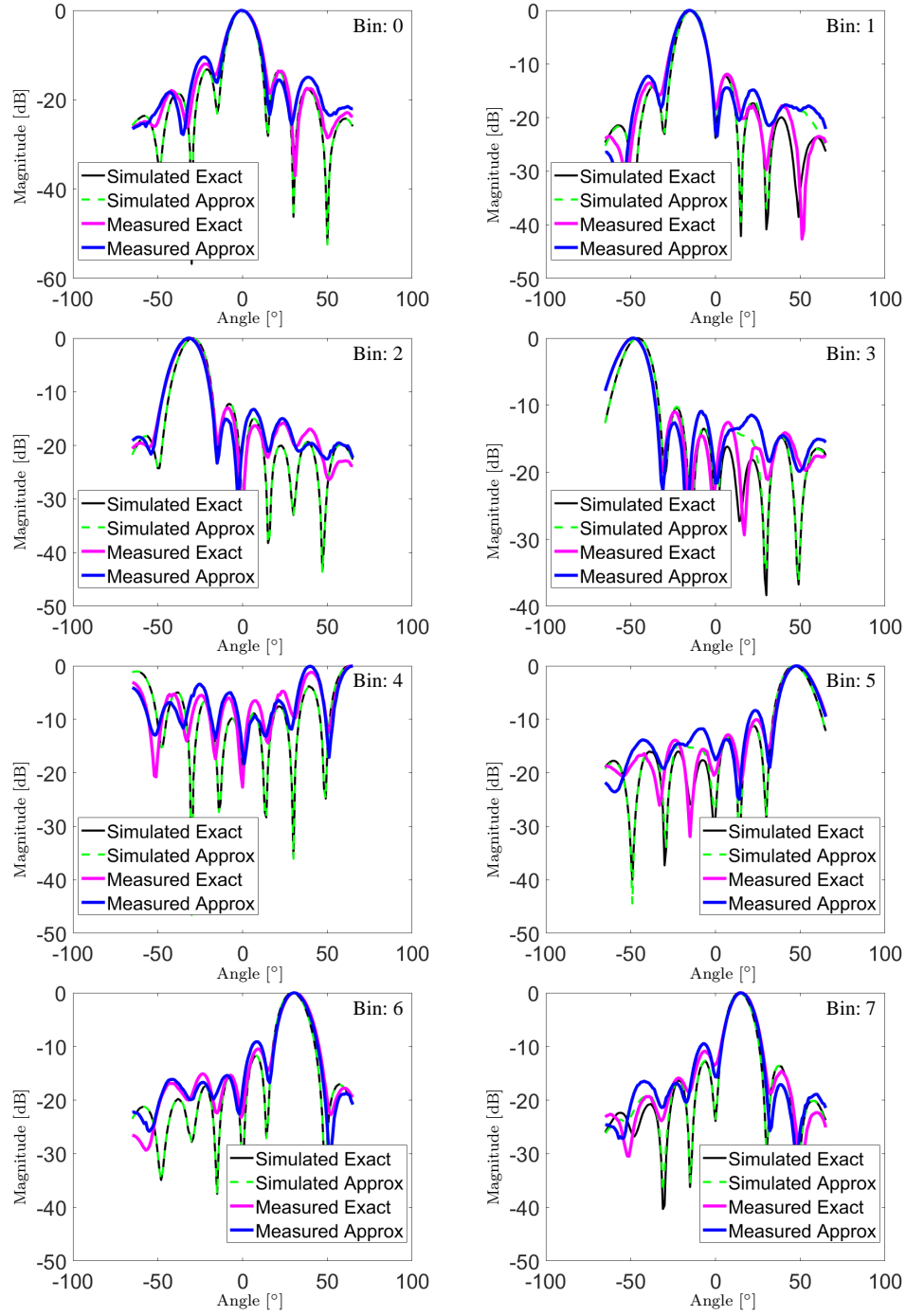


Figure 3.13: Measured and simulated beam patterns for each bin of 8-point approximate and exact transforms.

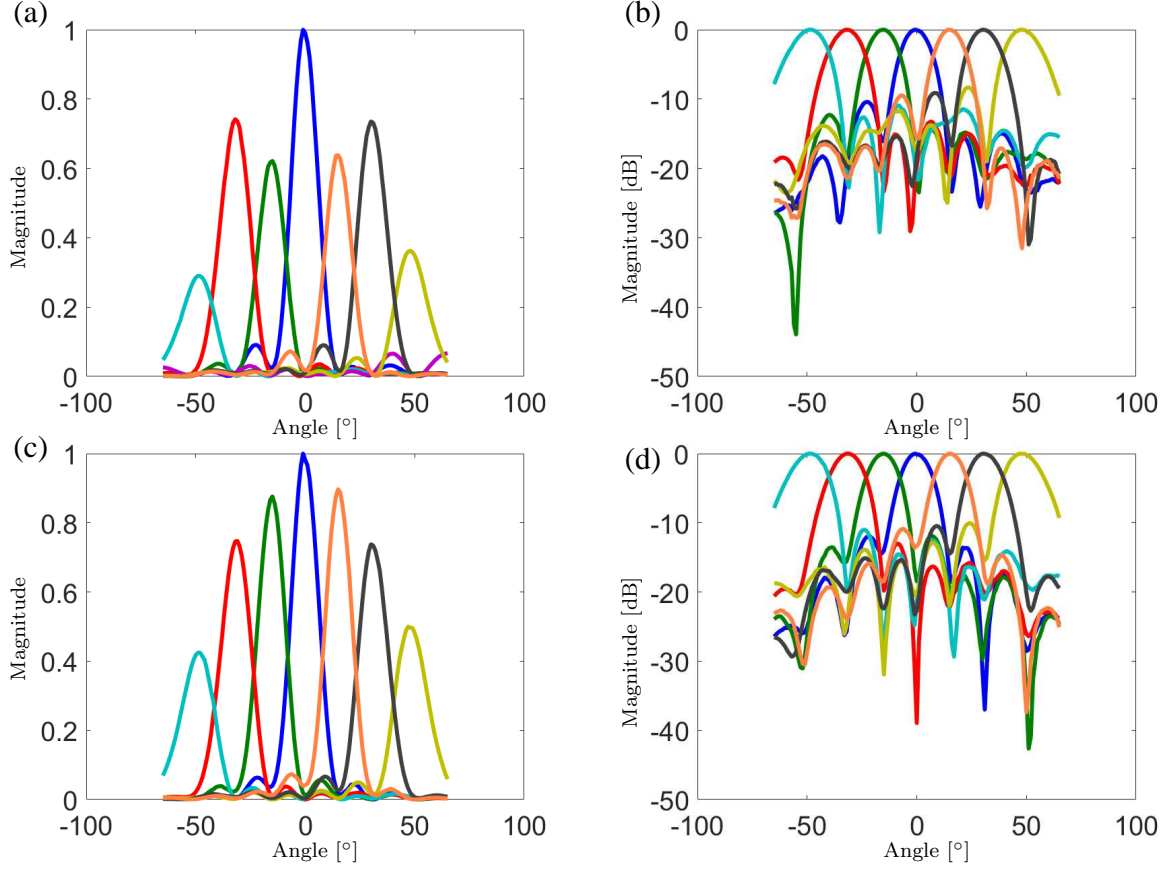


Figure 3.14: (a) All beam patterns using the approximate transform from the raw values measured at each bin output, (b) The normalized beam patterns in the log domain for the approximate transform, (c) All beam patterns obtained using the the exact FFT core, (d) The normalized patterns of (c) in the log domain.

Fig. 3.13 shows the plots generated from the measured values. The digital circuits were clocked at 200 MHz. The LO signal was maintained at 2.410 GHz generating a 10-MHz IF signal to the FPGA ADC inputs. As a reference, Matlab-simulated beam patterns for each transform (approximate and exact) are also plotted, taking the element pattern into consideration. That is, the resultant beam pattern of the ideal beam pattern resulting from the transform and the element pattern is generated. To make simulated patterns more realistic, a time domain simulation has been conducted taking the measured element pattern of each antenna into account

by scaling the signal at each antenna element by using the gain corresponding to the direction of reception. It should be noted that the plot containing Bin 4 is only shown for completeness. The beam direction for this bin is at the end-fire (90° due to the $\lambda/2$ geometry chosen) which falls into the null direction of each antenna pattern. Fig. 3.14 shows all the beam patterns in single plots. Fig. 3.14(a) shows the observed beam patterns using the approximate transform with the use of raw values measured at each bin output. It can be noticed that bins 1,2 and 6,7 do not follow the element pattern due to non-uniform gains inherent in the approximate transform. Fig. 3.14(b) shows the normalized beam patterns for the same beams in the log domain, where each beam output has been normalized to 1 by dividing by each beam's maximum value. Fig. 3.14(c) shows the beam patterns observed from the exact FFT implementation. Fig. 3.14(d) depicts the normalized beam patterns in the log domain. It should be noted that the end-fire beam corresponding to the beam output of bin:4 has been ignored in these plots.

16-Point Beam Measurements

The same measurement procedure was repeated using the full 16-elements of the array along with the implemented 16-point digital cores to obtain the beam measurements. For reference, the beams arising using the exact-FFT digital core were also measured. It is a critical fact that the separation between transmitter and the receiver needs to be high enough to ensure the assumption that a plane wave is received by the array. This is important to obtain a good measurement of the beam patterns. During broadside calibration it was observed that a significant phase deviation existed between the signals captured at two end-fire elements. This is due to the fact that the physical aperture size of the full 16-element array (96 cm) is comparable to the distance between the transmitter and receiver. Figs. 3.15

and 3.16 show the individual beam plots arising from the measured values for both approximate and exact transforms. The transmitter and the receiver separation is constrained to the dimensions of the anechoic chamber and this issue has affected as an increased side-lobe level of the the measured result for both transforms. The simulated beam patterns for each transform have been plotted taking the element pattern into consideration as in the 8-point case. Bin 8 in Fig. 3.16 corresponds to the beam looking at the end-fire which falls into the null direction of each antenna pattern and is shown only for completeness.

Fig. 3.17 shows all the beam patterns in single plots. Fig. 3.17 (a) shows the observed beam patterns using the approximate transform with the use of raw values measured at each bin output. As for the case of the beams measured for the 8-point approximate transform, it can be noticed that bins do not follow the element pattern due to non-uniform gains inherent in the approximate transform. Fig. 3.17 (b) shows the normalized beam patterns for the same beams in the log domain, where each beam output has been normalized to 1 by dividing from its maximum value. Fig. 3.17 (c) shows the beam patterns observed from the exact FFT implementation. Fig. 3.17 (d) depicts the normalized beam patterns in the log domain. It should be noted that the end-fire beam corresponding to output of bin:8 has been ignored in these plots.

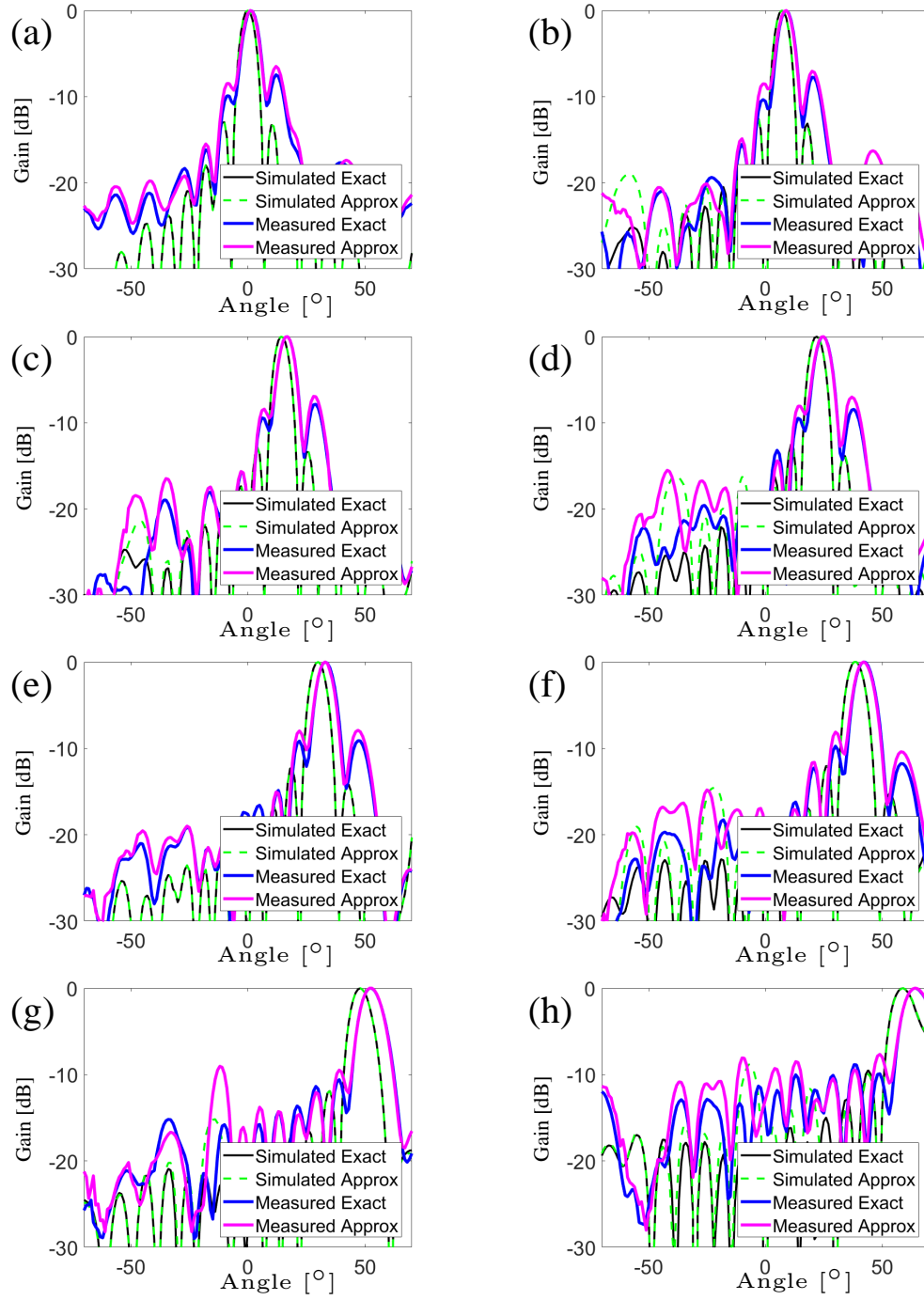


Figure 3.15: Measured beam patterns for bins 0-7 of 16-point approximate and exact transforms.

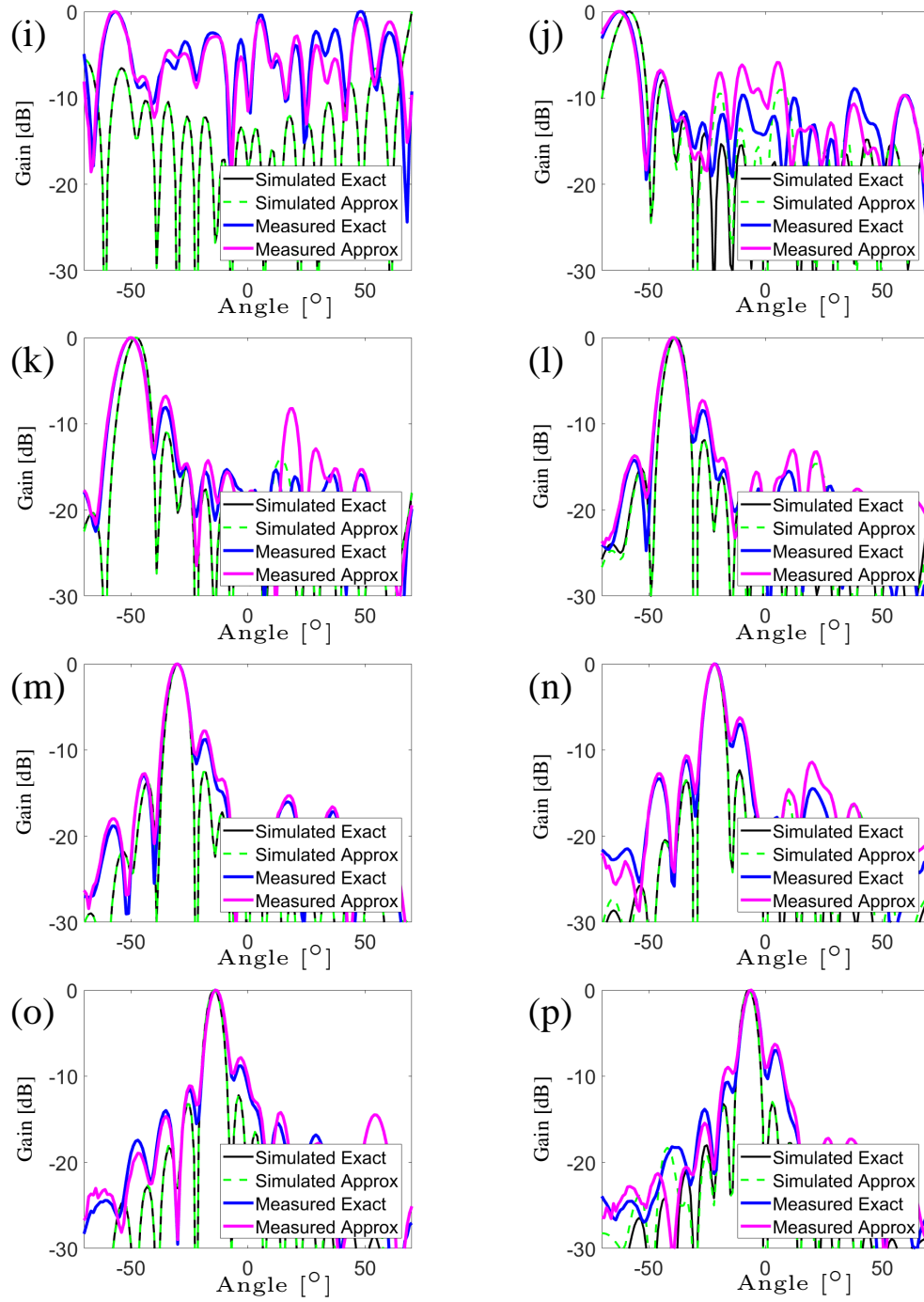


Figure 3.16: Measured beam patterns for bins 8-15 of 16-point approximate and exact transforms.

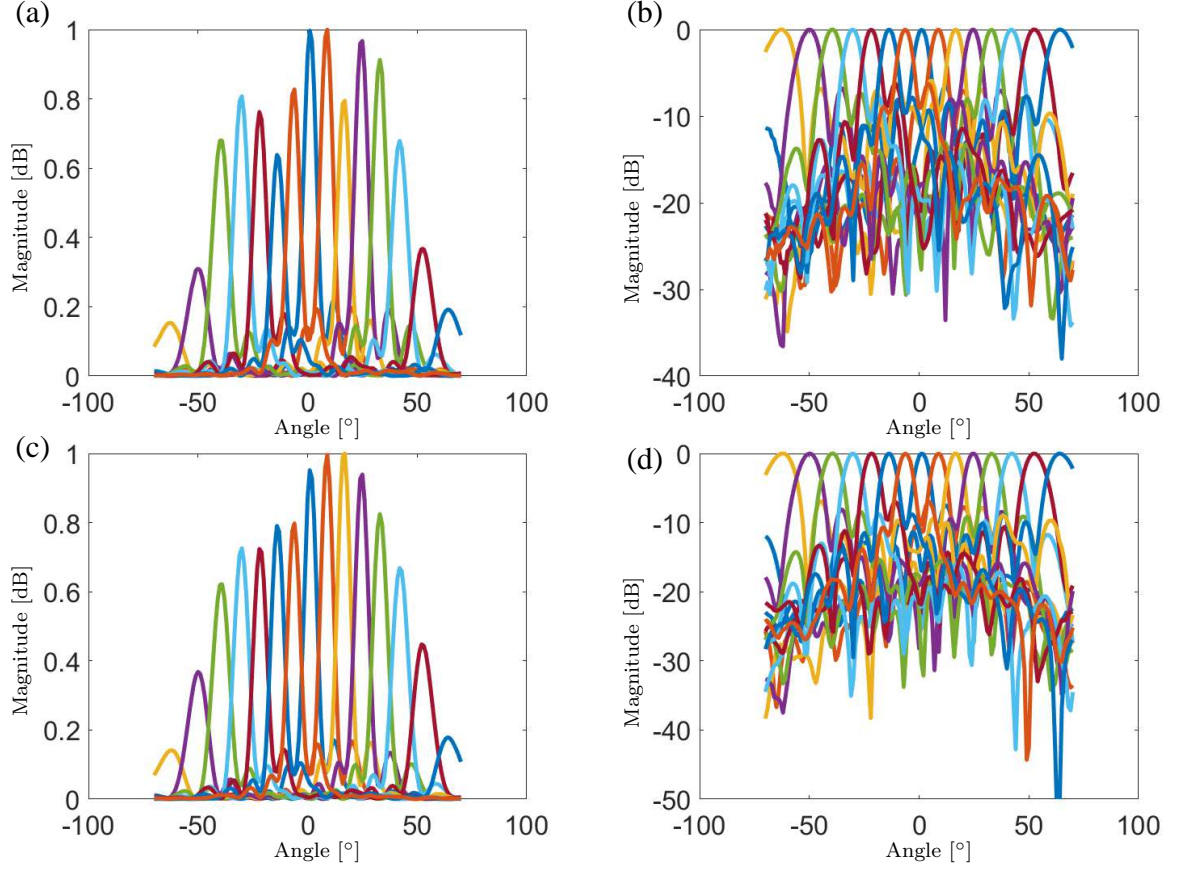


Figure 3.17: (a) All beam patterns drawn in one plot using the 16-point approximate transform from the raw measured values at each bin's output, (b) the normalized beam patterns (log domain) for the approximate transform, (c) all beam patterns obtained using the the exact FFT core, (d) normalized patterns of (c) in the log domain.

It can be observed that measured beam patterns using the 8-point are much closer to the simulated beams than that of the 16-point beam measurements. The performance of the beams is mainly determined by the performance of the analog front-end of the beamformer. The cable length mismatches and the phase incoherence of receiver chains deteriorates the performance of the beams. Apart from that the ideal measurement of a beam would require an ideal plain wave impinging on the receiver array. For a lab anechoic measurement environment, having limited separation between the transmitter and the receiver affects the beam measurement

as the receiver aperture size increases. This is due to the fact that the path length to each element of the receiver array being different from the transmitter for finite size receiver apertures (the receive aperture here is $\approx 1\text{m}$ and the separation of the transmitter and the receiver is $\approx 3\text{m}$). Therefore, owing to the experimental measurement setting conditions ideal plain wave simulated beam performance cannot be achieved.

3.7 Conclusion

A low-complexity 8- and 16-beam multibeam beamformers have been proposed and implemented based on the multiplierless approximate DFT algorithms. The ADFTs have been obtained through the solution of constrained discrete optimization problem resulting from the DFT matrix parameterization and are much lower in complexity than the fixed-point FFT counter parts while maintaining the mathematical properties of the exact DFT. The proposed DFT approximation's for multibeam applications together with their fast algorithm enables digital realizations using only additions and bit shifts and therefore, brings down the lower bound on the multiplication complexity from $\mathcal{O}(N \log N)$ to zero.

An FPGA based digital realization of the proposed low-complexity 16-point ADFT was obtained for 16 achieving simultaneous RF beams. These RF beams were measured and verified using a 16-element 2.4 GHz array setup which generated the complex-valued (IQ) signals as the input to the FPGA implemented digital cores. The FPGA realization of the digital beamformer supports 120 MHz bandwidth per beam. Sampling and the digital realizations were based on the ROACH-2 platform which integrated a Xilinx Virtex-6 FPGA. The beams generated from the outputs of the approximate DFT transforms were measured by rotating the receiver

antenna array and were compared against the beams generated from the fixed-point (8-bit twiddle factors) FFT counter part digital cores. The measured beams for both the cases (ADFT and fixed-point FFT) with comparison to the floating point theoretical beams have been reported. It can be seen that the beams corresponding to the approximate DFT transform are in good agreement with the beams corresponding to the fixed-point FFT. The performance of the beamformer is dominated by the post-calibration phase errors in the microwave front-ends.

The future work can be directed towards investigation of larger ADFTs and realization at emerging mm-wave bands.

CHAPTER 4

LOW-COMPLEXITY 32-BEAM MULTIBEAM SYSTEM: BUILDING BLOCK FOR A MULTIPLIERLESS 1024-BEAM DIGITAL ARRAY

This chapter extends the work in 3 to investigate a low-complexity multiplication-free 32-point digital computing architecture that can form 32-multiple simultaneous RF beams that would lead towards the realization of a 1024 2D low-size-weight-and-power (SWaP) RF beams. Arithmetic complexity due to multiplication is reduced from the FFT complexity of $\mathcal{O}(N \log N)$ for DFT realizations, down to zero, thus yielding a 46% and 55% reduction in chip area and dynamic power consumption, respectively, for the $N = 32$ case. The chapter describes the the proposed 32-point DFT approximation targeting 1024-beams using a 2D uniform rectangular array, and shows the multiplierless approximation and its mapping to a 32-beam sub-system consisting of 5.8 GHz antennas that can be used for generating 1024 digital beams without multiplications. Real-time beam computation is achieved using the ROACH-2 FPGA platform at 120 MHz bandwidth per beam. Theoretical beam performance is compared with measured RF patterns from both a fixed-point FFT as well as the proposed multiplier-free algorithm.

4.1 Introduction

A novel low-complexity multibeam architecture for realizing a massive number of simultaneous sharp beams, which are vitally important in coping with the rapid increases in path loss expected in future mmW/sub-THz wireless systems is proposed. In particular, a low-SWaP approach for generating 1024 beams using a 32×32 aperture and ultra-low-complexity digital VLSI hardware is discussed. A 32-beam subsystem based is proposed based on a novel 32-point DFT approximation as the building block of such a 32×32 system. The proposed 32-beam subsystem has been

implemented at 5.8 GHz and the digital beams have measured and compared with those from exact-DFT-based beams. The measured beams have been used to derive the beam patterns of the corresponding 32×32 rectangular aperture by assuming identical element patterns in all directions.

4.2 2D DFT based Multibeam Transceivers

Following the discussion from the ULA based multibeam beamforming using the spatial DFT in Chapter 3, the discussion is extended to achieving multiple simultaneous beams using 2D uniform rectangular arrays in this chapter. Multibeam on an $N \times M$ ($N, M \in \mathbb{Z}^+$) linearly spaced rectangular array can be achieved by uniformly sampling the spatial frequency domains to define a set of far-field plane-waves having spatial frequencies determined by setting $(\omega_x, \omega_y) = (\frac{2\pi}{N}k_1, \frac{2\pi}{M}k_2)$ where $k_1 = 0, 1, \dots, M-1$ and $k_2 = 0, 1, \dots, N-1$. For this analysis carried out in this chapter, the case where $M = N$ is considered so that the same proposed N -point transform can be used row-wise and column-wise in a rectangular aperture for generating 2D beams. The spatial frequency points $(\frac{2\pi}{N}k_1, \frac{2\pi}{N}k_2)$ correspond to beams pointing at unique angle pairs indexed by $(k_1, k_2) \in \mathbb{Z}^2$. The corresponding spatially-sampled time-continuous plane waves at the terminals of the array elements can be expressed in a Fourier basis as,

$$E(n_x, n_y, t) = E_0 \sum_{k_1=0}^{N-1} \sum_{k_2=0}^{N-1} x_m(t) e^{j(n_x \omega_x + n_y \omega_y + 2\pi f_c t)} \quad (4.1)$$

where f_c is the unmodulated carrier frequency, E_0 is a constant that sets the signal power, and $x_m(t)$ is the complex modulated information component of the signal. It is assumed that the bandwidth of $x_m(t)$ is much smaller than f_c and the analysis is only valid for narrowband signals for which the so-called *spatial-wideband effect* is negligible [121, 122].

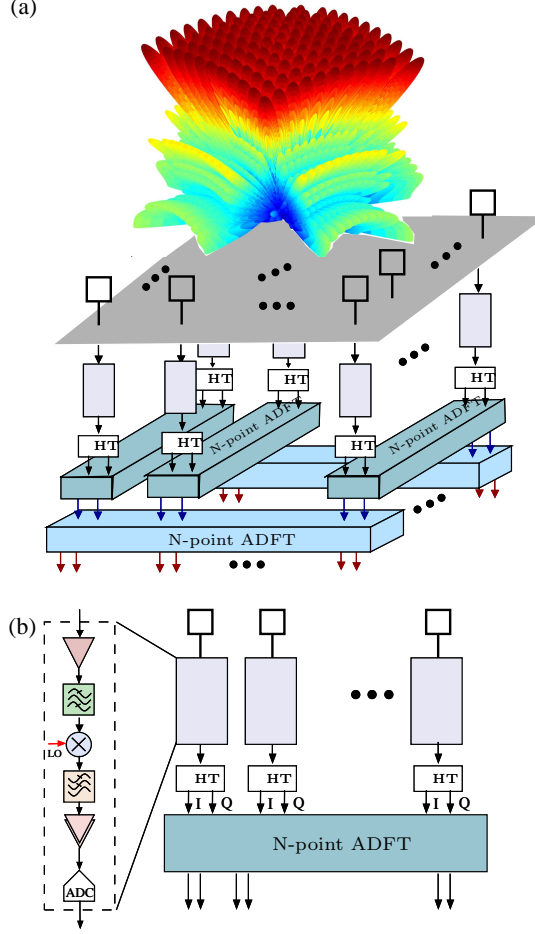


Figure 4.1: (a) Digital beamforming architecture for obtaining N^2 beams using an $N \times N$ URA. (b) Block diagram of a N -element sub-system that acts as a building block for the N^2 rectangular aperture array. The block named HT in the figure denotes the Hilbert transform operation.

In receiver mode, the plane-waves present at the antennas are sampled in the spatial domain, amplified and filtered, down-converted to baseband (or an IF), and finally digitized by an ADC present at each array location. The digitized signals at each location is complex, i.e., has I and Q components. For example, down-conversion using a quadrature mixer (which is modeled as multiplication by $e^{-j2\pi f_c t}$) leaves the spatial frequency components intact as implied by (4.2)

$$E_{BB}(n_x, n_y, t) = x_{m,k}(t)e^{j(n_x\omega_x + n_y\omega_y)} \quad (4.2)$$

As a result, the spatial spectrum of the wave remains localized at (ω_x, ω_y) . The creation of a sharp RF beam for extracting directional information for a particular plane-wave therefore involves the application of a 2D spatial bandpass filter having the sharpest possible selectivity centered on a particular frequency pair in the spatial frequency domain. As discussed in chapter 3 the DFT realizes a filter bank of FIR filters with sharp bandpass responses that take the well-known $\text{sinc}(\omega)$ response shape; the peak stopband magnitude for this shape has an asymptote of to -13.25 dB for increasing filter order N . Therefore, to simultaneously receive an $N \times N$ array of signals, the multibeam beamformer must compute the 2D DFT spatially across the n_x, n_y dimensions of the array.

For transmit applications, the waves to be transmitted at simultaneous multiple directions are applied to the inputs of the 2D inverse DFT (IDFT), with the corresponding IDFT outputs being converted to analog using digital to analog converters (DAC)s, filtered, up-converted to the desired carrier frequency, and amplified before being applied to the input terminals of the transmit array.

Fig. 4.1(a) shows the digital beamforming architecture for an $N \times N$ uniform rectangular array (URA) that generates N^2 beams. The block diagram of an N -element ULA subsystem that acts as a building block for the N^2 URA is shown in Fig. 4.1(b). It is noted that a Hilbert transform block is shown in the Fig. 4.1 to transform the real signals to complex. This is one alternative of achieving the transformation when quadrature downconversion is not used in the analog path. One other method to achieve the same is to use digital quadrature down conversion directly on the low-IF input. Using analog quadrature mixing provides the luxury of using the full ADC bandwidth in a system where as the digital down conversion (DDC) based approaches lose half of the ADC bandwidth.

As it has been discussed in detail in Chapter 3, the direct computation of the DFT of an N -point vector of input values requires a number of complex arithmetic operation in $\mathcal{O}(N^2)$, and it was also explained in Chapter 3 that using the symmetries of the N -point DFT matrix \mathbf{F}_N , it is possible to compute the matrix-vector product $\mathbf{X} = \mathbf{F}_N \cdot \mathbf{x}$ with order $\mathcal{O}(N \log N)$ complex arithmetic operations using the FFT algorithms. FFTs achieve this saving by the use of fast algorithms based on sparse matrix factorizations. The complexity reduction from $\mathcal{O}(N^2)$ to $\mathcal{O}(N \log N)$ is substantial as N grows large.

4.3 A 32-point DFT Approximation and Fast Algorithm for RF Beamforming

4.3.1 32-point Approximate DFT

A 32-point approximate DFT matrix $\hat{\mathbf{F}}_{32}$ is proposed for which the matrix-vector multiplication operation in computing the RF beams can be computed without multipliers. Let \mathbb{P} be the set $\{0, \pm 1, \pm 2, \pm 1/2\}$. Let $\mathcal{M}_{\mathbb{P}^2}(32)$ be the set of 32×32 complex matrices such that the real and the imaginary parts are defined over the set \mathbb{P} . The approximate transform $\hat{\mathbf{F}}_{32}$ can be found according to a multi-criterion optimization considering the search space represented by the parametrized mapping below:

$$\begin{aligned} g : \mathbb{R} &\longrightarrow \mathcal{M}_{\mathbb{P}^2}(32), \\ \beta &\longmapsto \text{round}(\beta \cdot \mathbf{F}_{32}) \end{aligned}$$

and objective functions given by the following selected matrix-based metrics:

- (i) Frobenius norm of the matrix difference, (ii) total error energy, (iii) average

percent absolute error, and (iv) orthogonality deviation. The optimal solution for the above DFT approximation has been found by determination of the Pareto efficient solution set, which is the set of non-dominant solutions [123] using $\beta \in (0, 5]$ with steps of 10^{-2} by UPFE collaborators [104].

The found optimal matrix resulting from the above optimization problem is given in (4.3). Due to the large matrix size of 32×32 , the matrix is represented as \mathbf{A}_i , $i \in \{0, 1, 2, 3\}$ 16×16 sub-matrices given by equation set (4.4) [104].

$$\hat{\mathbf{F}}_{32} = \begin{bmatrix} \mathbf{A}_0 & \mathbf{A}_1 \\ \mathbf{A}_2 & \mathbf{A}_3 \end{bmatrix}, \quad (4.3)$$

Among the efficient solutions, the matrix $\hat{\mathbf{F}}_{32}$ exhibits the smallest total error energy of approximately $3.32 \cdot 10^2$. The Frobenius norm of the matrix error *per matrix element* $\frac{1}{32^2} \|\hat{\mathbf{F}}_{32} - \mathbf{F}_{32}\|_F = 1.004 \cdot 10^{-2}$, where $\|\cdot\|_F$ is the Frobenius norm. This measurement is 54.9% lower than the error per element of the DFT approximation described in [105, 124, 125] and is regarded to be acceptable for beamforming applications.

Fig. 4.2 shows a comparison of the frequency responses of all the bins for the 32-point proposed approximate DFT and the DFT. The shapes and locations of the main beams are almost identical to the exact DFT. The relative errors of the magnitude response of each filter response are largely confined to the stopbands away from the main lobe (i.e., deep side lobes), and are generally below the -15 dB level. Fig. 4.2(c) shows the magnitude error plot of the filter bank responses of the proposed DFT approximation. The plot in Fig. 4.2(c) is computed by evaluating the difference of the magnitude responses of approximate and exact DFT transforms for each filter (i.e., DFT/ADFT bin). The plots in Fig. 4.3 show the bins in Fig. 4.2(c) that have the highest magnitude error. All other bins have a magnitude error that

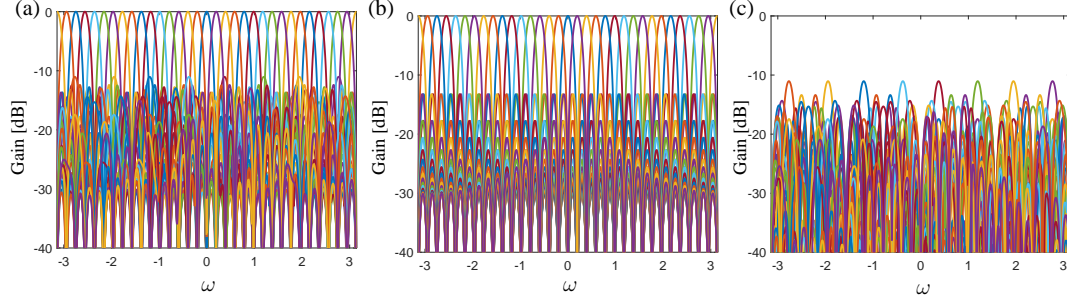


Figure 4.2: The simulated frequency responses of the 32 output bins of the (a) proposed 32-point ADFT, (b) exact DFT; (c) the magnitude error of the two responses.

It is also noted that similar to the 16-beam algorithm discussed in Chapter 3, the proposed approximation would also not directly work with conventional windowing functions due to its numerical structure. However, these functions can be modified to achieve the desired windowing performance.

4.3.2 Fast Algorithm for Computing the 32-point ADFT

A fast algorithm for computing the approximate transform $\hat{\mathbf{F}}_{32}$ in (4.3) to be used in place of usual FFTs can be derived by means of sparse matrix factorization in a decimation-in-frequency approach [81]. The matrix transform $\hat{\mathbf{F}}_{32}$ has been factorized as shown in (4.5) by the collaborating Brazilian mathematicians.

$$\hat{\mathbf{F}}_{32} = \mathbf{W}_8 \cdot \mathbf{W}_7 \cdot \mathbf{W}_6 \cdot \mathbf{W}_5 \cdot \mathbf{W}_4 \cdot \mathbf{W}_3 \cdot \mathbf{W}_2 \cdot \mathbf{W}_1, \quad (4.5)$$

where \mathbf{W}_i for $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$ are sparse matrices (factorization stages). The non-zero matrix elements of each matrix \mathbf{W}_i are given in Table 4.1 and 4.2. The matrix factorization in (4.5) is not unique (i.e., can admit multiple different factorizations) unlike factorization of a composite integer [126]. The number of stages (i.e., sparse matrices) in the matrix factorization depend on the factorization method employed. The number of stages is not important as long as the overall number of elementary arithmetic operations in the factorized form is lower when

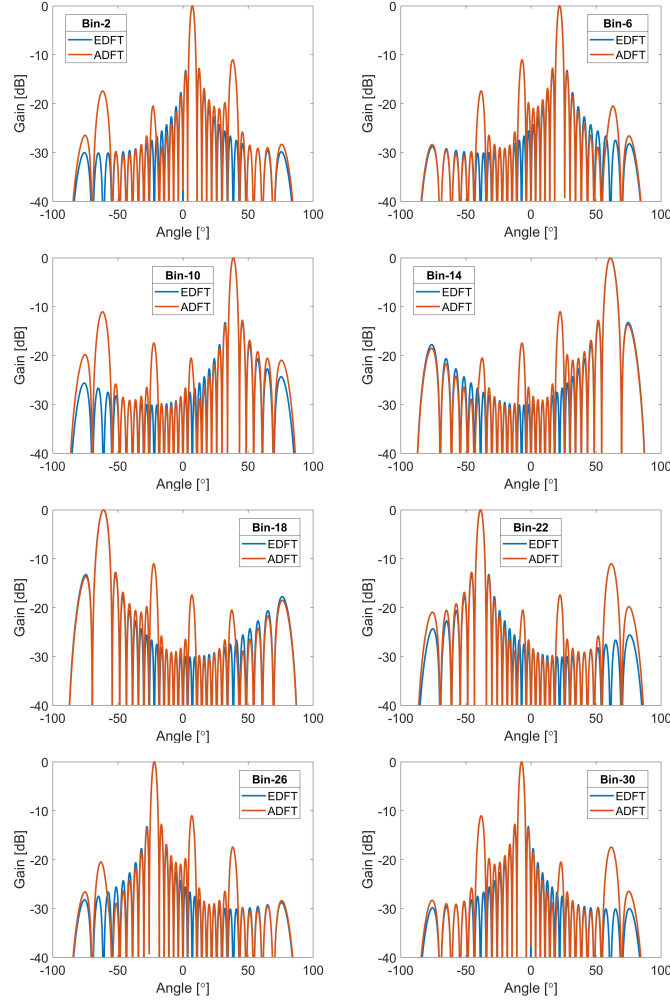


Figure 4.3: Bins that have the highest magnitude error in Fig. 4.2. (c).

compared to the direct non-factorized form of the matrix-vector product. Notice that the entries of the sparse matrices \mathbf{W}_i only contain the elements from the set $\mathbb{P}_0 = \{+1, -1, +j, -j\}$ which imply trivial arithmetic operations in digital implementations. Given the fast algorithm in (4.5), the computational complexity associated with computing can be quantified. Let us consider the complex input signals which correspond to inputs being the I and Q outputs of the received signal from the array to the digital processor and evaluate the arithmetic complexity in terms of real operations. The arithmetic cost of each matrix in each factorization

Table 4.1: Matrix factors \mathbf{W}_1 to \mathbf{W}_4 , represented by their non-zero indexes

Factorized Stage	+1	-1
\mathbf{W}_1	(1,1), (1,17), (2,2), (2,16), (3,3), (3,15), (4,4), (4,14), (5,5), (5,13), (6,6), (6,12), (7,7), (7,11), (8,8), (8,10), (9,9), (10,8), (11,7), (12,6), (13,5), (14,4), (15,3), (16,2), (17,1), (18,18), (18,32), (19,19), (19,31), (20,20), (20,30), (21,21), (21,29), (22,22), (22,28), (23,23), (23,27), (24,24), (24,26), (25,25), (26,24), (27,23), (28,22), (29,21), (30,20), (31,19), (32,18)	(10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)
\mathbf{W}_2	(1,1), (2,2), (2,18), (3,3), (3,19), (4,4), (4,20), (5,5), (5,21), (6,6), (6,22), (7,7), (7,23), (8,8), (8,24), (9,9), (9,25), (10,10), (10,26), (11,11), (11,27), (12,12), (12,28), (13,13), (13,29), (14,14), (14,30), (15,15), (15,31), (16,16), (16,32), (17,17), (18,2), (19,3), (20,4), (21,5), (22,6), (23,7), (24,8), (25,9), (26,10), (27,11), (28,12), (29,13), (30,14), (31,15), (32,16)	(18,18), (19,19), (20,20), (21,21), (22,22), (23,23), (24,24), (25,25), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)
\mathbf{W}_3	(1,1), (1,9), (2,2), (2,8), (3,3), (3,7), (4,4), (4,6), (5,5), (6,4), (7,3), (8,2), (9,1), (10,10), (10,16), (11,11), (11,15), (12,12), (12,14), (13,13), (14,12), (15,11), (16,10), (17,17), (18,18), (19,19), (20,20), (21,21), (22,22), (23,23), (24,24), (25,25), (26,26), (27,27), (28,28), (29,29), (30,30), (31,31), (32,32)	(6,6), (7,7), (8,8), (9,9), (14,14), (15,15), (16,16)
\mathbf{W}_4	(1,1), (1,5), (2,2), (2,4), (3,3), (4,2), (5,1), (6,6), (7,7), (7,9), (8,8), (9,7), (10,10), (11,11), (11,13), (12,12), (13,11), (14,14), (14,16), (15,15), (16,14), (17,17), (17,29), (18,18), (19,19), (20,20), (21,21), (21,25), (22,22), (23,23), (24,24), (25,21), (26,26), (27,27), (28,28), (29,17), (30,30), (31,31), (32,32)	(4,4), (5,5), (9,9), (13,13), (16,16), (25,25), (29,29)

stage of (4.5) is evaluated as described in [81]. Because the coefficients of the real and imaginary parts of \mathbf{W}_i for $i \in \{1, 2, 3, 4, 5, 6, 7, 8\}$ are also in \mathbb{P}_0 , only additions are required. The additive cost is based on the number of nonzero elements the rows

Table 4.2: Matrix factors \mathbf{W}_5 to \mathbf{W}_8 , represented by their non-zero indexes

	+1	-1		
W₅	(1,1), (1,3), (2,2), (3,1), (4,4), (4,5), (5,4), (6,6), (6,9), (7,7), (7,8), (8,7), (9,6), (10,10), (10,13), (11,11), (11,12), (12,11), (13,10), (14,14), (14,15), (15,14), (16,16), (17,31), (18,18), (19,19), (19,25), (20,20), (20,22), (20,24), (21,21), (21,23), (22,20), (23,21), (24,20), (25,19), (26,26), (27,27), (27,29), (28,28), (28,30), (28,32), (29,27), (30,28), (31,17), (31,31), (32,28)	(3,3), (5,5), (8,8), (9,9), (12,12), (13,13), (15,15), (17,17), (22,22), (23,23), (24,24), (25,25), (29,29), (30,30), (32,32)		
W₆	(1,1), (1,2), (2,1), (3,3), (4,4), (5,5), (6,6), (7,7), (8,8), (9,9), (10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (18,18), (18,22), (19,19), (20,20), (20,21), (21,20), (22,18), (23,23), (24,18), (24,24), (25,25), (26,26), (26,30), (27,27), (28,28), (28,31), (29,29), (30,26), (31,28), (32,26), (32,32)	(2,2), (18,24), (21,21), (22,22), (26,32), (30,30), (31,31)		
W₇	(1,1), (2,2), (3,3), (4,4), (5,5), (6,6), (7,7), (8,8), (9,9), (10,10), (11,11), (12,12), (13,13), (14,14), (15,15), (16,16), (17,17), (17,30), (18,18), (18,25), (19,24), (20,20), (21,21), (22,22), (22,23), (23,22), (24,19), (24,24), (25,18), (26,26), (26,27), (27,26), (28,28), (29,29), (29,32), (30,17), (31,31), (32,29)	(19,19), (23,23), (25,25), (27,27), (30,30), (32,32)		
	+1	-1	+j	-j
W₈	(1,1), (2,28), (3,7), (5,4), (6,26), (9,3), (11,9), (15,8), (17,2), (19,8), (23,9), (25,3), (28,26), (29,4), (31,7), (32,28)	(4,29), (7,6), (8,17), (10,30), (12,27), (13,5), (14,32), (16,31), (18,31), (20,32), (21,5), (22,27), (24,30), (26,17), (27,6), (30,29)	(5,14), (13,15), (15,12), (18,21), (20,19), (22,25), (23,13), (24,22), (25,16), (26,23), (27,10), (28,18), (30,24), (31,11), (32,20)	(4,24), (12,25), (14,19), (16,21), (19,12), (21,15)

of each \mathbf{W}_i matrix, as detailed in [81]. Therefore, the matrices \mathbf{W}_1 , \mathbf{W}_2 , and \mathbf{W}_5 require 60 real additions; the matrices \mathbf{W}_3 , \mathbf{W}_4 , and \mathbf{W}_6 require 28 real additions; and the matrix \mathbf{W}_7 requires 24 real additions. The only complex matrix in the factorization, \mathbf{W}_8 , requires 60 real additions. In total, the transform $\hat{\mathbf{F}}_{32}$ requires 348

Table 4.3: Comparison of arithmetic complexities for performing the 32-point DFT using different FFT algorithms

Method	No. of real additions	No. of real multipliers
Radix-2 FFT [81, p. 76]	408	88
Split-Radix FFT [127]	388	68
Winograd FFT [128]	388	68
Direct Computation $\hat{\mathbf{F}}_{32}$	584	0
Fast Algorithm $\hat{\mathbf{F}}_{32}$	348	0

real additions. Table 4.3 shows the real multiplicative and additive costs associated with several well-known FFT algorithms compared with the proposed algorithm. Table 4.3 also shows the additive complexity achieved through the proposed fast algorithm is 40% lower when compared to direct computation of $\hat{\mathbf{F}}_{32}$.

4.3.3 Hardware Metrics of the Proposed ADFT Realization

The 32-point ADFT fast algorithm in (4.5) was realized as a digital core and synthesized using 45 nm CMOS free-PDK standard cells [129]. For comparison purposes, a 32-point FFT core based on the Duhamel algorithm was also implemented in digital and synthesized using the same technology. Both the approximate and fixed point exact FFT digital cores assume inputs of 8-bit word length. The fixed-point exact FFT core was designed with 10-bit twiddle factors [83] which maintains a precision of 2^{-9} in the phasing coefficients. The multiplications throughout the signal paths were handled such that they preserve at least the coefficient precision. Table 4.4 compares the following metrics for the two implementations: chip area A , critical path delay T , maximum clock frequency F_{max} , area-time AT , area-time-squared AT^2 , frequency- and voltage-normalized dynamic power consumption D_p , and maximum side-lobe level. It can be seen that the proposed ADFT algorithm consumes

46% less area than the reference fixed-point FFT design, while achieving a 50% drop in critical path delay. It is also noted that the metrics AT and AT^2 are reduced by 73% and 86%, respectively, where the metric AT is important when area/cost is more important, AT^2 is critical when speed performance is crucial. Note that the speed values mentioned in Table 4.4 are only based on synthesis results, i.e., do not consider layout effects that slow down the performance of physical implementations. However, such effects will be present in both designs, so the relative improvements in AT and AT^2 metrics are expected to remain valid. The compromise is an ≈ 2 dB increase in sidelobe level, which is assumed to be tolerable in most RF beamforming applications where unwanted signals (jammers) can fall on larger sidelobes.

Table 4.4: Comparison of ASIC realization metrics for the proposed ADFT vs a 32-point FFT (Duhamel) using a 45-nm PDK

Metric	Duhamel algorithm	ADFT	Change
Area, A (mm^2)	0.856	0.465	46%↓
Critical path delay, T (ns)	1.73	0.86	50%↓
Frequency, F_{max} (GHz)	0.58	1.16	100%↑
AT ($\text{mm}^2 \cdot \text{ns}$)	1.481	0.400	73%↓
AT^2 ($\text{mm}^2 \cdot \text{ns}^2$)	2.562	0.344	86%↓
Dynamic Power, D_p (mW/GHz)	1303	580	55%↓
Largest side-lobe level (dB)	-13.26	-11.03	2.23↑

**The proposed algorithm achieves $\approx 50\%$ reduction in area and time at the expense of ≈ 2 dB increase in side lobe levels.

4.3.4 N -Beam Beamforming Architectures for ULAs and URAs

Fig. 4.1 shows the top-level hardware architectures for realizing N and N^2 simultaneous orthogonal beams for an N -element and $N \times N$ aperture respectively using an N -point spatial DFT digital core as the basic signal processing block. The front-end is shown as a direct-conversion receiver chain followed by analog-to-digital conversion for digital beamforming. The digitized data can be converted to complex (I - Q) form using a Hilbert transform. This can also be achieved by using a quadrature mixer in the RF chain, with the luxury of going to baseband directly at the cost of double the amount of ADCs.

The numerically simulated array factors resulting from a 32-element spatially Nyquist sampled ULA are given in Fig. 4.4(i). Fig. 4.4(i-b) shows the beams generated using the proposed 32-point ADFT algorithm and Fig. 4.4(i-a) shows the corresponding beams of the exact algorithm with (i-c) showing the error magnitude between them. Fig. 4.4(ii) shows three simulated example beams out of the 1024 beams generated by the proposed ADFT algorithm when it is applied to a 32×32 -element URA. The first and second columns of Fig. 4.4(ii) show the beams corresponding to the exact and approximate DFT, respectively; the third and fourth columns of Fig. 4.4(ii) show the errors between the two algorithms in the elevation and azimuthal planes, respectively, which are small enough to be ignored for most microwave and mm-wave beamforming applications.

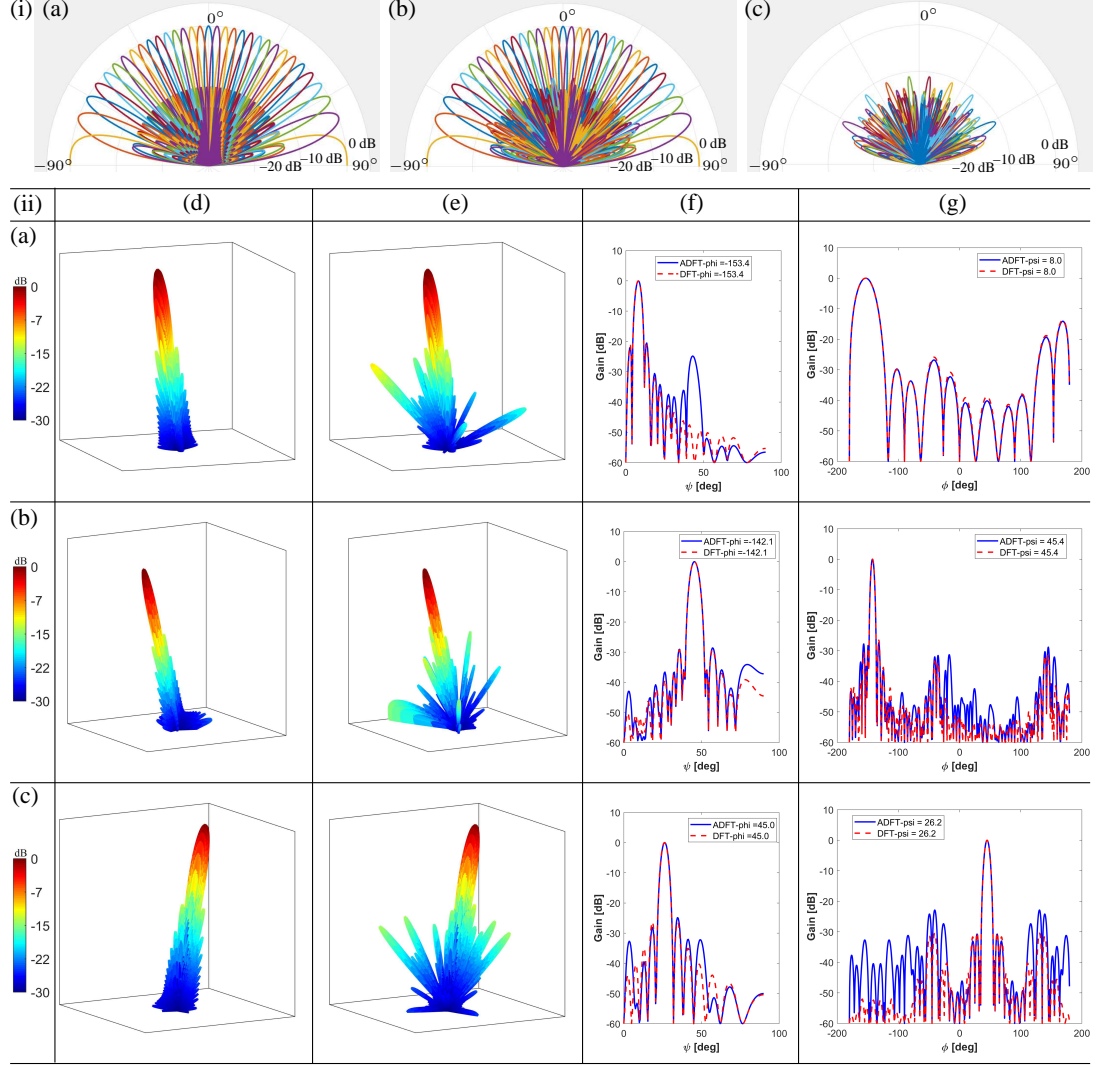


Figure 4.4: (i) Simulated polar patterns of the 32-beams for a ULA with $\lambda/2$ element spacing. (i-a) Beams corresponding to the ADFT, (i-b) beams obtained with the ideal FFT, and (i-c) the magnitude error between the ADFT and the exact FFT. (ii) Example simulated beam patterns from a Nyquist-spaced URA; (a) $\psi = 8.0^\circ$, $\phi = -153.4^\circ$, (b) $\psi = 45.4^\circ$, $\phi = -142.1^\circ$, (c) $\psi = 26.2^\circ$, $\phi = 45.0^\circ$ (the plots are color-coded on a dB scale).

4.4 A 32-Beam ULA-based Multibeam Beamformer

System architecture used for verifying the proposed low-complexity multibeam beamforming algorithm is shown in Fig. 4.5(a). This section explains the system design.

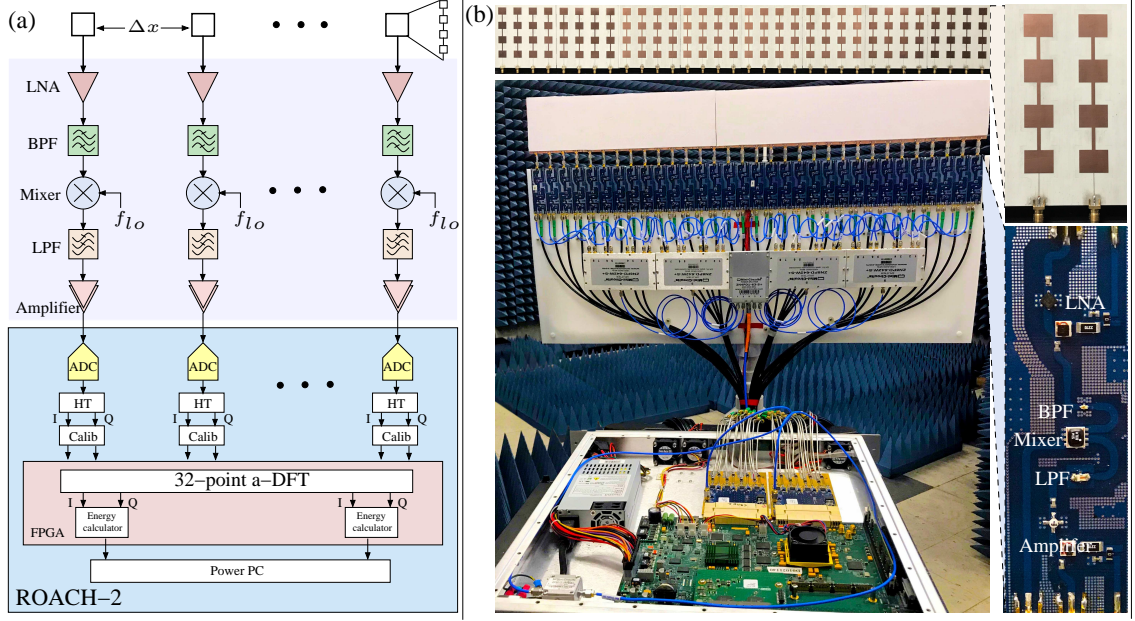


Figure 4.5: (a) Overall architecture of the test setup; (b) 5.8 GHz 32-beam array receiver setup.

4.4.1 5.8 GHz Front-End Design

The RF front-end of the receive-mode beamformer is constructed by integrating a 32-element ULA at 5.8 GHz with 32 direct conversion RF receiver chains (on PCB) as shown in Fig. 4.5(b). The inter-element spacing of the array Δx was set to 0.6λ , which is ≈ 31 mm at 5.8 GHz. The specifics of the antenna design can be found in [130].

Each antenna element of the ULA was designed as a 4×1 vertical sub-array of patch antennas that employs passive beamforming at RF in the orthogonal (vertical) plane. This design improves the gain in the vertical plane, thus simplifying array factor measurements in the azimuthal plane. The sub-array is designed by feeding antenna elements in series along a uniform transmission line, and performing a parametric sweep to provide better impedance matching and performance [131]. Note that such analog beamforming does not affect the performance of the beamforming

algorithm under consideration as it happens in the azimuthal plane. The antenna outputs are directly fed into 32 heterodyne receivers designed on FR-4 PCBs using surface mount devices. The LO signals for each receiver are provided through a centralized LO scheme that consists of a 32-output power divider network connected to a low-phase-noise oscillator. The first stage of each receiver consists of a low-noise amplifier (LNA) that provides 16 dB gain at 5.8 GHz with a noise figure of 2.4 dB. The amplified signal is band-pass filtered within the frequency range 4.7-6 GHz, which helps to reject out-of-band interference and noise. The band-limited amplified signal is then passed through a mixer and low-pass filter to produce a downconverted low-IF input. The 32 downconverted low-IF signals are further amplified by ~ 30 dB and then digitized in parallel using two ADC16x250-8 ADC cards (16 single-ended input channels, 8-bit, up to 250 MS/s per channel) [132]. The in-band gain and noise figure of the entire receiver are estimated to be 38.6 dB and 2.9 dB, respectively; the latter is dominated by the LNA.

A sample clock of 200 MHz was used for clocking the ADCs for real-time hardware experiments. The same clock was also routed to drive the digital circuits implemented on the FPGAs. The digital circuits were pipelined to support clocking at the ADC sample rate.

4.4.2 Digital Back-End

Digital processing and the beamforming were performed using the ROACH-2 platform [117]; which is the same board used for verifying the 16-beam algorithm in Chapter 3. The ADC16x250-8 ADC cards [132] that were also used for the work in Chapter 3 were used for sampling the 32 channels in to digital. Each ADC16x250-8

ADC card supports 16 channels at a max rate of 240 MSps and the ROACH-2 can support 2 such cards.

The overall architecture of the digital beamforming test-setup is shown in Fig. 4.5(a). The digital design consists of four main subsystems: (i) a digital calibration stage; (ii) an IQ decomposition FIR filter that implements the Hilbert transform [103]; (iii) the 32-point DFT/ADFT algorithm implementation; and (iv) an energy calculation subsystem for facilitating real-time measurements on each output beam. The exact DFT core was designed using 10-bit precision twiddle factors which provide a good compromise between circuit size and maximum operating frequency.

4.5 Experimental Results

This section describes experimental results obtained from the 32-element ULA, including antenna characterization and beam measurements.

4.5.1 Antenna Array Characterization

The performance of the array was characterized using S-parameters [133], that were measured using a vector network analyzer. The return loss $|S_{11}|$ of a single patch sub-array was measured as -20.6 dB at 5.9 GHz which was the best resonating point of the antenna.

As described in Chapter 2 mutual coupling is another important factor that has to be considered during the design of an antenna array processor. The mutual coupling (MC) can be characterized using S-parameters for the array [44, 134]. The parameter, $S_{n,m}$ indicates the coupling between the m th and the n th antenna which characterizes the coupling at n th antenna when the m th antenna is excited.

For a general characterization, $S_{14,16}$, $S_{15,16}$, $S_{17,16}$ and $S_{18,16}$ measurements were taken from the 32-element array exiting the 16th antenna while the other antenna ports were terminated with 50Ohm loads. The above mentioned mutual coupling coefficients at 5.8 GHz were recorded as, $|S_{14,16}| = -39.2$ dB, $|S_{15,16}| = -33.2$ dB, $|S_{17,16}| = -33.0$ dB, and $|S_{18,16}| = -37.3$ dB. As expected, mutual coupling decreases with inter-element separation. These mutual coupling parameters have to be ideally considered in the beamforming algorithm to nullify the effects of coupling in the array. Such task needs a separate study and therefore is not investigated in this work. Due to the affect of MC the measured beams will deviate from the expected theoretical behavior.

4.5.2 Calibration

Calibration of the RF array system is vital for obtaining optimal beamforming performance. Calibration was performed in two stages. The first stage was performed on the ADCs, and used open source routines that have already been developed for the same hardware by members of the CASPER group [118]. The second stage focused on digitally removing the effects of mismatches in the microwave front-end. Relative gain and phase mismatches of the IF outputs for each chain were calculated with respect to a reference chain using a input reference carrier at 5.86 GHz. Since the overall system is narrowband, the recorded gain and phase values were directly used to equalize the gain and phase of the sampled IF inputs. This was achieved by adding a complex multiplier after the digital Hilbert transform in each channel.

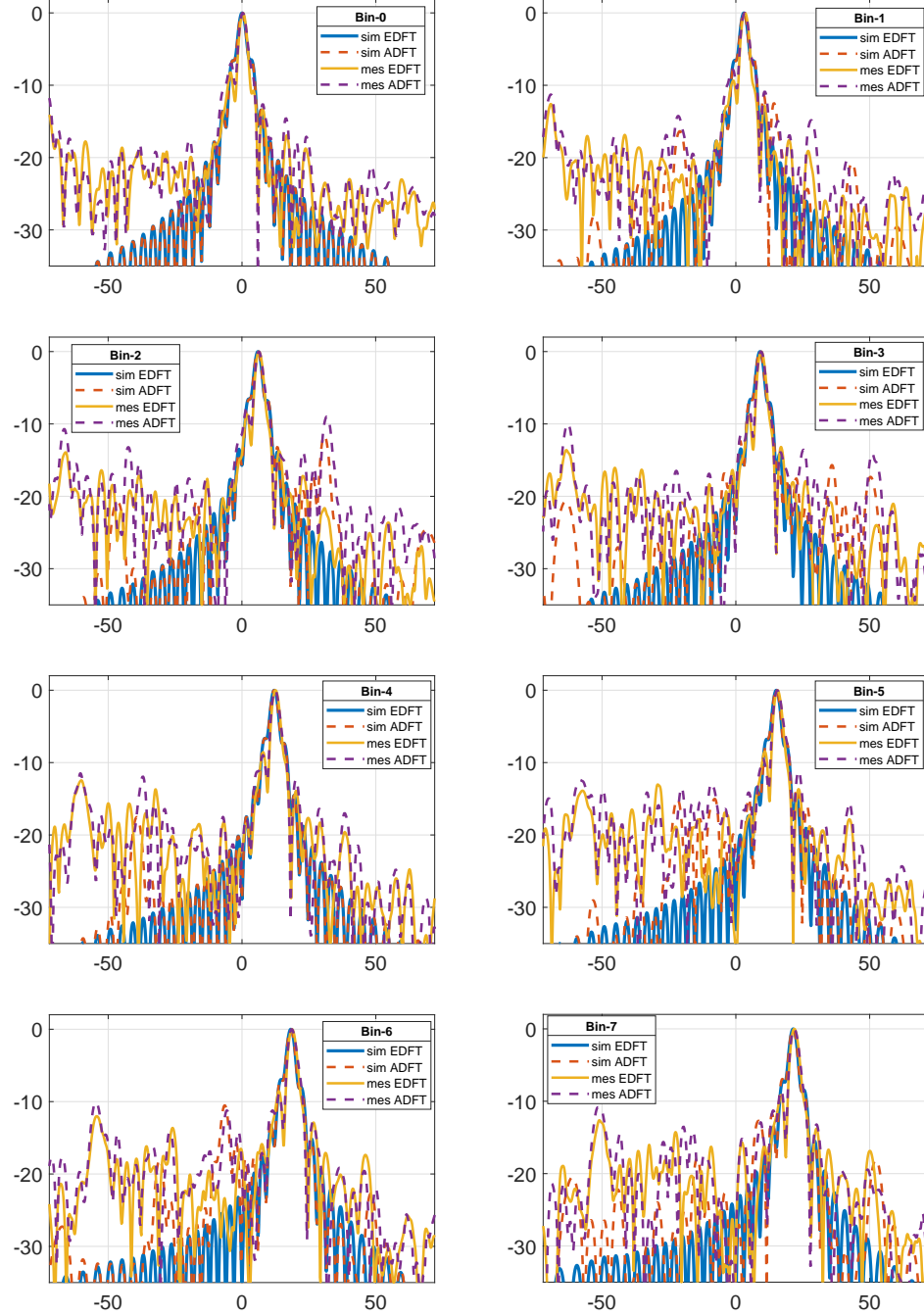


Figure 4.6: The beam outputs at bins 0-7.

4.5.3 Beam Measurements

As shown in Fig. 4.5(b), the entire 5.8 GHz 32-element digital array placed in an anechoic chamber for measuring the received beam patterns ([135] shows a short

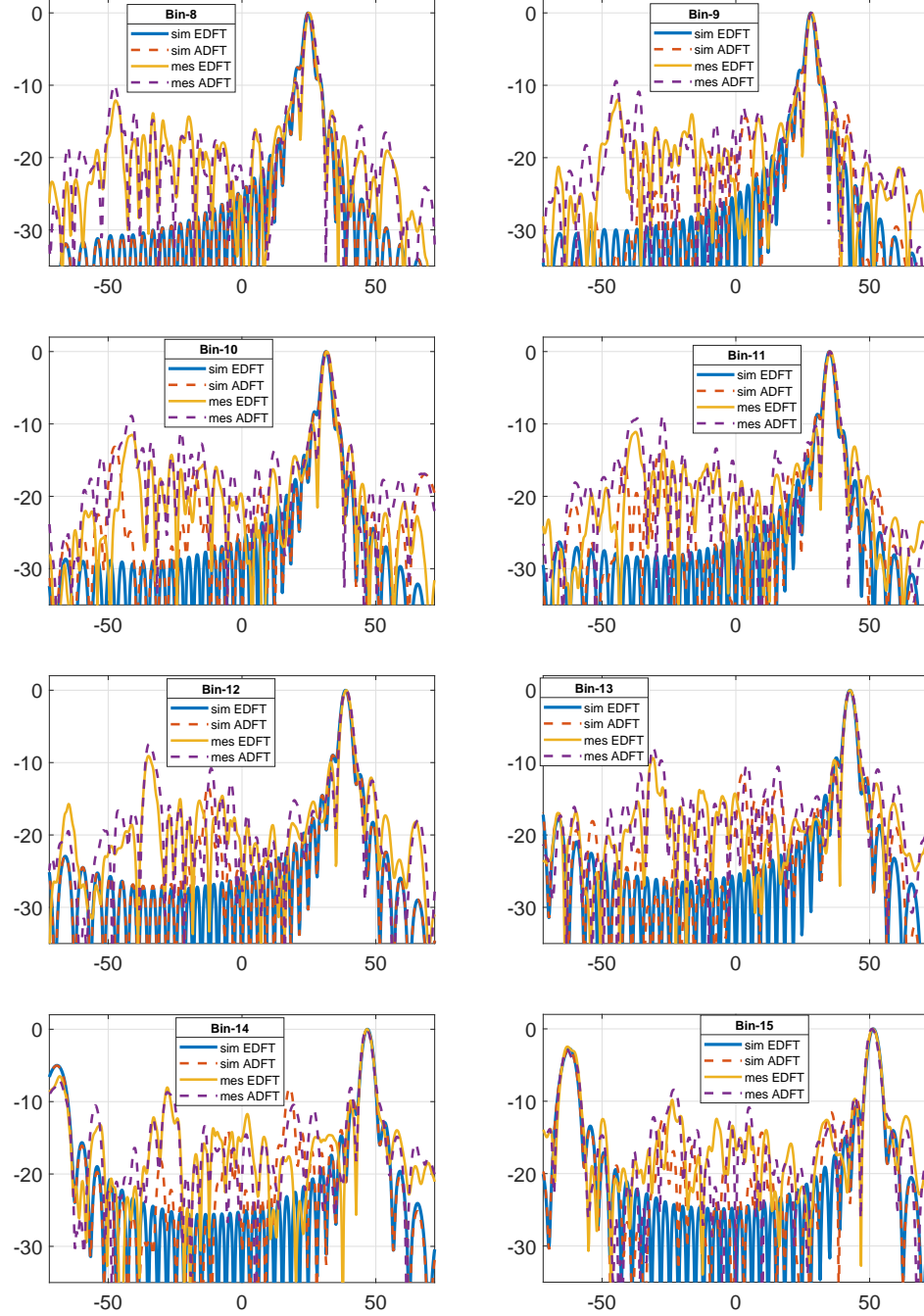


Figure 4.7: The beam outputs at bins 8-15.

realtime demo of the total system). Power patterns were measured by sending a continuous-wave (CW) signal at $f_{RF} = 5.86$ GHz. The LO signal frequency f_{LO} determines the IF $f_{RF} - f_{LO}$. The measurements were generated by setting

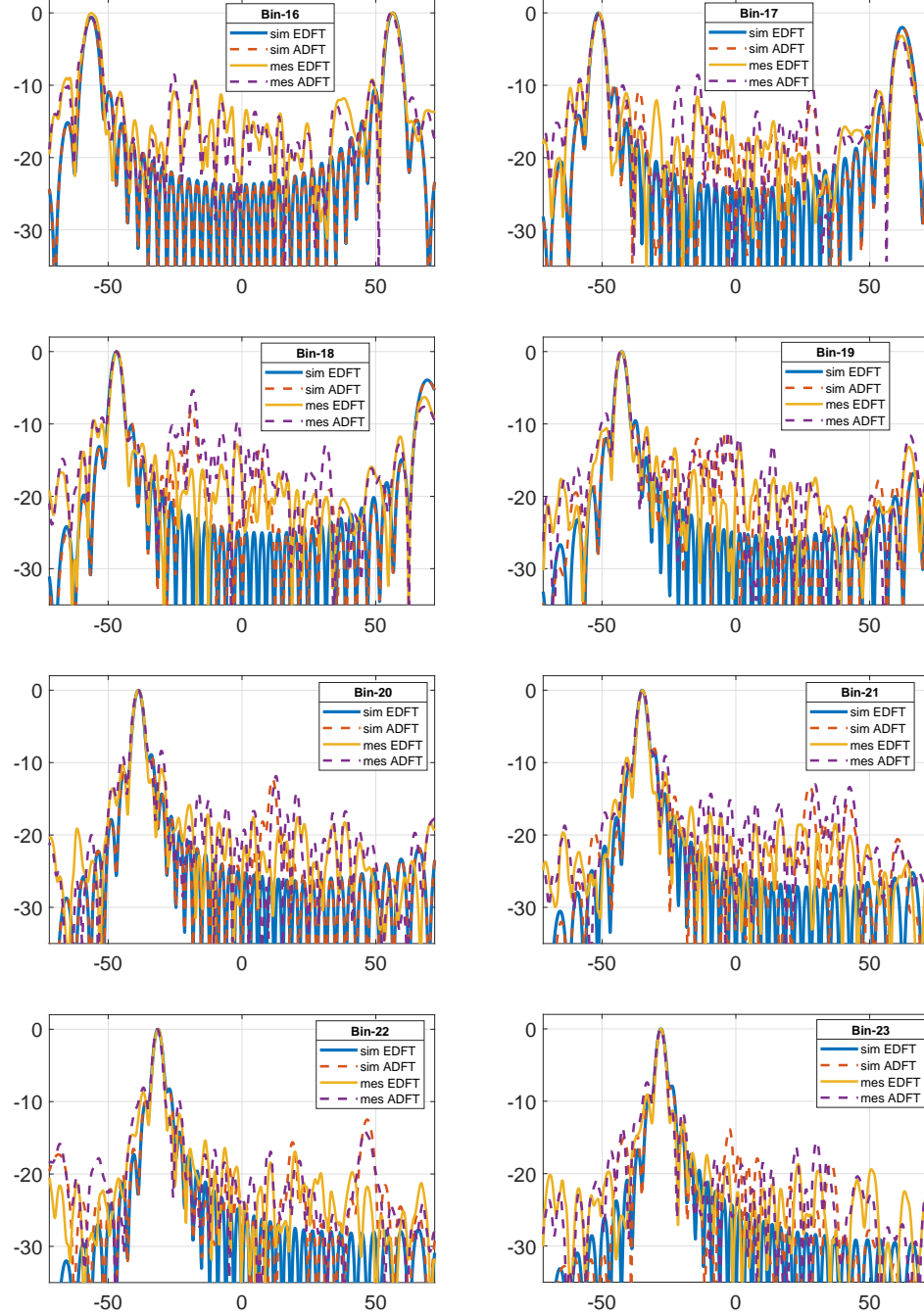


Figure 4.8: The beam outputs at bins 16-23.

$f_{LO} = 5.85$ GHz, thus resulting in an IF of 10 MHz, and digitizing the down-converted outputs at $f_{clk} = 200$ MHz. The measurement was conducted using digital integrators at each FFT/ADFT bin output to calculate the received energy

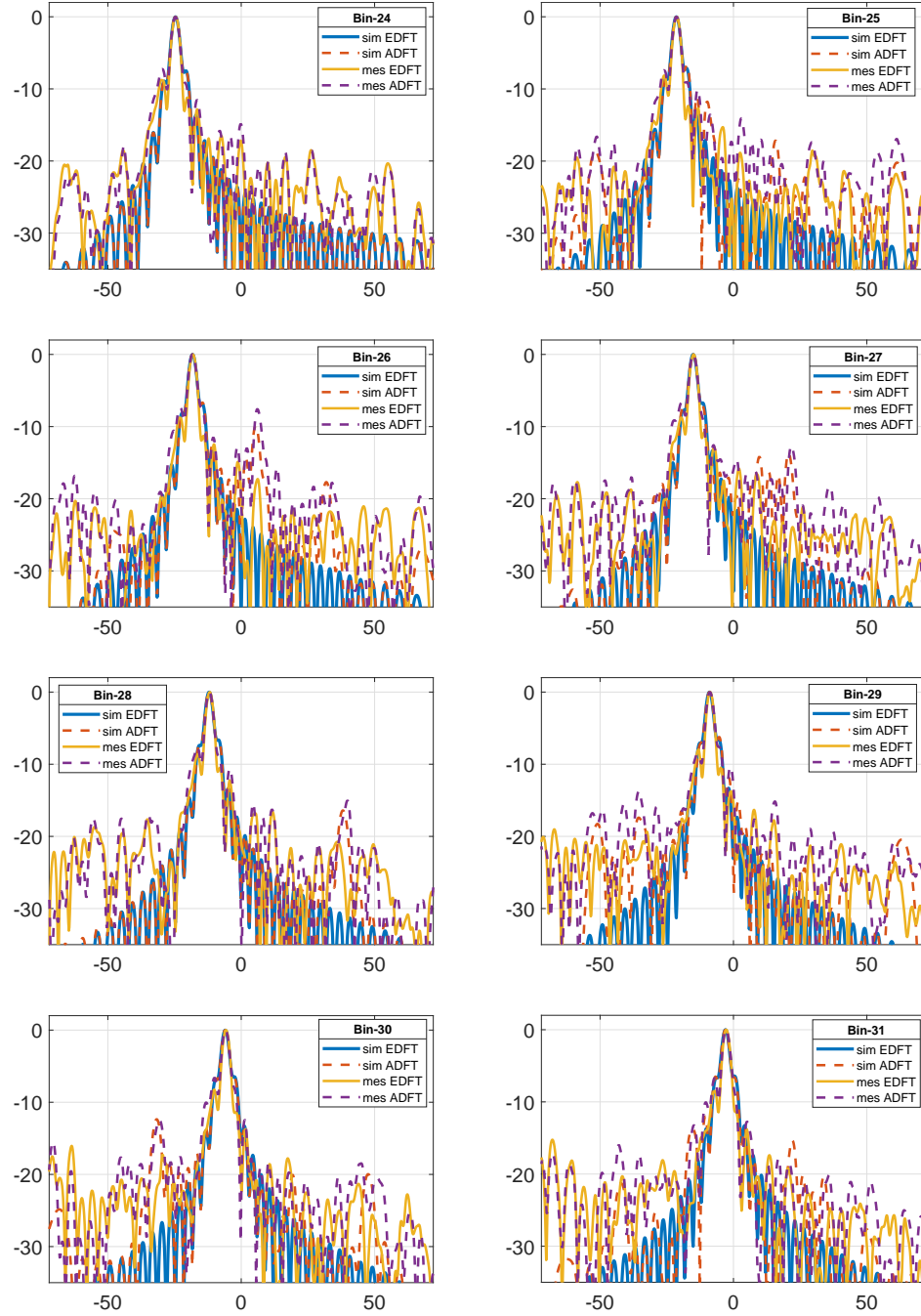


Figure 4.9: The beam outputs at bins 24-31.

for a fixed amount of time. Figs. 4.6,4.7,4.8,4.9 show the measured beams from the 5.8 GHz real-time experimental setup for both the exact fixed-point FFT and approximate algorithms along with the corresponding simulated curves. Simulated

beams accounts antenna element pattern and the actual separation of the transmitter and the receiver in the measurement setup. The vertical axis of the plots is in dB and the horizontal axis is the azimuthal angle for the range $[-72^\circ, 72^\circ]$.

The measured array factor of the beams highly depends on the measurement setup geometry. Ideally, the transmitter and the receiver should be placed far enough apart for waves incident on the receiver array to be approximated as plane waves. Numerical simulation in Fig. 4.10 shows how the actual array factor being measured deviates from this ideal depending on the geometry of the test setup. Based on the standard rules [33, p. 42], the transmitter and receiver should have a separation exceeding 20 m at 5.8 GHz in order for the receiver aperture to be in the far field. However, such a large separation was not achievable within our test facility. In particular, the beams were measured in an open parking deck with a transmitter receiver separation of approximately 7 m. Due to this reason, the measured beams shown in Figs. 4.6 to 4.9 have been compared with numerically-simulated beams that account for both finite transmitter-receiver separation and the actual element pattern.

Beam plots in Figs. 4.6,4.7,4.8,4.9 show that the measured beam patterns for both the algorithms closely follow each other for all the bins. The measured beams also follow the expected patterns quite well in the vicinity of the main beam. For both algorithms, the measured plots have higher side-lobe levels in the deeper stop bands compared to the simulated ones. The degradation in stop band performance can be due to mutual coupling effects and post-calibration errors of the system; which are dominated by the performance of the analog front-ends in the receiver. Measurement errors, including the fact that the tests were not performed in an anechoic environment, also lead to deviations from the expected patterns.

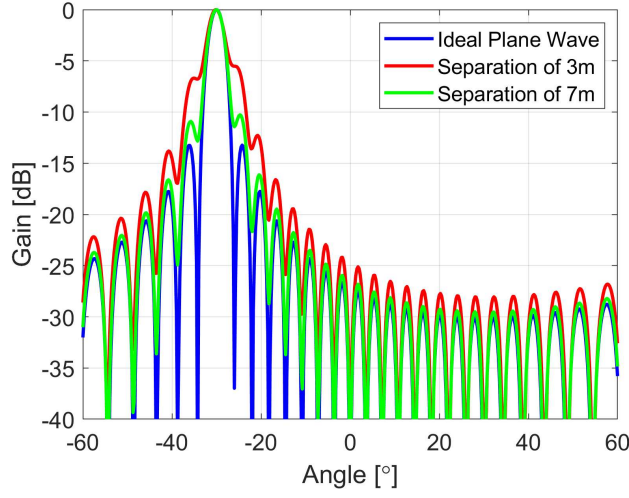


Figure 4.10: The impact of the measurement setup geometry on the measured beam response.

The 2D array factor of each beam arising from the proposed linear transform can be expressed as,

$$\Psi_{k,l}(\omega_x, \omega_y) = \sum_{n=0}^{31} \sum_{m=0}^{31} [\hat{\mathbf{F}}_{32}(k, m) \hat{\mathbf{F}}_{32}(l, n) e^{-j(\omega_x \Delta x m + \omega_y \Delta y n)}], \quad (4.6)$$

which may be rearranged to

$$\Psi_{k,l}(\omega_x, \omega_y) = \left(\sum_{m=0}^{31} \hat{\mathbf{F}}_{32}(k, m) e^{-j\omega_x \Delta x m} \right) \times \left(\sum_{n=0}^{31} \hat{\mathbf{F}}_{32}(l, n) e^{-j\omega_y \Delta y n} \right) \quad (4.7)$$

$$= \Upsilon(k, \omega_x) \times \sum_{n=0}^{31} \hat{\mathbf{F}}_{32}(l, n) e^{-j\omega_y \Delta y n}, \quad (4.8)$$

where $k, l \in [0, 1, \dots, 31]$, $\omega_x = \omega_{ct} \sin \psi \cos \phi$, $\omega_y = \omega_{ct} \sin \psi \sin \phi$, ψ and ϕ are elevation and azimuthal angles, respectively. Δx and Δy denote the inter-element spacing in x and y directions. The relationship in (4.8) can be used to compute the 2D beam responses corresponding to a 2D URA consisting of 32 linear arrays, each with the measured responses shown in Figs. 4.6 to 4.9. In particular, the term $\Upsilon(k, \omega_x)$ denotes the array factor of the k th beam in the 32-element linear array subsystem. The measured 1-D beam patterns were thus used in place of $\Upsilon(k, \omega_x)$ to

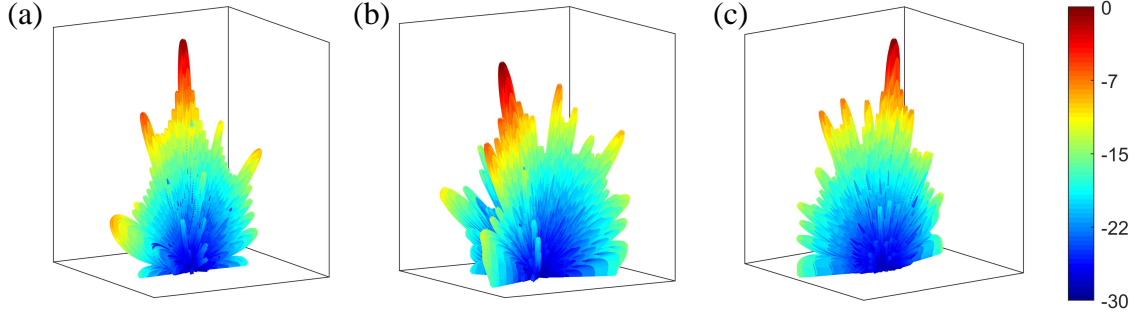


Figure 4.11: 2D beam patterns computed from 1-D array beam measurements using the ADFT algorithm. The beams correspond to the bin outputs (same angles) as the beams shown in Fig. 4.4(a-c).

synthesize the corresponding 2D beam patterns from a 2D aperture. Fig. 4.11 shows the 2D beam patterns obtained using the measured ULA beam measurements for the same beams shown in Fig. 4.4 assuming $\Delta x = \Delta y$.

4.6 Conclusion

A large number of simultaneous beams has become an essential requirement for emerging mm-wave based 5G systems. Moreover, future communications applications, such as space-based Internet services, demand an ultra-high number of beams. An $N \times N$ square antenna array aperture can generate up to N^2 orthogonal simultaneous beams by using the 2D N -point spatial DFT. The upper bound of the multiplicative complexity associated with such processing using FFT algorithms is $\mathcal{O}(2N^2 \log N)$. The work presented in this chapter presents a low-complexity digital beamforming architecture for generating 1024 simultaneous RF beams using a 32-point DFT approximation that completely eliminates multiplication operations. The proposed ADFT algorithm consumes 46% less area than the reference FFT-based design, while achieving a 50% drop in critical path delay. The VLSI metrics AT and AT^2 for the proposed algorithm are reduced by 73% and 86%, respectively.

The proposed approach has been validated on a fully-functional 32-element digital 1D receive array that operates at 5.8 GHz. This design will serve as the main subsystem for future implementations of a 32×32 2D rectangular aperture that could generate 1024 simultaneous RF beams with significantly lower SWaP in VLSI implementations. The 1-D array uses 32 parallel ADCs for sampling the antenna outputs and the ADFT (implemented on a Xilinx FPGA) for computing 32 RF beams in real-time. The measured RF beams show a per-beam bandwidth of 100 MHz when all 32 beams are realized in real time, with only marginal (< 2 dB) degradation in beam performance compared to a control experiment based on the Duhamel FFT core.

CHAPTER 5

DIGITAL BEAMFORMING AT 28 GHZ USING XILINX RFSOC PLATFORM

This chapter presents the digital beamforming work done at 28 GHz using a 4-element array receiver. The work can be viewed as an attempt to push forward the work done in chapters 3 and 4 and demonstrate fully digital beamforming in the mmW frequencies supporting the wider bandwidths. Due to the constraints of cost in mmW front-ends, the 28 GHz prototype digital beamformer has been limited to a 4-element array. The Federal Communications Commission (FCC) in the United States has allocated the 27.5-28.35 GHz [136] band for 5G mobile communication. There is a total bandwidth allocation of 850 MHz in the 28 GHz band. Therefore, the objective of the work is to perform and demonstrate fully digital beamforming across the whole bandwidth which has not been reported in the literature. Digital beamforming is performed using the Xilinx ZCU 1275 board which features the Xilinx RFSoc device that comes with RF ADCs (and DACs) integrated to the same chip along with the programmable logic and the processor subsystem. The results of the beams measured across 800 MHz bandwidth is presented.

5.1 28 GHz Receiver Array

The digital beamforming work described in this chapter uses a 4-element 28 GHz array receiver and the design procedure of the mmW front-end is described in [137]. The overall architecture of the 28 GHz array receiver setup is shown in Fig. 5.1. The receiver is designed as a direct-conversion receiver that brings the RF passband down to baseband. The specification and the design procedure of the receiver is detailed in [137]. The receiver has been designed to support 845 MHz bandwidth using orthogonal frequency division modulation (OFDM) that incorporates an FFT

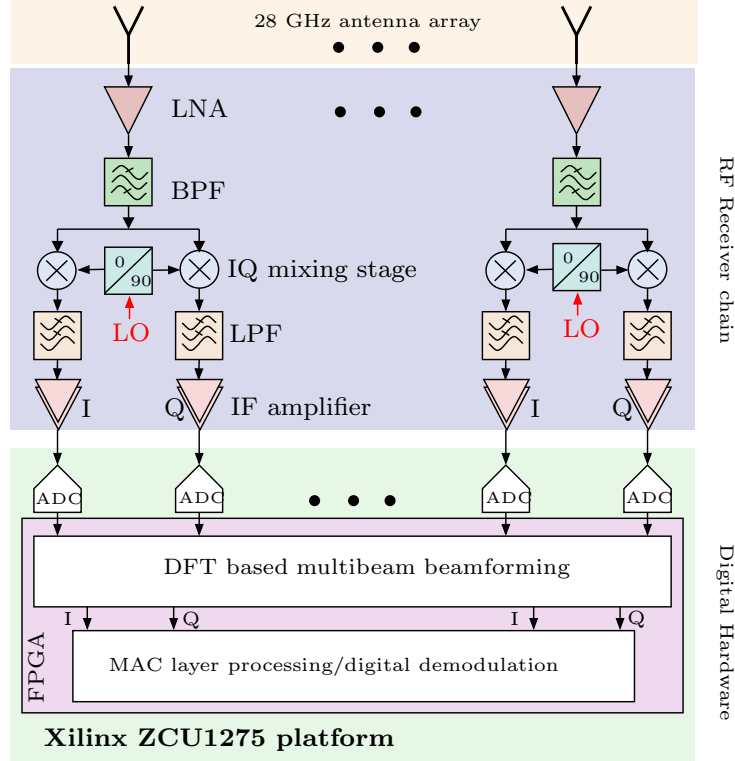


Figure 5.1: The overall architecture of the 4-element 28 GHz digital beamforming receiver.

size size of 512. Following subsections will describe each of the sub-components of the receiver array front-end.

5.1.1 Antenna Array

A 4-element ULA in receive mode where each antenna element of this array operates at a center frequency of 28 GHz, with a bandwidth of 850 MHz was used in the array receiver setup. This antenna was designed by a fellow labmate and the design details are provided in [138]. The inter-element spacing of the 4-element array that was used for the digital beamforming setup has been set to 0.75λ at 28 GHz. The antenna array is shown in Fig. 5.2. As seen in Fig. 5.2, the individual antenna has been build as an 8-element series fed sub-array. The vertical subarray provides higher gain in

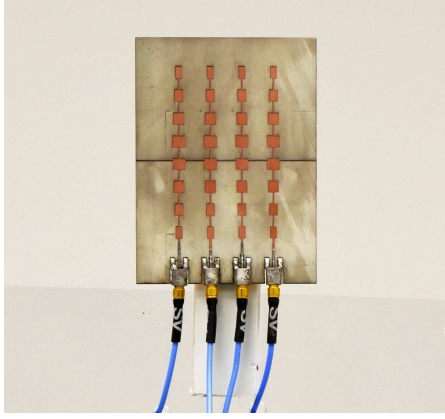


Figure 5.2: The 4-element ULA consisting of series fed sub-array patches at 28 GHz.

the elevation plane to aid the real-time beam measurements. The antenna resonates at 28.05 GHz with a return loss of -27.41 dB. The tapered 28 GHz array produced a side-lobe level lower than -18 dB in the elevation plane as compared to -13 dB down side-lobes for non-tapered rectangular structure.

5.1.2 Receivers and Front-End

The direct-conversion receiver chains were designed using COTS electronics following the specifications as described in [138]. The RF receiver chain components and their specifications are tabulated in Table 5.1. The down converter module

Table 5.1: RF receiver chain components and specifications

Component	Gain	NF	OIP3
LNA [MACOM] MAAL-01111	19	2.5	20
Down Converter [AD] HMC1065LP4E	9	3	14
LPF [MiniCircuits] LFCN-900+	-1	1	NA
IF Amp [MiniCircuits] RAM-8A+	[31.5,24]	2.6	24.4
VGA [AD] ADL5331)	[-15,15]	9	39

HMC1065LP4E incorporates a frequency doubler in it and therefore, the LO input can be driven at half the frequency of the RF band. An LO frequency of 13.95 GHz

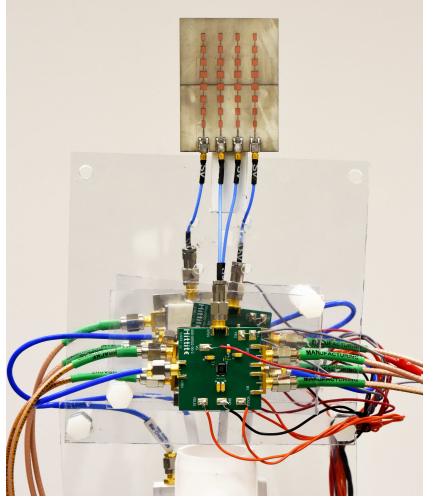


Figure 5.3: The 4-element receiver array front-end having the antenna array and the receivers.

has been used for this beamforming setup. A centralized LO distribution network is used to simultaneously and coherently drive all the channels from the array. As per the calculation shown in [138], the receiver is designed to have a cascaded gain $G_{cas,dB} = 70$ dB with an overall noise figure $F_{cas,dB} = 2.5$ dB. The receiver is capable of demodulating up to 64 quadrature amplitude modulation (QAM) at an apt power of -80 dBm at the antenna input [137]. The entire front-end incorporating the antenna array is shown in Fig. 5.3.

5.2 Digital Back-End

The digital back-end of the system is implemented using Xilinx ZCU 1275 [139] development platform which incorporates an Zynq UltraScale+ RFSoc [140]. In addition to a high-capacity FPGA fabric, the Xilinx RFSoc XCZU29DR chip in the ZCU 1275 board contains 16, 2 GSps ADCs having a resolution of 12-bits and 16, 6.4 GSps DACs of 14-bit resolution, all integrated into a single integrated circuit. The digital beamforming system uses 8 ADC channels in the RFSoc to sample

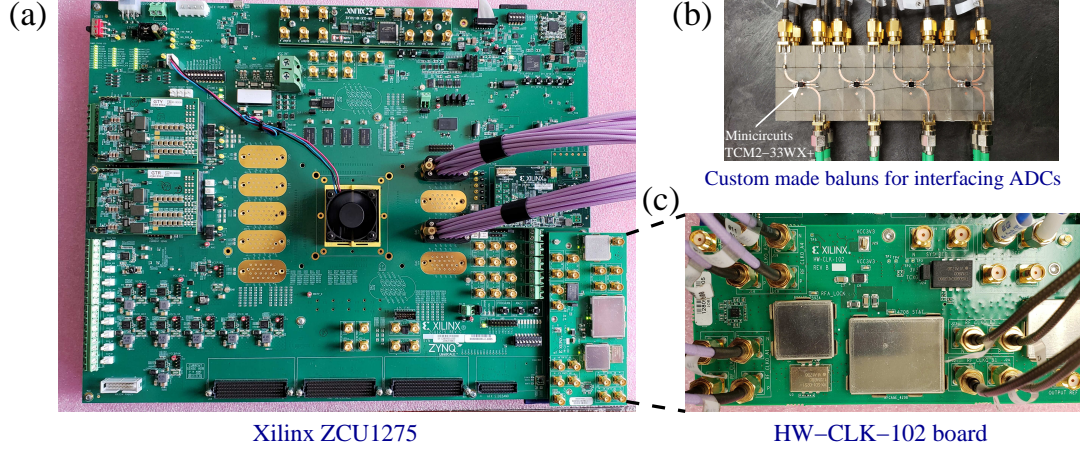


Figure 5.4: (a) Xilinx ZCU 1275 platform incorporating Zynq UltraScale+ XCZU29DR chip; (b) custom-made balun boards for interfacing the ADCs; (c) HW-CLK-102 clock generation board.

the 4 IQ IF signal pairs from the 28 GHz antenna front-end to perform digital beamforming. Fig. 5.4(a) shows a picture of the ZCU 1275 board that is used in the described beamforming setup. The following section will provide a description of the architecture of the RFSoc data-converters in general and the setting up of the board for using data-converters.

5.2.1 RF ADCs on the Xilinx RFSoc

The architecture of the Xilinx XCZU29DR RFSoc's ADCs is shown in Fig. 5.5 [3]. The 16 ADCs in the XCZU29DR are arranged in 4-tiles where each tile contains 4 data converters. Each tile can be clocked separately with either an external clock input or using the phased-locked-loop (PLL) that is inbuilt into each tile. All tiles can be synchronized using a *SYSREF* input that has been routed to all the tiles. The synchronization mechanism is detailed in [3]. The ZCU1275 comes with separate clocking boards as a solution to provide phased-locked clocking to data converters. Fig. 5.4(c) shows the HW-CLK-102 clock board that is shipped with the ZCU 1275

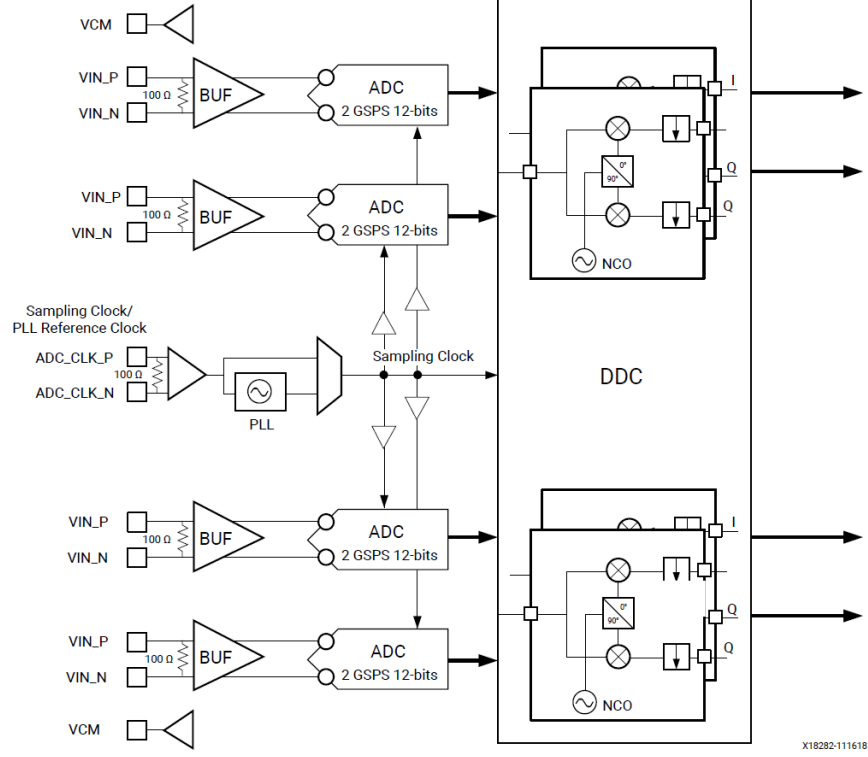


Figure 5.5: RF ADC tile overview (figure is taken from [3]).

platform. The board consists of 2 PLLs namely PLL-A and PLL-B where PLL-A is able to provide four phase aligned RF clocks in differential form for clocking the RF-ADCs and DACs in the RFSoc. PLL-B is able to generate 2 pairs of differential clocks. The particular board also supports three additional phase-aligned reference clocks for synchronization.

The data converters of the RFSoc can be configured to either AC- or DC-coupled modes. The AC-coupled mode requires differential inputs for each channel. Since the outputs from the 4-element array receiver was single-ended, a custom set of balun boards were built in-house. Fig. 5.4(b) shows a set of such baluns that were built. The balun uses the MiniCircuits TCM233WX+ transformer chip [141] with two AC-coupling capacitors at the differential output. The balun nominally works

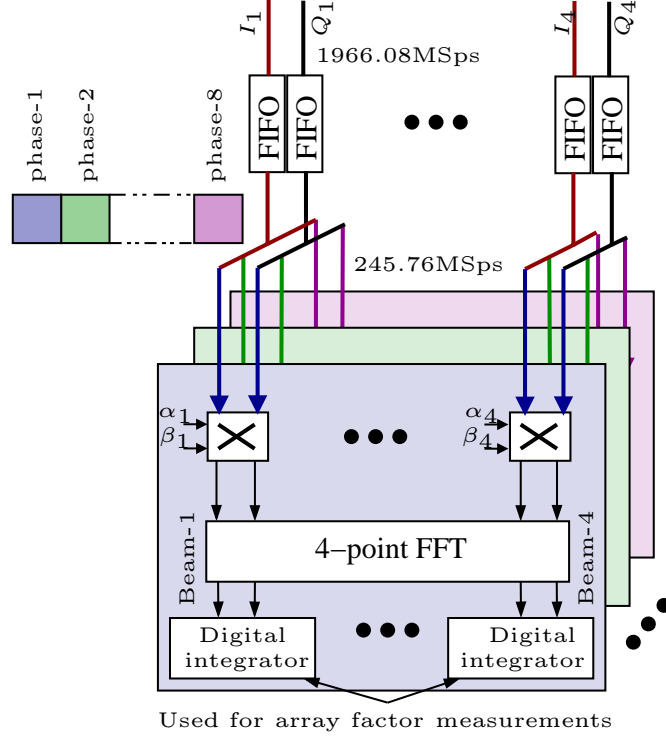


Figure 5.6: The overview architecture of the digital back-end.

in the range of 30 to 3000 MHz. For the system considered here, 8 baluns were built, tested and used for sampling all 8-IQ channels to the RFSoc.

5.2.2 Digital Beamforming

All IF inputs are connected to the data converters of the Xilinx RFSoc which are configured to sample at 1966.08 MHz. To handle the total bandwidth of 845 MHz supported by the receivers, the digital circuits were designed in a polyphase architecture that will have 8-parallel beamforming cores. Therefore, the inbuilt first-in first-out (FIFO)s of the Xilinx Data Converter IP (XDCIP) core was configured to output a sample rate of $1966.08/8 = 245.76$ MSps rate with 8 sampled words per clock edge streamed into the beamforming cores. The overview architecture of the digital back-end is shown in Fig. 5.6. The outputs of each FIFO stream were

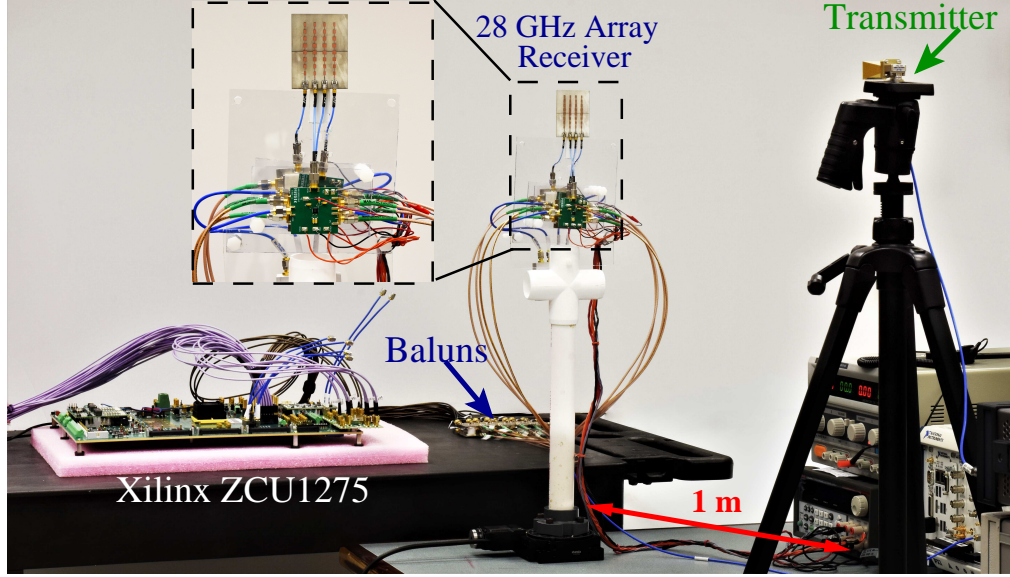


Figure 5.7: The entire measurement setup comprising the 28 GHz receiver array and the 28 GHz transmitter.

synchronized to a single reference clock of 245.76 MHz that was derived from the analog sampling clock. Four simultaneous beams were realized by using a 4-point FFT digital core across the spatial samples realizing the 4-simultaneous beams. As shown in the Fig. 5.6, the digital design uses 8 parallel such digital cores to process the entire sampled bandwidth.

5.3 Real-Time Beam Measurements Setup

The full transmitter receiver setup for real-time beam measurement is shown in Fig. 5.7. A horn-antenna is used as the transmitter to send test signals centered at 27.9 GHz f emulating different RF bandwidths. The frequency of the LO input to the receivers were set at 13.95 GHz so that after the frequency doublers, the LO signal is set at 27.9 GHz to bring down the RF center frequency to baseband zero. The beamformed outputs of each beam of each phase is then used to compute the received energy for each direction of arrival using digital integrators.

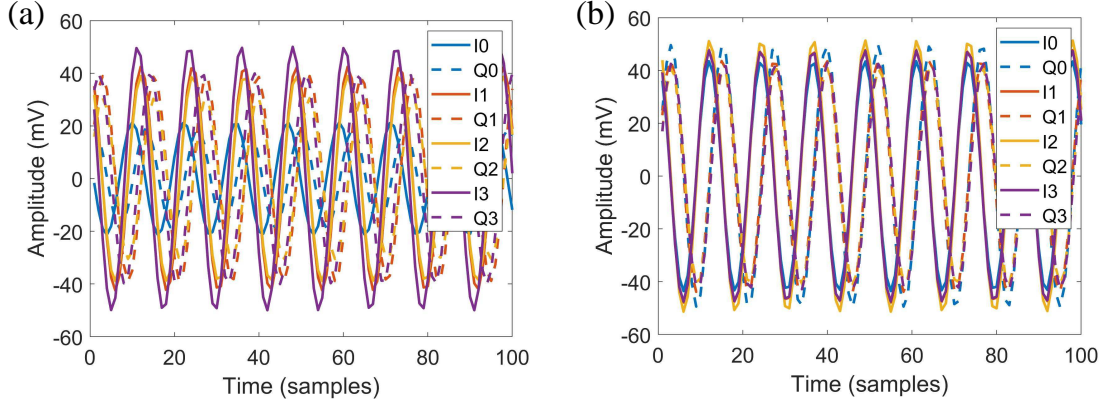


Figure 5.8: (a) The IQ outputs of the 4 downconverted channels at an IF frequency of 100 MHz.

5.3.1 Calibration

The calibration mode of each ADC channel was set to “Mode-2” [3] in the XDCIP. The ADC calibration is handled by the start-up finite-state-machine inbuilt in the XDCIP. Calibration of the RF front-ends were performed digitally by imposing gain and phase correction. The gain phase mismatches were pre-measured using a reference signal with respect to one receiver chain. This was done by employing a complex multiplier at each phase of each channel. $\alpha_i + j\beta_i$ is a constant for $i = \{0, 1, 2, 3\}$ where $\{\alpha_i, \beta_i\} \in \mathbb{R}$ represents the complex coefficient that calibrates each receiver channel. Fig. 5.8(a) shows samples recorded at each of the 8 channels from the array before calibration where $f_{LO} = 28$ GHz, $f_{RF} = 28.1$ GHz. Fig. 5.8(b) shows the samples recorded for the same configuration after calibration.

5.3.2 Real-Time Beam Measurements

The receive-mode beams generated from the digital beamforming was measured in a similar procedure as described in Chapter 3. The angle of arrival of the 28 GHz wave front was changed by rotating the receiver array to obtain the array

factors of each beam. Array factor measurements were conducted at different mmW frequencies around 27.9 GHz to demonstrate beamforming in the full 800 MHz bandwidth supported by the receiver. The beam patterns were measured changing the $f_{RF} = 28$ GHz the values in the frequency ranging from 27.5 GHz to 28.3 GHz, across a 800 MHz bandwidth at steps of 100 MHz.

The simulated (solid) and measured (dashed) set of beams measured at $f_{RF} = 28$ GHz is shown in Fig. 5.9. The simulated beams shown here have been generated by taking the element pattern into effect. Fig. 5.9(a-d) corresponds to Bins 1-4 of the spatial FFT digital core and each bin correspond to different look-directions. The look directions are set by the antenna spacing and can be calculated using (3.2). Since the 28 GHz array is spaced at 0.75λ , the Bin 1 points to the boresight where as Bin-2 and Bin-4 points to $\pm 19.5^\circ$ respectively. Since the antenna elements are not critically spaced, grating lobes occur beam directions beyond $\pm 41.8^\circ$ in this array. The beam output from Bin 3 points $\pm 41.8^\circ$ and thus the plots in Fig. 5.9(d) indicates two main lobes. Fig. 5.9(e,f) show all simulated beams and all the measured beams ($f_{RF} = 28$) in a single plot, respectively. From Fig. 5.9 it is evident that the measured beams agree quite well with the simulated beam patterns at the emulated IF frequency of 100 MHz.

Fig. 5.10 shows the measured patterns for output bin for different f_{RF} frequencies across the bandwidth [27.5, 27.3] GHz. The plots confirm that the main beam direction remain constant across the bandwidth. The sidelobe levels changes across the bandwidth of interest and the measurement indicates that the sidelobe levels are elevated towards the band edges. This is a consequence of the calibration being not wideband. The maximum sidelobe level recorded for Bins 1, 2, 4 across the whole bandwidth is ≈ 9 dB.

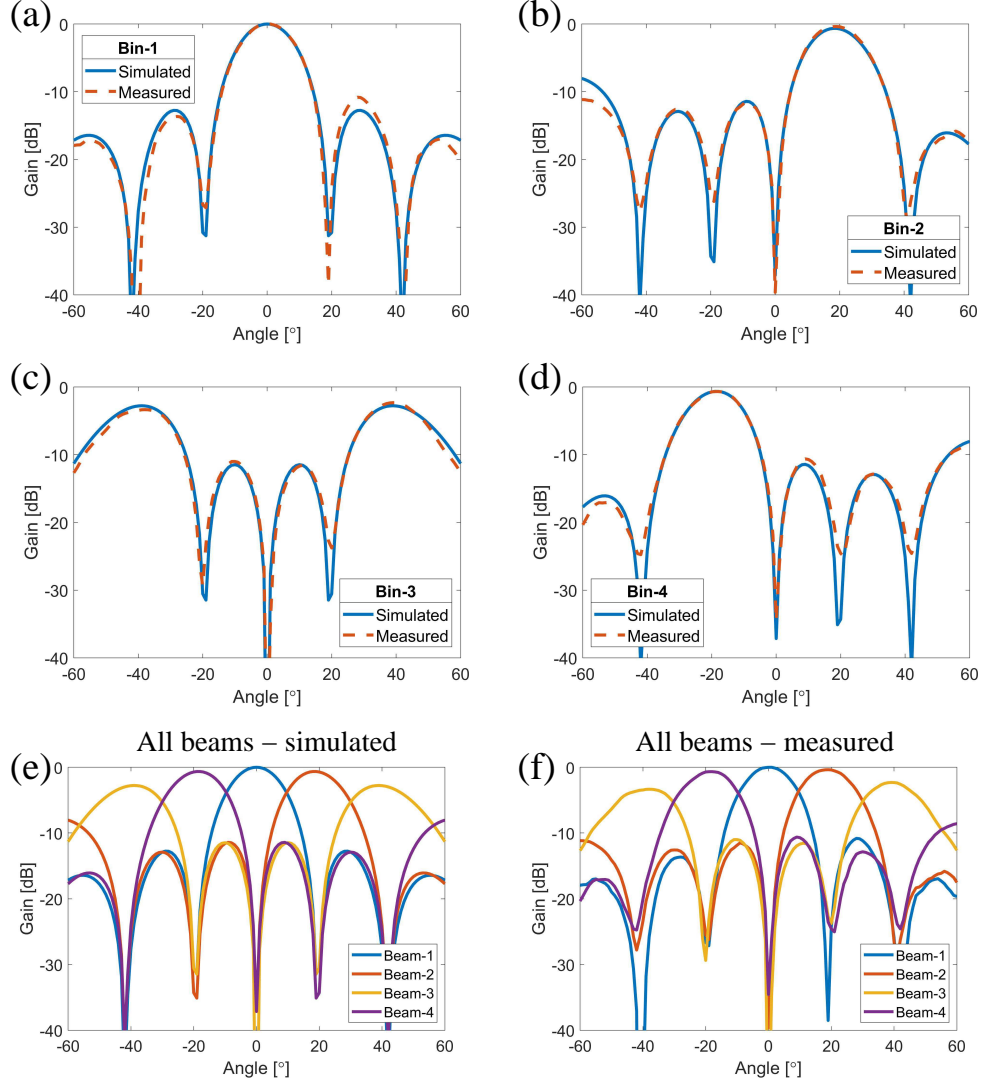


Figure 5.9: (a-d) Simulated and measured beam corresponding to each output of the FFT at $f_{IF} = 100$ MHz. (e) All simulated beams in a single plot. (f) All the measured beams in a single plot.

5.4 Conclusion

A 4-element digital beamforming array receiver at 28 GHz has been design and built using Xilinx RFSoc based ZCU1275 platform as the digital back-end. The use of the Xilinx RFSoc platform provides the luxury of processing the entire bandwidth of the 28 GHz band FCC allocation by using the on chip data converters that can

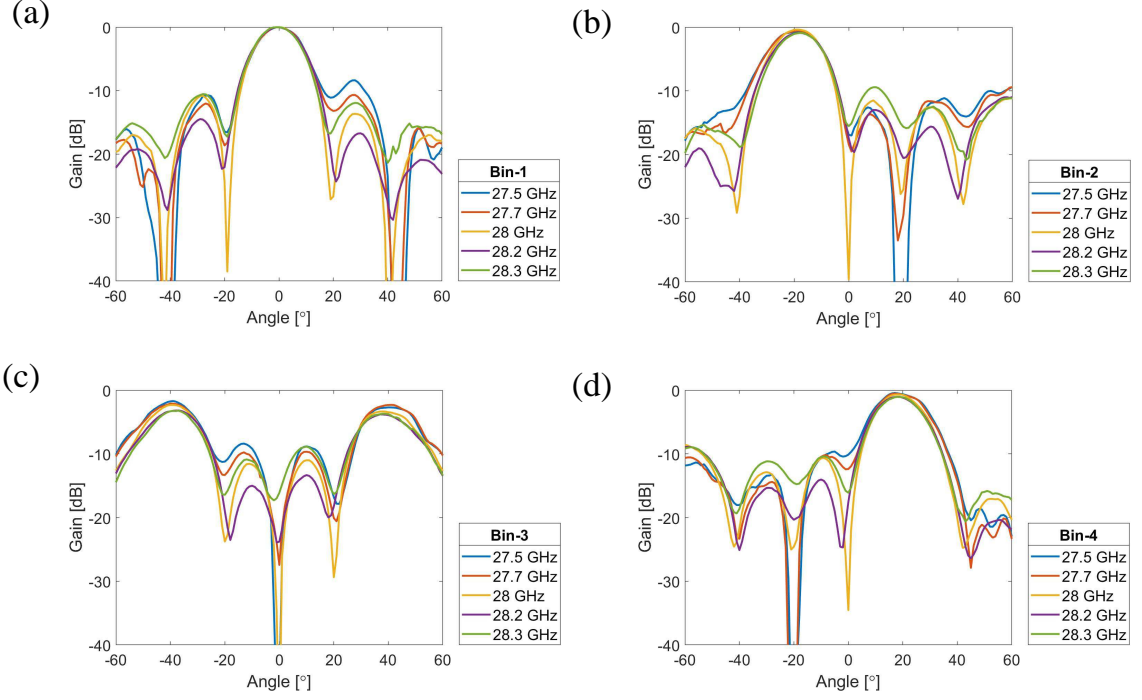


Figure 5.10: (a-d) Measured beams corresponding to the outputs of the FFT bins at $f_{RF} \in \{27.5, 27.7, 28, 28.2, 28.3\}$ GHz.

support huge bandwidths. Two ADC tiles in the RFSoc have been used to sample all 8 IQ channels in to digital to perform a 4-point spatial-FFT based multibeam beamforming to produce 4 simultaneous mmW beams. Digital polyphase beamforming architectures have been used to generate the beams in digital across the full baseband bandwidth. Array factors of the digitally formed multibeam have been measured in real-time and have been presented. They are in good agreement with the simulated beams.

CHAPTER 6

ANALOG 16-BEAM BEAMFORMING ARCHITECTURE AND THE CMOS CIRCUITS USING APPROXIMATE DFT

This chapter explores a baseband multibeam beamforming method based on the spatial Fourier transform. Approximate computing techniques that have been introduced in chapters 3, 4 are used to propose a low-complexity, low-power, high bandwidth beamforming architecture by exploiting the sparse factorizations of the ADFT algorithms that were proposed for multibeam beamforming in chapters 3 and 4. The sparse factorization stages having small integer coefficients can be neatly mapped to integer W/L ratios in CMOS current mirrors. The approximate fast Fourier transform can thus be efficiently realized using CMOS analog integrated circuits to generate multiple, parallel mmW beams in both transmit and receive modes. The work in this chapter uses the 16-point approximate-FFT algorithm given in Chapter 3 to design a novel analog multibeam network using 65 nm CMOS models. The proposed multi-beam architectures have the potential to reduce circuit area and power requirements while exceeding the baseband bandwidth requirements of emerging 5G commercial systems.

6.1 Introduction and Review of RF System Considerations

As described in Chapter 1 multibeam systems are essential and are envisioned for 5G wireless network base stations, mobile stations, micro base stations, pico cells, and user equipment. For mobile 5G systems, compact and energy-efficient integrated multi-beam solutions are highly desirable to improve battery life and reduce heat-dissipation problems while enabling directional agility. The wide bandwidths of 5G systems have created new challenges in realizing fully-integrated transceivers and

have made some currently-favored transceiver architectures, such as passive mixer-based receivers, not directly applicable [142].

As an example of such a solution, a recent work by IBM [4] demonstrates fully integrated dual-polarization 16-element arrays for 28-GHz 5G applications. The transceiver architecture presented in [4] is a 2-step sliding-IF half-duplex architecture as shown in Fig. 6.1. A transceiver topology that is similar to in [4] is very

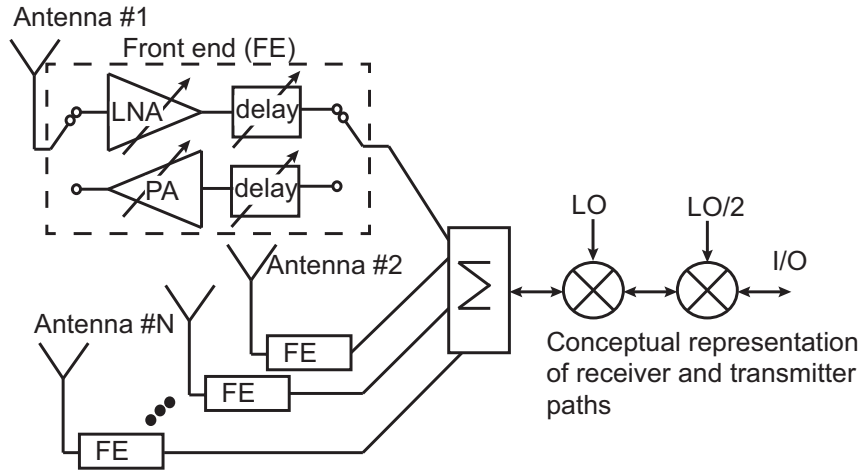


Figure 6.1: A representative 28-GHz 5G half-duplex transceiver architecture based on delay-and-sum beamforming [4].

representative, and it is anticipated that this type of architecture will likely remain favorite for 28 GHz 5G systems for a few years to come until 5G systems are widely adopted and more advanced transceiver topologies are developed. Unlike steerable beamformers using tunable delays at mmW bands, the proposed multi-beam architecture in this chapter operates in the baseband while supporting up to 1.5 GHz of bandwidth per beam. Similar to the digital approach present in Chapter 3, the proposed method utilizes the spatial frequency distribution of directed mmW energy where each mmW beam has a unique spatial frequency that remains intact through up-down conversion in the mixers. Thus, the proposed baseband analog-FFT can

realize multiple far-field mmW beams for variety of transceiver architectures without requiring tunable mmW delay lines.

6.2 Spatial FFT-based Multi-Beam Architectures

In Chapter 3, the use of DFT operation digitally across an ULA samples for obtaining multiple simultaneous beams was discussed. Also, the Chapter 3 showed that any type of FFT implementation has computational error due to the use of finite precision arithmetic to realize irrational DFT matrix coefficients. Therefore, it was proposed that approximated DFTs can be used for applications like generating multibeam as the beamforming is an application that can tolerate accuracy errors. Having this said, computations in the analog domain are known to handle much higher bandwidths than the digital implementations at much lower power consumptions. Therefore, in this chapter, the use of ADFTs that were proposed to achieve low-complexity digital multibeam are investigated to produce analog multibeam owing to the small integer coefficients in them.

In particular, transforms with small integer coefficients are desirable because they enable straightforward current-mode implementations by changing the W/L (width/length) ratios of CMOS transistors to implement multiplication by the particular coefficient. Such current-mode implementations are intrinsically fast because their bandwidth is only limited by the poles of the current mirrors and not by the maximum clock rate as for digital counterparts [143].

In current-mode, current-mirror-based IC implementations of the approximate algorithms would need only 2-4 well-matched transistors for realizing each coefficient. The area and power consumption of both these signal processing approaches (digital and analog) scale with accuracy requirements [144]. Fig. 6.2 shows system

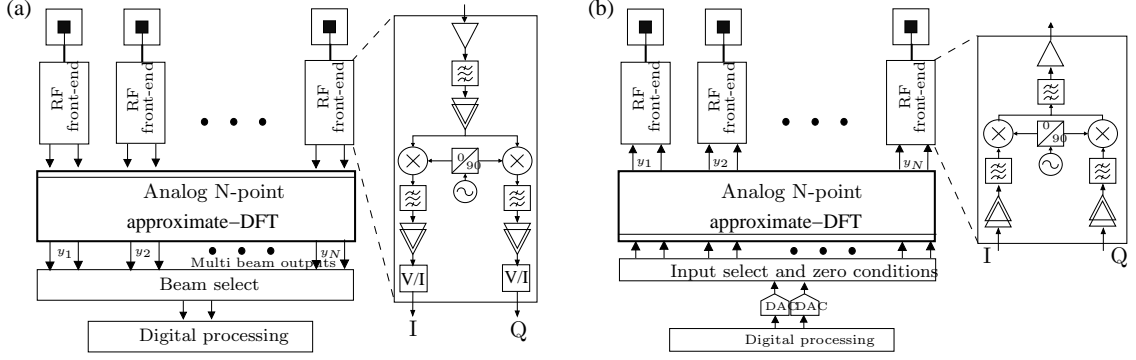


Figure 6.2: (a) Receive-mode multi-beam system with down-converted analog base-band beamforming; (b) transmit-mode multi-beam system using baseband analog beamforming.

configurations for both transmit and receive modes that can produce N simultaneous beams by using the proposed analog N -point approximate-DFT (ADFT), where $N \in \{8, 16, 32\}$. This chapter specifically focuses on the 16-point ADFT in (3.9) and its factorization algorithm in (3.14) to explore CMOS circuits in order to generate 16 high bandwidth analog beams. The discussed methodology can be adopted for other sizes of N , given similar small integer coefficient transforms that approximates the respective N -point transform that found through a similar approach in (3.14). The method in (3.8) can also be applied for larger matrix sizes such as $N = 1024, 2048, \dots$. The resulting approximation matrices will then possess better properties such as near-orthogonality and spectral behavior that is close to the exact DFT. The main problem in deriving such larger approximate DFT matrices is the necessity of creating associated fast algorithms: the larger the matrix, the harder it becomes to derive such algorithms. A possible alternative for generating such large approximations is the use of scaling methods. Essentially, larger ADFTs can be generated by *re-using* smaller ADFTs. This avoids the hassle of deriving fast algorithms for large matrices, and the CMOS circuit architecture

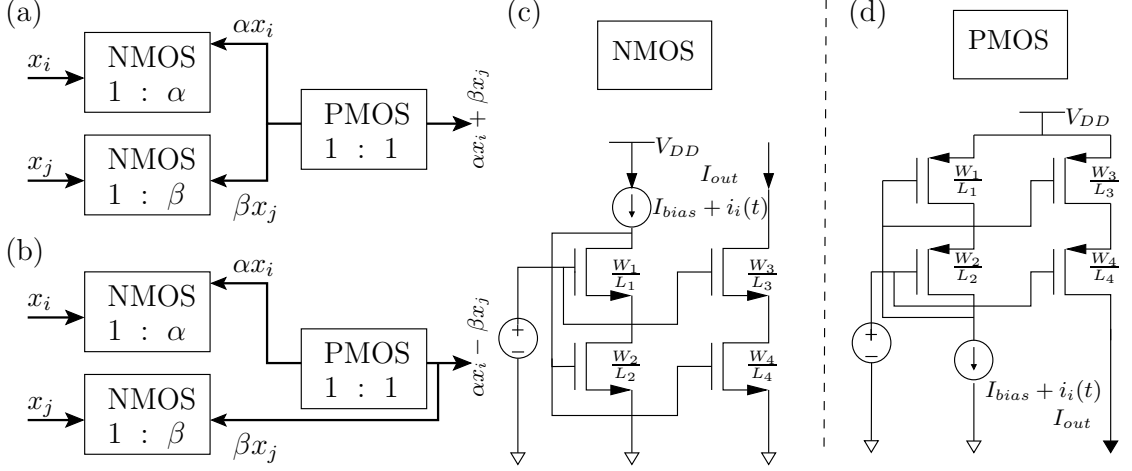


Figure 6.3: Current-mode implementation of (a) addition and (b) subtraction operations, which are the primary functions for implementing the ADFT using analog CMOS circuits; (c) NMOS and (d) PMOS current mirrors designed using a low-voltage cascode topology.

proposed in this chapter can be used as the building block that generates the higher order beams in a larger array.

6.3 Circuit Topologies, Beamforming Architectures

Realization of the analog-DFT is key to implementing the mmW receiver and transmitter architectures shown in Fig. 6.2. Early attempts to implement analog DFT processors used op-amp circuits to realize the weights of the DFT matrix [145]. This approach is slow and difficult to scale to larger arrays because the twiddle factors become closer to each other as the FFT size increases, making them harder to realize accurately. More recently, a $0.13 \mu\text{m}$ CMOS 8-point Cooley-Tuckey FFT processor for orthogonal frequency division multiplexing (OFDM) applications was reported [146,147]. The processor uses a time-interleaving bank of sample-and-holds and discrete time analog multipliers, and has been tested with 1 GS/s OFDM inputs. However, dedicated input signals are used to represent the FFT coefficients, which

makes scaling difficult. 2-D rectangular LC lattices implemented on CMOS have also been proposed for computing analog DFTs of spatial input signals [148]. The method has been verified using numerical simulations, and bandwidths of > 10 GHz are possible for on-chip implementations. However, such large bandwidths require small inductor and capacitor values, which are difficult to realize accurately, and unwanted mutual coupling between the inductors is also an issue. The analog FFT processor in [149] uses a current-mirror-based architecture to scale the input current by the twiddle factor weights. However, the authors had to approximate the weights to the first decimal place for ease of implementation, resulting in degraded beam shapes. Finally, the work in [150] describes a 16-point analog domain FFT using a charge-reuse analog Fourier transform (CRAFT) engine. The circuit uses charge reuse to achieve an input bandwidth of 5 GHz. However, the design requires RF samplers in the front-end, and inaccuracies in the capacitance network lead to twiddle factor errors that make scaling difficult.

A critical issue faced by all previous approaches for realizing analog DFTs has been that accurate twiddle factor values are difficult to generate on-chip. The level of difficulty grows as the FFT size increases since the factors become closer to each other, which results in performance degradation. Hence it makes sense to allow some error margin and implement approximate transforms with integer twiddle factors. The resulting implementations are more scalable since the transform coefficients are now constrained to a small set of Gaussian integers. The approximate transforms in (3.6) and (3.9) satisfy this special property, i.e., are limited to small integer coefficients $\mathcal{P} \in \{0, \pm 1, \pm 2\}$. This property enables high-bandwidth current-mode analog ICs in which well-controlled geometric parameters (namely, the W/L ratios of current mirror transistors) determine the integer coefficients.

6.3.1 Analog Current-Mode ADFT Designs

Let the current-mode signals captured by the N Nyquist-spaced antennas of an N -beam multi-beamforming system be $x_{\text{in}} = [x_1, x_2, \dots, x_N]^T$. The beam outputs $y = \hat{F}_N \cdot x_{\text{in}}$ where $y = [y_1, y_2, \dots, y_N]^T$ correspond to unique directions of arrival given by $\psi_i = \sin^{-1}(\frac{2k}{N})$ where $k = \begin{cases} i; & 1 \leq i \leq N/2 \\ -i; & N/2 < i \leq N \end{cases}$ and i is the output bin number. In current mode, the output current at each output bin y_i requires implementation of $\sum_{k=0}^{N-1} p_{ik}x_k$ where p_{ik} denotes a matrix coefficient. The addition and subtraction arithmetic required for this calculation can be implemented directly using NMOS and PMOS current mirrors as shown in Fig. 6.3(a). Here α and β are the weights by which the input current needs to be scaled. Thus the transforms in (3.9) can be realized using analog current-mode CMOS. The $Re\{\hat{F}_{16}\}$ and $Im\{\hat{F}_{16}\}$ transforms can be implemented separately to realize the full transformation.

In [151], an 8-point current-mode design that follows this approach has been discussed. Such an approach would in general require $\mathcal{O}(N^2)$ current mirrors for generating N -beams. A digital architecture which implements a fast algorithm (e.g. Fourier, discrete sine/cosine) involves the implementation of butterfly matrices. Use of such sparse factorization matrices reduces the hardware complexity of the transform. Given that a sparse factorization exists for the transform of interest, the same principle can be applied to analog implementations. Therefore, the work in this chapter targets on benefiting from the sparse factorization that reduces the arithmetic complexity of the approximate transforms given in (3.14). It is realized by implementing each factorization stage individually as a series structure.

After observing the factorization matrices of (3.7) and (3.14), it can be seen that each row and column of the factorized matrix consists of a maximum of two elements. This implies that i) each output of the factorization stage requires an

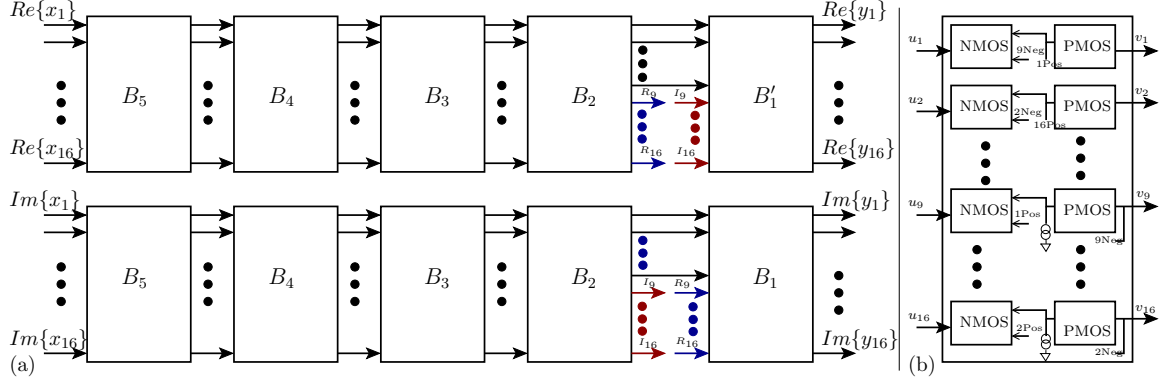


Figure 6.4: (a) System architecture of the 16-point analog ADFT; (b) realization of the B_5 factorization stage using current mirrors.

addition of the form $pa_i + qa_j$ where $p, q \in \mathcal{P}$ and a_i and a_j are $i^{\text{th}}, j^{\text{th}}$ $0 < i, j \leq N$ inputs to the factorized matrix; and ii) each input a_i has to be copied a maximum of two times. Thus an implementation of each stage of the factorization given in (3.7) and (3.14) would comprise of N NMOS current copiers producing two current copies and N PMOS mirrors attached to the outputs of each stage. The full realization of the analog circuit would require implementation of all the factorization stages and separate copies of the hardware for the real and imaginary parts as shown in Fig. 6.4. The analog implementation of the last factorization stage B_1 in the real signal path would require small changes in the circuit compared to the implementation (denoted by B_1) used in the imaginary signal path. Therefore it is denoted as B'_1 . In the design of the B'_1 block, the polarity of the signals entering from inputs 10-16 have been negated to account for the -1 generated by multiplication of the outputs 10-16 of the imaginary component at the B_2 stage by j .

6.3.2 16-point ADFT Implementation in 65 nm CMOS

The reduced hardware complexity of the factorized version makes it attractive for higher values of N . Specifically, the number of current copies needed for realizing

Table 6.1: W/L values of the NMOS transistors used to realize the NMOS current mirrors at each factorized stage in the 16-point ADFT circuit.

NMOS	B_5	B_4	B_3	B_2	B_1
W_1	$0.8 \mu\text{m}$	$0.8 \mu\text{m}$	$1.8 \mu\text{m}$	$1.2 \mu\text{m}$	$1.2 \mu\text{m}$
L_1	$0.15 \mu\text{m}$	$0.15 \mu\text{m}$	$0.15 \mu\text{m}$	$0.06 \mu\text{m}$	$0.06 \mu\text{m}$
W_2	$0.6 \mu\text{m}$	$0.6 \mu\text{m}$	$1.4 \mu\text{m}$	$1.2 \mu\text{m}$	$1.2 \mu\text{m}$
L_2	$0.09 \mu\text{m}$	$0.09 \mu\text{m}$	$0.06 \mu\text{m}$	$0.06 \mu\text{m}$	$0.06 \mu\text{m}$

Table 6.2: W/L values of the PMOS transistors used to realize the PMOS current mirrors at each factorized stage in the 16-point ADFT circuit.

PMOS	B_5	B_4	B_3	B_2	B_1
W_1	$3.7 \mu\text{m}$	$3.7 \mu\text{m}$	$3.7 \mu\text{m}$	$3.7 \mu\text{m}$	$3.7 \mu\text{m}$
L_1	$0.24 \mu\text{m}$	$0.24 \mu\text{m}$	$0.12 \mu\text{m}$	$0.12 \mu\text{m}$	$0.12 \mu\text{m}$
W_2	$4 \mu\text{m}$	$4 \mu\text{m}$	$4 \mu\text{m}$	$4 \mu\text{m}$	$4 \mu\text{m}$
L_2	$0.24 \mu\text{m}$	$0.24 \mu\text{m}$	$0.12 \mu\text{m}$	$0.12 \mu\text{m}$	$0.12 \mu\text{m}$

an N -point ADFT transform in non-factorized form has a maximum value of $4N^2$ (asymptotically $\mathcal{O}(N^2)$), whereas it is $4S_N N$ in the factorized form where S_N is the number of factorization stages (realized using NMOS mirrors). Since $S_N \ll N$, the latter number asymptotically converges to $\mathcal{O}(N)$. The factorized circuit also needs $\mathcal{O}(N)$ PMOS mirrors for performing current addition/subtraction, so the total number of mirrors required remains $\mathcal{O}(N)$ as compared to $\mathcal{O}(N^2)$ for the direct approach. For example, 308 current copies are needed for implementing the factorized version of the 16-point ADFT in current mode, whereas a direct realization would require 768 copies. Although the number of PMOS mirrors required for current addition/subtraction of currents is higher for the factorized implementation (160 versus 96), the overall complexity associated with the factorized implementation is still significantly lower. Moreover, this performance benefit becomes larger as N increases. Thus the individual factorization stages given by B_1 to B_5 in (3.14) were implemented using 65 nm CMOS. The real and imaginary components of the designs were implemented separately and the top-level architecture is shown in Fig.

6.4. The inputs to the design were assumed to be $5\text{ }\mu\text{A}$ peak-to-peak RF signals superimposed on a $100\text{ }\mu\text{A}$ DC bias current. The factorized stages were designed and cascaded starting from B_5 to B_1 to generate the 16-point transformation as shown in Fig. 6.4. The diagonal matrix D is implemented as a cross-connection of wires. All NMOS and PMOS mirrors used are low-voltage cascode current mirrors. The output bias currents of the stages were equalized by using PMOS mirrors with appropriate bias currents. The transistor sizes (named as shown in Fig. 6.3 (c) and (d)) used for the basic NMOS and PMOS mirrors in each individual stage are shown in Tables 6.1 and 6.2. The transistor sizes of the output branch were set depending on the magnitude of the matrix coefficient that was realized.

6.3.3 Simulated Beams

The circuit was simulated in Cadence Spectre using noiseless input signals generated by MATLAB. For a given direction of arrival (DOA) ψ , 16 spatially Nyquist-sampled sinusoidal signals (which emulate downconverted plane waves) were generated. The simulation frequencies of the signals were chosen to be within the baseband bandwidth of interest, which is smaller than the bandwidth of the circuit being simulated [12]. These inputs were fed to the circuit and the simulated output waveforms were recorded. To obtain the array factor for each bin of the ADFT, waveforms were generated for different values of ψ in the range -90° to 90° . The output waveforms were then exported to MATLAB in order to compute the beamformed signals as a function of ψ . Fig. 6.5 shows the power patterns of each beam at different frequencies.

In general, the beam shapes obtained from Cadence simulations closely follow theoretical ADFT responses. The side lobe levels of the beam patterns at 500 MHz

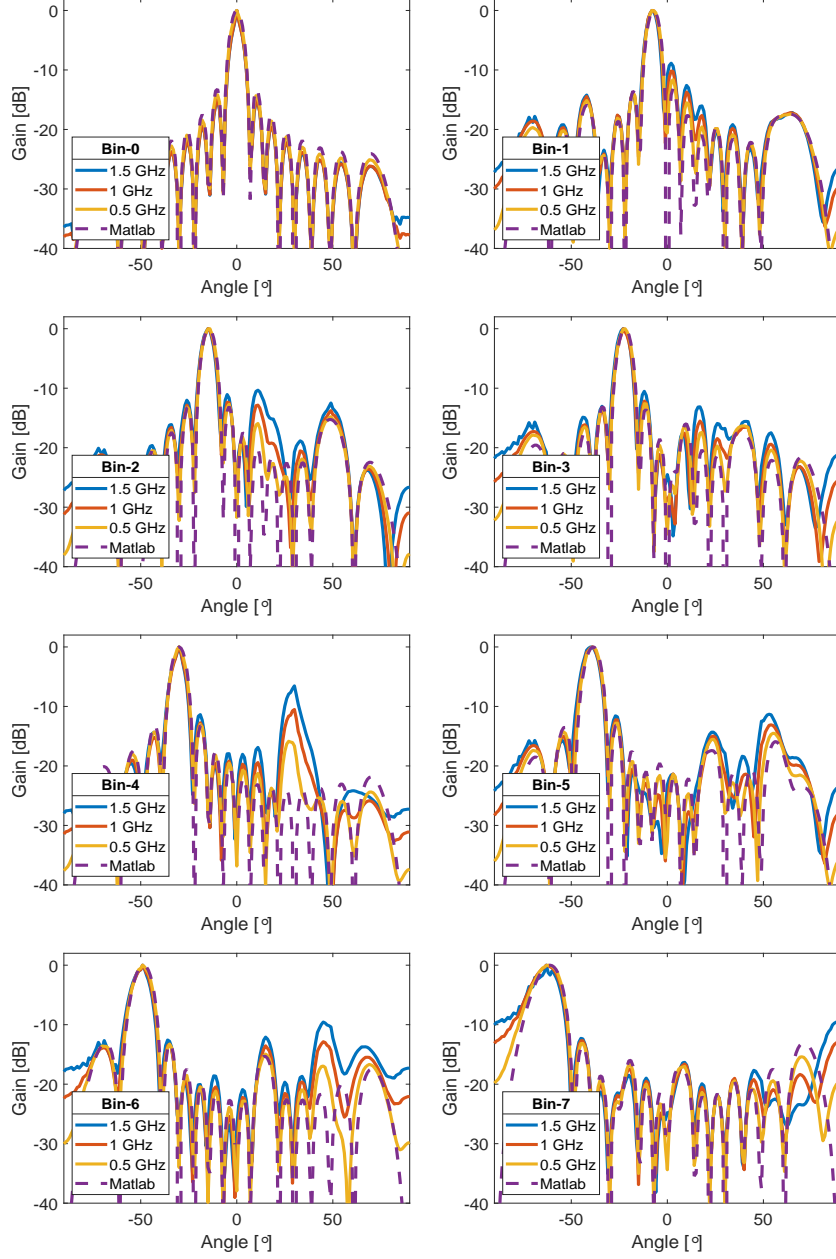


Figure 6.5: Beam outputs generated from Cadence Spectre simulations for output bins 0-7 of the 16-point analog ADFT design. Each sub-figure shows beam patterns for different IF bandwidths from Cadence and the simulated from MATLAB. .

remain consistent with theoretical responses except for bins 5, 7, 11, and 13, which have significantly higher side-lobe levels in the stop band than expected. This effect arises due to slight deviations between the theoretical coefficients and those

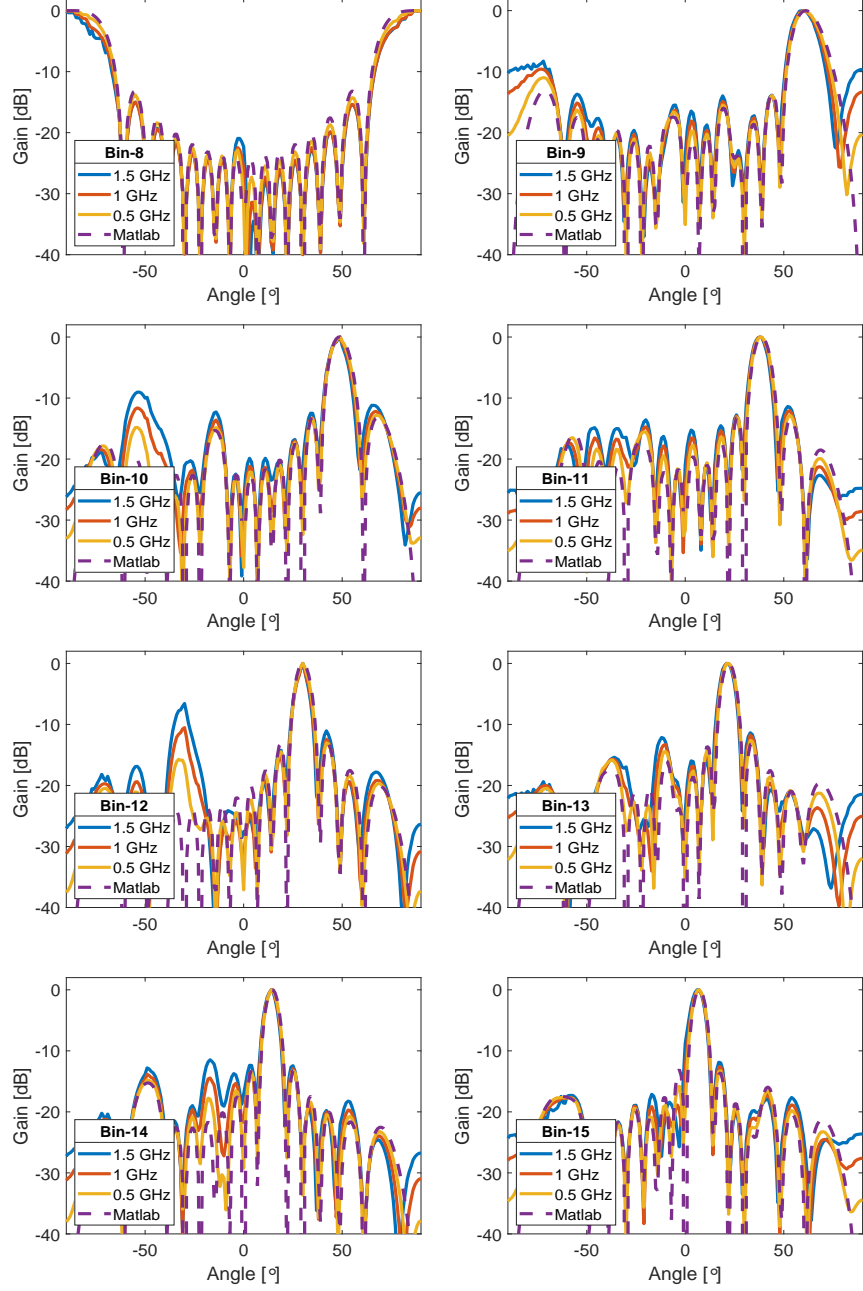


Figure 6.6: Beam outputs generated from Cadence Spectre simulations for output bins 8-15 of the 16-point analog ADFT design.

realized by the cascaded current-mode architecture. Since the bias currents grow in magnitude when traversing from input to the output through the factorization stages, the absolute values of the current matching errors also tend to grow. Thus,

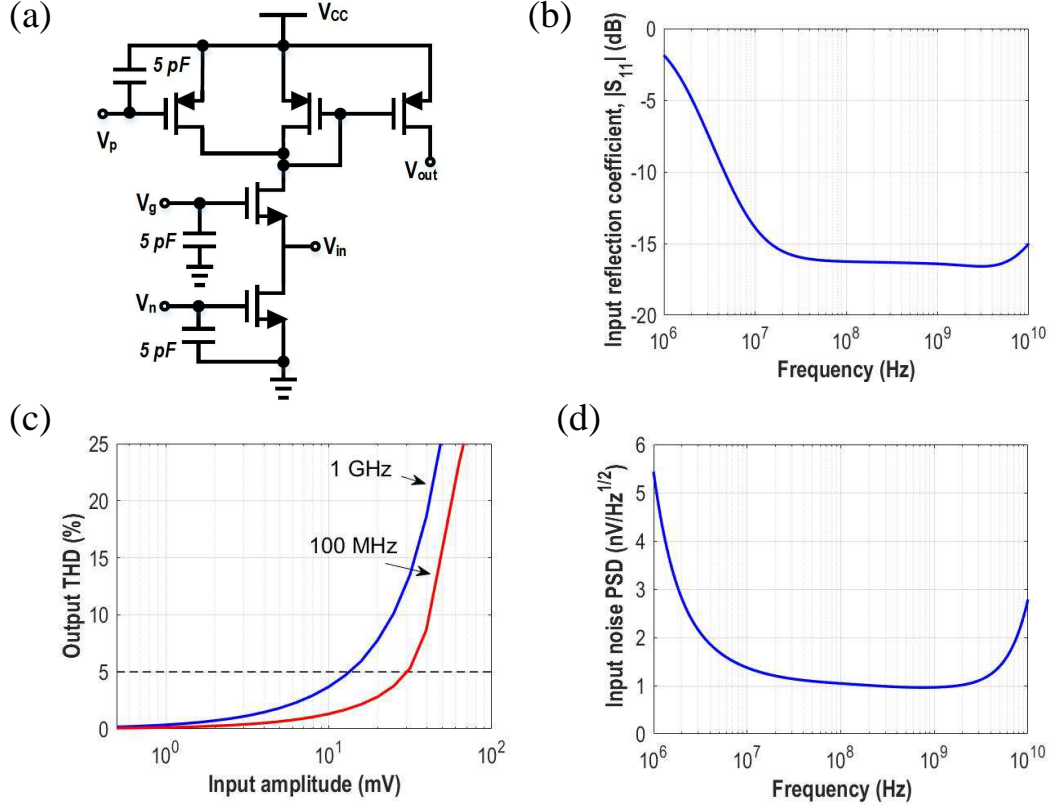


Figure 6.7: (a) The proposed V-I converter circuit. (b) Simulated input reflection coefficient $|S_{11}|$. (c) Simulated THD versus input amplitude. (d) Simulated input-referred noise PSD over the frequency range from 1 MHz to 10 GHz.

the realized coefficient values deviate from the required ones, resulting in deviations in the beam patterns. Nevertheless, these changes are in the stop band and are lower than the maximum side lobe level. Thus, they are of minor importance for beamforming applications. However, they become more significant as the frequency increases. At a baseband frequency of 500 MHz the average and worst case peak lobe levels were -12.9 dB and -11.85 dB, respectively. At 1 GHz and 1.5 GHz these numbers increased to -12.2 dB and -11.32 dB (average) and -10.17 dB and -9.08 dB (worst case), respectively.

6.3.4 Design of V-I/I-V Converter Circuits

As shown in Fig. 6.2, V-I/I-V converter circuits are necessary for interfacing the current-mode ADFT core with external circuits. Thus, such converters have to be added with $50\ \Omega$ impedance at each input and output port of the ADFT realization circuit. The noise and linearity of the V-I converter dominate the dynamic range (DR) of the multi-beamformer. The VI converter design shown in Fig. 6.7(a) uses a common-gate input stage for impedance matching. The bias current is adjusted via V_n to set the desired input impedance $Z_{in} \approx 1/g_s$, while the AC current is mirrored to create the output current I_{out} . The DC value of I_{out} , which sets the power consumption and bandwidth of the current-mode core, can be independently adjusted via V_p .

Fig. 6.7 shows simulation results for the V-I converter for a NMOS bias current (set by V_n) of 1.6 mA, a PMOS bias current (set by V_p) of 1.1 mA, and an output bias current of $(1.6 - 1.1) = 0.5$ mA. The power consumption is 2.38 mW. A Bode plot of the effective small-signal transconductance G_m (see Fig. 6.7(c)) shows a -3 dB bandwidth of 2.7 GHz. The lower cut-in frequency is set to $f_c \approx g_s / (2\pi C_{dc})$ by the value C_{dc} of an input DC blocking capacitor (not shown here). The circuit is well-matched over the useful frequency range: $|S_{11}|$ is approximately -16 dB from 10 MHz to 4 GHz as shown in Fig. 6.7(b). The input-referred noise power spectral density (PSD) - including noise from the source resistance - is $\approx 1\ \text{nV/Hz}^{1/2}$ as shown in Fig. 6.7(f). The resulting noise figure (NF) is 6-8 dB over the operating bandwidth, which is adequate since in practice this baseband circuit will be preceded by an RF receiver chain. The total integrated (1 MHz~10 GHz) output current noise is $i_{out,n} = 1.0\ \mu\text{A}_{rms}$.

The simulated total harmonic distortion (THD) versus input amplitude at two frequencies is shown in Fig. 6.7(e). As expected, THD levels increases with fre-

quency. The maximum input amplitudes for $\text{THD} < 5\%$ are $V_{in,max} = 30$ mV and 13 mV at 100 MHz and 1 GHz, respectively. Assuming no further low-pass filtering to limit the output bandwidth, the dynamic range (DR) of the circuit is

$$DR = 20 \log_{10} \left(\frac{V_{in,max} G_m / \sqrt{2}}{i_{out,n}} \right). \quad (6.1)$$

The resulting values are 49.9 dB and 42.2 dB at 100 MHz and 1 GHz, resulting in an effective number of bits (ENOB) of 8.0 and 6.7 bits, respectively. Similarly, the signal to noise and distortion ratio ($SNDR$) of the ADFT circuit is

$$SNDR = 20 \log_{10} \left(\frac{V_{in}/\sqrt{2}}{\sqrt{v_{in,n}^2 + \alpha^2 V_{in}^2/2}} \right), \quad (6.2)$$

where $v_{in,n} = i_{out,n}/G_m$ is the total input-referred noise voltage, and α is the THD at an input amplitude of V_{in} . For a 1 GHz input, the maximum value of $SNDR \approx 32$ dB occurs for an input amplitude of $V_{in} = 7$ mV, for which $\text{THD} = 2.5\%$. This results in a significantly lower ENOB of 5.0 bits. Note that the capacity of the wireless system depends on both THD and SNDR; the relative importance of these specifications thus needs further study. Given that the noise and linearity of the current-mode core and output I-V converter do not limit system performance (the latter is simply a 50Ω resistor), the ENOB of the final analog outputs are limited either by THD or SNDR to the values stated above. For the rest of the chapter it is assumed that the overall ENOB is limited by SNDR, i.e., to 5.0 bits. This level is considered very conservative precision that is sufficient for most mmW communications applications.

The finite bandwidth of the current mirrors in the ADFT core slightly reduces the output bandwidth compared to that shown in Fig. 6.7(c). The -3 dB bandwidth of a single mirror is given by $BW \approx g_m/C_{tot}$, where g_m is the transconductance of the input transistor and $C_{tot} \approx 2C_{gs}$ is the total parasitic capacitance. BW can

be improved at the cost of current matching accuracy (and eventually beam shape fidelity) by decreasing the transistor area WL , since $C_{tot} \propto WL$ and threshold-voltage mismatch $\sigma_{\Delta V_{th}} \propto 1/\sqrt{WL}$. Alternatively, it can also be improved at the cost of power consumption by increasing $g_m \propto \sqrt{I_{ds}}$. In this case the value of g_m (and thus BW) can be adjusted through the bias voltage V_p in the V-I converters. The actual circuit uses $N = 3$ cascaded mirrors (one NMOS, two PMOS) in the signal path. Assuming that these are identical, the bandwidth is further reduced to $BW \times \sqrt{2^{1/N} - 1} \approx BW/2$.

6.4 Comparison with a Baseline Digital Implementation

Equivalent digital designs for the proposed analog 16-point ADFT circuit that was implemented in hardware description language (HDL) for the work in Chapter 3 was used to compare the bandwidth, power, and area requirements with the proposed analog implementations. The digital core was synthesized using the NCSU 45 nm FreePDK library [129]. Note that this is a more advanced technology than the 65 nm process used for the analog designs. The input word length for the digital synthesis was set to 6-bits to be comparable with the SNDR-limited analog ENOB of 5.0 bits.

The figures of merit for the both digital and analog implementations are listed in Table 6.3 for comparison. The number of digital cores N_c needed for processing a bandwidth B (assuming polyphase sampling) is given by $N_c = \left(\frac{2B}{f_{s,max}}\right)$. Thus to handle a bandwidth of 1 GHz $N_c \approx 2$. The total power consumption of the digital equivalent implementation includes that of the digital cores as well as the analog-to-digital converters (ADCs). For quadrature receivers, the digital implementation requires two ADCs per antenna (in total $2 \times N$ for an N -point transform) while the analog implementation only requires two ADCs per sampled beam (real and

imaginary outputs). Therefore, when implementing an N -point transform in analog, the number of ADCs required is $2M$ where $1 \leq M \leq N$. The numbers in Table 6.3 assume the worst case, i.e., that all N beams are sampled, resulting in $M = N$. ADC power was estimated by assuming a converter with suitable specifications (≥ 1 Gs/s, ENOB = 5-6 bits) and the lowest possible Walden figure of merit (FoM). We searched Dr. Boris Murmann's ADC survey [152] for this purpose. As of writing, the lowest reported FoM is 28.7 fJ/conversion for ENOB = 5.5 bits at 1 Gs/s [153]. As shown in Table 6.3, since the bandwidth of the digital cores is ≈ 460 MHz, the ADC power is $2 \times 0.46 \text{ GHz} \times 2^{5.5} \times 28.7 \text{ fJ} = 1.2 \text{ mW}$ per channel.

According to the table, the total power consumption of the proposed analog implementation is $\approx 41\%$ less than that of the digital implementations. This is despite the fact that the digital results were obtained using a more advanced process (45 nm versus 65 nm).

There is another significant advantage of the analog implementation. In a fully-digital implementation all antenna outputs have to be amplified to span the full-scale input range of the ADCs. For example, the design in [153] has a input single-ended range of 300 mV. Amplifying all N input signals to such large levels prior to digitization is not trivial; the amplifiers have to be linear and so are power hungry. This is even more difficult if directional blockers are present, since these blockers are not rejected until after the beamformer and so the amplifiers and the ADCs have to deal with them. On the other hand, the proposed analog multi-beamformer can sit right after a baseband mixer, so only M amplifiers (one per beam) are needed. Moreover, since these amplifiers operate after the beamformer, their linearity requirements are relaxed since the beamformer can greatly suppress blockers.

Table 6.3: Comparison of 16-point analog ADFTs with digital implementations in the 45 nm FreePDK library.

	Digital Circuit	Analog Circuit
T_{cpd}	1067 ps	-
$f_{s,max}$	937 MHz	-
BW	468 MHz	1 GHz
Power	215 mW ⁽¹⁾	162.4 mW
Area	66556 μm^2 ⁽²⁾	(layout not done)
ADC power	38.4 mW	38.4 mW
V to I power	-	76.1 mW
Total power (1 GHz BW)	468.4 mW ⁽³⁾	276.9 mW
Total area (1 GHz BW)	133112 μm^2 ⁽⁴⁾	-

6.5 Conclusion and Future Work

An analog CMOS architecture that generate 16 simultaneous beams using the approximate DFT transforms introduced in Chapter 3 has discussed. The direct realization of the ADFT matrices for beamforming by mapping the proposed ADFT matrix to analog current mirrors has a hardware complexity (number of mirrors) of $\mathcal{O}(N^2)$; making it difficult to realize higher values of N for 5G systems with massive MIMO front-ends. Thus, a more scalable approach has been proposed for the realization of the 16-point ADFT in analog CMOS for obtaining 16 simultaneous beams. Instead of directly implementing the matrix, individual sparse factorization stages of the 16-point matrix is proposed to map to current mirrors. This approach reduces the number of current mirrors to $\mathcal{O}(N)$, resulting in lower hardware complexity and circuit area. However, realizing even larger values of N remains challenging.

Beamforming circuits were designed in 65-nm GP CMOS technology. The designs were simulated using Cadence Spectre to obtain the multi-beam array factors. Moreover, Cadence simulation results show high beam fidelity up to 1.5 GHz of base-band bandwidth, which is sufficient for proposed 5G communications standards.

As future work, the 16-point ADFT circuit can be laid out and fabricated to obtain measurement results. Efforts can be targeted to improve the circuit topology of the proposed V to I converter which is not particularly power efficient as it significantly increases total power consumption. Future circuit design efforts can thus be focused on designing a more power-efficient V-I topology.

CHAPTER 7

ANALOG LOW-COMPLEXITY SQUINT-FREE WIDEBAND MULTIBEAM NETWORKS

The ability to form a large number of sharp and parallel RF beams that can support high bandwidth that are not dependent on the frequency of operation is a major challenge for high-capacity wireless systems. This is a common problem to both sub 6 GHz legacy systems as well as emerging mmW systems. Emerging 5G systems promise to achieve orders of magnitude increase in the capacity and data rate owing to the proliferation of bandwidth that is being opened up but the key for enabling such throughputs rely on the ability to form multiple simultaneous beams across the full bandwidth of the link [154]. The wideband beamformers should be squint-free (this phenomenon will be explained in Section 7.1) and capable of handing the full RF bandwidth to leverage the true benefit of 5G and above 5G systems. Nevertheless, most of the initial mmW systems that uses larger antenna arrays are proposed to use analog phase shifter based beamformers due to cost of implementations. Thus, producing higher number of analog beams simultaneously that does not suffer from beam-squint is a challenging problem.

However, the realization of multibeam itself is a difficult problem as was discussed in the previous chapters, due to the associated high complexity of the aperture transceivers. The wideband beamformers require true-time-delays at each antenna path, and wideband multibeam networks would require TTD networks to achieve the required bandwidth. For example, for an N -element receiver array, the beamforming network (BFN) required for forming N beams has N beamforming networks, which in turn requires N^2 time delays or phasing elements. Thus, while conceptually simple, multi-beam array receivers and transmitters are difficult to realize in practice due to the underlying complexity of the N -beam SFG. This chapter proposes

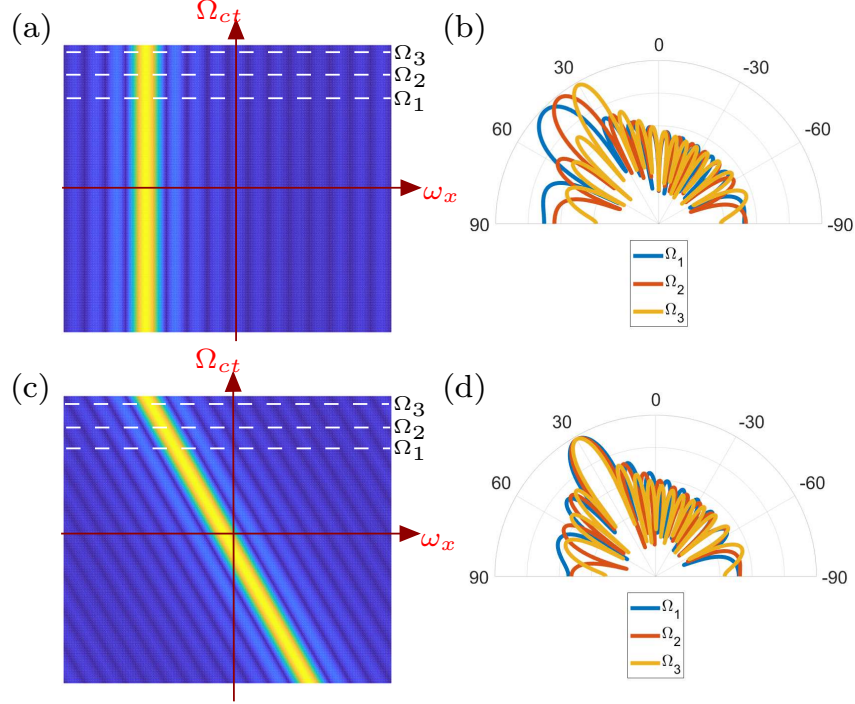


Figure 7.1: (a) 2D frequency response of a typical complex-weighted phased array beam; (b) its array factor at different temporal frequencies showing squint; (c) beam realized using true-time-delays, and (d) its squint-free array factors at different frequencies.

a method of reducing the implementation complexity of the analog non-squinting wideband N -beam networks.

7.1 The Problem of Beam Squint

In general, the beamformers that are implemented by realizing complex weightings at each antenna elements are narrowband. For the case of multibeam beamformers that are DFT based in digital or “Butler Matrix” type multi-beam array beamformers that are well known in literature on analog implementations are also narrowband. This is due to the fact that, the DFT or the Butler Matrix implements its “twiddle factors” (complex weights) which are inherently narrowband. The fact that beam-forming weights are narrowband makes the beam direction strongly depend on the

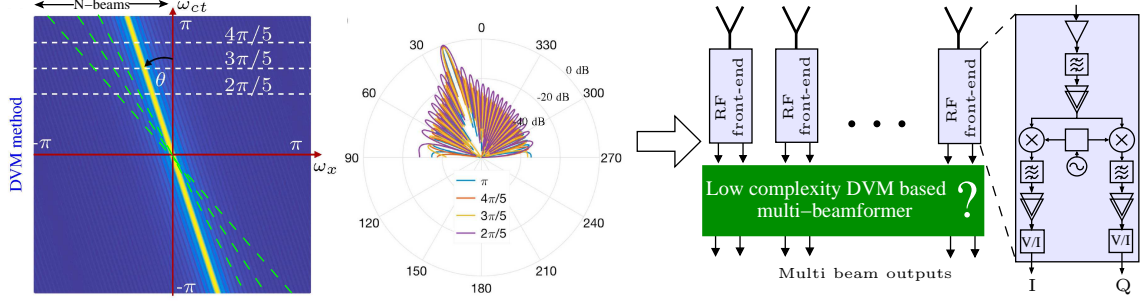


Figure 7.2: An algorithm that enables low-complexity realization of analog TTD N beam networks is desired for future wideband systems that demands higher number of multiple simultaneous beams.

temporal frequency. This phenomenon is known as the beam-squint. Fig. 7.1 illustrates this problem. Fig. 7.1(a) shows the 2D frequency response of a typical complex-weighted phased array beam. It is obvious that the passband is confined to a single spatial frequency and thereby is narrowband and works only at the vicinity of Ω_3 frequency producing the intended beam direction. Fig. 7.1(b) shows the different array factors at different temporal frequencies. It can be clearly seen that the beam direction changes with respect to temporal frequency and thus undergoes squinting. On the other hand, Fig. 7.1(c) shows the 2D frequency response of beam realized using true-time-delays. Similarly, Fig. 7.1(d) shows the squint-free array factors at different frequencies. The term Ω_{ct} in Fig. 7.1 refers to the wave speed normalized temporal (continuous-time) frequency and ω_x refer to sampled spatial frequency.

7.2 Analog Multibeam Beamformers

Analog beamforming networks which are based on either Butler matrix circuits or microwave lenses, are used to implement multi-beamforming systems in analog [57, 60, 61, 155]. BFNs consist of an antenna array fed by a multiple-input

multiple-output microwave network. The Rotman and Ruze lenses are TTD systems which provide multiple frequency independent beams (with no beam squint) [60]. A detailed article of the design of mmW Rotman lenses can be found in [156].

The Butler, Blass, and Nolen matrices are the other category of BFNs [57, 61, 155]. Butler matrix based BFNs realize the twiddle factors of the DFT matrix in analog. Since, the DFT matrix can be computed in fast-algorithms, Butler matrix based multibeam systems can be implemented at $\mathcal{O}(N \log N)$ hardware complexity. A review of Butler matrices and Nolen matrices based multibeam networks can be found in [61, 155]. The latter make use of a computer-coded algorithm for the design of the networks. Butler matrices with unequal numbers of inputs and outputs is reported in [157]. A mmW Butler matrix multibeam beamformer is proposed in [158].

Microwave lenses are wideband, provide low-phase error, and are capable of wide-angle scanning compared to the matrix-based implementations. However, lenses are large and bulky because they are typically based on planar microwave/mmW technologies. On the other hand, the TTD beamformers do provide completely squint-free wideband beams. As illustrated in Fig. 7.2, TTD beamformers do not have $\mathcal{O}(N \log N)$ complexity typical of Butler matrix/FFT beamformers or similar low-complexity realization algorithm. TTD N -beam networks are of complexity $\mathcal{O}(N^2)$. Thus, direct implementation of such beamformers are not feasible even for moderately large N and thus entailing the development of FFT-like wideband multi-beam beamforming algorithms.

Hitherto, there has been no FFT like fast algorithm proposed in the literature that reduces the incurred complexity of a wideband N beam TTD system. Therefore, this chapter investigates novel fast algorithms to obtain wideband squint-free N beam BFNs at a much lower hardware complexity using analog RF CMOS circuits.

7.3 Analog RF Squint-Free N Beam System Model

Consider a ULA of antennas where the elements are placed at the Nyquist spacing Δx (i.e. $\Delta x = \lambda_{\min}/2$ where λ_{\min} corresponds to the highest frequency of interest). It is assumed that the signals of interest of the system that impinge on the ULA is bandpass at the center carrier frequency carrier $\Omega_c = 2\pi f_c$ with a bandwidth B .

From the previous discussion in Chapter 2, the system model of a p beam network having an N element antenna array involves implementing the linear system given in (2.24). In this analysis an N beam (i.e. $p = N$) system is considered utilizing the full DoFs from the array. Therefore the system model with $p = N$ is considered and (2.24) for $p = N$ is given below.

$$\mathbf{y}_m = \mathbf{W}_N \cdot \mathbf{Z} \cdot \mathbf{a}_{pw,m}. \quad (7.1)$$

Here \mathbf{y}_m is the Fourier domain vector containing N RF beams with $\mathbf{y}_m = [y_m(0, j\Omega_t), y_m(1, j\Omega_t), \dots, y_m(N-1, j\Omega_t)]^\top$ and $\mathbf{W}_N \in \mathbb{C}^{N \times N}$ is the $N \times N$ matrix containing N beamforming vectors as given in (2.25).

$$\mathbf{W}_N = [\mathbf{w}_1, \mathbf{w}_2, \dots, \mathbf{w}_N]^\top. \quad (7.2)$$

Each $\mathbf{w}_k = [1, e^{-j2\pi f\tau_k}, \dots, e^{-j2\pi f(N-1)\tau_k}]^\top$, $1 \leq k \leq N$, where $\tau_k = \frac{\Delta x \sin \psi_k}{c}$ correspond to a steering weighting vector realizing a beam at an angle of ψ_k off broadside. Therefore, the \mathbf{W}_N matrix takes the form as given in (7.3) where $\alpha_k = e^{-j\Omega\tau_k}$.

$$\mathbf{W}_N = \begin{bmatrix} 1 & \alpha_1 & \dots & \alpha_1^{(N-1)} \\ 1 & \alpha_2 & \dots & \alpha_2^{(N-1)} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & \alpha_N & \dots & \alpha_N^{(N-1)} \end{bmatrix} \quad (7.3)$$

The system \mathbf{W}_N in (7.3) is in the generalized Vandermonde matrix structure. A low-complexity implementation of (7.3) is feasible if a sparse factorization can be

found for \mathbf{W}_N . If at all this is possible, then the TTD multibeam network that is being realized via a butterfly network has to be based on a single unit-delay element. Typically, making longer delay realizations in analog IC design is difficult. Realizing lower group delay filters such as APFs is relatively easy and longer delays are realized by cascading such smaller group-delay active elements. Therefore, if the TTD beamforming network in (7.3) is represented in a realizable group delay t_{GD} then the modified transformation matrix $\overline{\mathbf{W}}_N$ of (7.3) can be rewritten in terms of α as expressed in (7.4) where $\alpha = e^{j\Omega t_{GD}}$.

$$\overline{\mathbf{W}}_N = \begin{bmatrix} 1 & \alpha & \dots & \alpha^{(N-1)} \\ 1 & \alpha^2 & \dots & \alpha^{2(N-1)} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & \alpha^N & \dots & \alpha^{N(N-1)} \end{bmatrix}. \quad (7.4)$$

$\overline{\mathbf{W}}_N$ in (7.4) is a special form of the generalized Vandermonde structure and as it represent a physical delay matrix it will be subsequently referred to as the ‘‘DVM’’.

For a given group delay element t_{GD} and if the inter-element spacing of the antenna array is Δx , then the look-directions of the beams that would be realized by a delay network represented by the DVM in (7.4) are given by (7.5).

$$\psi_k = \sin^{-1} \frac{c \cdot k \cdot t_{GD}}{\Delta x}, \quad 1 \leq k \leq N. \quad (7.5)$$

If the beam directions of the N -beam multibeam beamformer are predetermined to be $\psi_k = \sin^{-1}(\frac{k}{N})$, then the unit TTD (τ) that needs to generate such beamforming network would be $\tau = \frac{\Delta x}{cN}$. If the antenna elements of the beamformer is critically spaced and the above required delay can be expressed in terms of the maximum frequency of interest in the system f_{max} as $\tau = \frac{1}{2f_{max}N}$.

The number of TTD elements of τ delay (or the smallest unit delay) that is required to construct the beamforming network is given by $\sum_{i=1}^N \sum_{k=1}^{N-1} k \cdot i$ and is

equal to $\frac{N^2(N^2-1)}{4}$. This chapter investigates a method of using a fast algorithm based factorization to reduce the total amount of $\frac{N^2(N-1)^2}{4}$ TTD elements needed in the squint-free wideband beamforming network.

7.4 Factorized DVM Algorithms

In general for a matrix $\mathbf{W}_N \in \mathbb{C}^{N \times N}$ determined by N^2 entries, the computational complexity of computing $\mathbf{W}_N \mathbf{x}$ for the input vector $\mathbf{x} \in \mathbb{C}^N$ costs $\mathcal{O}(N^2)$ operations, with N^2 complex multiplications and complex $N(N-1)$ additions. For well structured types of \mathbf{W}_N , e.g., like banded, Toeplitz, Hankel, Bezoutian, Cauchy, Vandermonde, Quasiseparable, DFT, etc., can be exploited to reduce the computational cost of the matrix vector product. Since the DVM is a Vandermonde structured matrix with complex entries the structure of the DVM can be used come up with a sparse factorization and also to derive a “novel” fast and stable DVM algorithm while reducing the arithmetic complexity leading to lower hardware complexity in circuit realizations.

Studying the literature, from [159, 160], if a Vandermonde matrix \mathbf{V} is of the form $\mathbf{V} = [x_i^k]_{i,k=0}^N$ where $x_0, x_1, \dots, x_N \in \mathbb{R}$ (real entries), then it can be factored into the product of 1-banded upper and lower triangular matrices with division entries by using complete symmetric functions. A $\mathcal{O}(N \log N)$ complexity algorithm has been reported in [161] to compute Vandermonde matrices having distinct prime nodes via interpolation. The work in [162] has shown that the product of a complex Vandermonde matrix and a vector can be computed using $\mathcal{O}(N \log N)$ complex arithmetic operations by exploiting its features such as using its low rank displacement structure, and pre-computing the generators. The existing work and results have all been established for the real nodes such that $x_i \in \mathbb{R}$ of the matrix

V except [159]. But the work in [159] even has limitations for a generator of the complex Vandermonde matrix. Therefore a fast algorithm that is based on complex nodes without considering quasiseparability and displacement equations is needed for the problem at hand. For this regard, our collaborator, Dr. Sirani Perera at *Embry-Riddle Aeronautical University* has proved that the LU factorization based sparse factorization for the complex nodes for reducing the $\mathcal{O}(N^2)$ implementation complexity of the N -beam TTD beamforming network. The detailed description of the algorithm, proofs and error analysis can be found in [163].

The sparse of the DVM $\overline{\mathbf{W}}_N$ over complex nodes $\{\alpha, \alpha^2, \dots, \alpha^N\}$ in (7.4) for $N \in \mathbb{Z}^+ \geq 4$ can be factored as given in (7.6) [163],

$$\overline{\mathbf{W}}_N = \mathbf{L}^{(1)} \mathbf{L}^{(2)} \dots \mathbf{L}^{(N-1)} \mathbf{U}^{(N-1)} \dots \mathbf{U}^{(2)} \mathbf{U}^{(1)}, \quad (7.6)$$

where for $1 \leq m \leq N - 1$

$$\mathbf{L}^{(m)} = \left[\begin{array}{c|cccc} \mathbf{I}_{N-m-1} & & & & \\ \hline & 1 & & & \\ & 1 & \alpha^{N-m}(\alpha - 1) & & \\ & & 1 & \ddots & \\ & & & \ddots & \ddots \\ & & & & 1 & \alpha^{N-m}(\alpha^m - 1) \end{array} \right],$$

and

$$\mathbf{U}^{(m)} = \left[\begin{array}{c|cccc} \mathbf{I}_{N-m-1} & & & & \\ \hline & 1 & \alpha & & \\ & & 1 & \alpha^2 & \\ & & & \ddots & \ddots \\ & & & & \ddots & \alpha^m \\ & & & & & 1 \end{array} \right].$$

The factorization of the DVM allows to compute the product of the DVM with a vector with only the use of the second column of the matrix $\overline{\mathbf{W}}_N$. That is, in actual circuit implementations, the number of delay elements that needs to realize $\overline{\mathbf{W}}_N$ will be reduced than the direct implementation of $\overline{\mathbf{W}}_N$. As noted in [163], since the Vandermonde matrix structure is considered extremely ill-conditioned, the condition number of the matrix tends to grow exponentially with the matrix size [164–166]. Therefore, an analysis of the error bound and the stability of the DVM factorization algorithm is important and a detail analysis of that can be found in [163]. Mathematical proof for the factorization involving complex nodes was performed by a collaborator at *Embry-Riddle Aeronautical University*. This particular approach has been used to develop example designs of 4- and 8-beam squint-free beamformers. The design approach and the challenges are discussed in subsequent sections.

7.5 4-Element Array Example using the Factorization

As an initial proof of concept, the 4-point DVM $\overline{\mathbf{W}}_4$ based 4-beam array is considered. The circuit designs for the 4-beam networks arising from $\overline{\mathbf{W}}_4$ are analyzed and the proposed beamforming networks are simulated using actual measured circuit responses that will be used as the basic realization element of the network. For

the 4-point case the DVM is given in (7.7). Here, the α represents the TTD delay $e^{-j\omega_t\tau}$.

$$\overline{\mathbf{W}}_4 = \begin{bmatrix} 1 & \alpha & \alpha^2 & \alpha^3 \\ 1 & \alpha^2 & \alpha^4 & \alpha^6 \\ 1 & \alpha^3 & \alpha^6 & \alpha^9 \\ 1 & \alpha^4 & \alpha^8 & \alpha^{12} \end{bmatrix}, \quad (7.7)$$

It is noted that direct implementation of (7.7) involves 60 TTD elements. According to the analysis in 7.4, (7.7) can be factorized into 6 sparse factorized stages as given in (7.8).

$$\overline{\mathbf{W}}_4 = \mathbf{L}_1 \mathbf{L}_2 \mathbf{L}_3 \mathbf{U}_3 \mathbf{U}_2 \mathbf{U}_1, \quad (7.8)$$

Each \mathbf{U}_i $i \in [1, 6]$ is given in (7.9).

$$\mathbf{U}_1 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & \alpha \\ 0 & 0 & 0 & 1 \end{bmatrix}, \quad (7.9a)$$

$$\mathbf{U}_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & \alpha & 0 \\ 0 & 0 & 1 & \alpha^2 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \quad (7.9b)$$

$$\mathbf{U}_3 = \begin{bmatrix} 1 & \alpha & 0 & 0 \\ 0 & 1 & \alpha^2 & 0 \\ 0 & 0 & 1 & \alpha^3 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \quad (7.9c)$$

$$\mathbf{L}_3 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & \alpha(\alpha - 1) & 0 & 0 \\ 0 & 1 & \alpha(\alpha^2 - 1) & 0 \\ 0 & 0 & 1 & \alpha(\alpha^3 - 1) \end{bmatrix}, \quad (7.9d)$$

$$\mathbf{L}_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & \alpha^2(\alpha - 1) & 0 \\ 0 & 0 & 1 & \alpha^2(\alpha^2 - 1) \end{bmatrix}, \quad (7.9e)$$

$$\mathbf{L}_1 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & \alpha^3(\alpha - 1) \end{bmatrix}. \quad (7.9f)$$

The factorized sparse matrices with elements of the matrices being mostly 1's and 0's leads to low-SWaP realizations. The low-complexity factorization, which requires only 24 delay elements, simplifies the N -beam architecture compared to the direct implementation of \mathbf{A}_4 which involves 60 TTD elements. However, the realization of a large number of delay elements that operate over a very wide band is still challenging.

Realization of the TTD in Analog-IC

The availability of a low-complexity factorization that implements delay elements simplifies the N -beam architecture. However, the realization of a large number of delay elements that operate over a very wide band is still challenging. A passive approach, based on transmission lines, is impractical for microwave frequencies, because the wavelength can be several mm or even a few cm (for S and L bands).

In lieu of transmission line solutions, analog RC-active circuit realizations of first- and second-order all-pass filters (APFs) using CMOS technology for approximating the required delays without using transmission lines. The ideal linear phase delay $e^{-j\Omega_t\tau}$ can be approximated by APFs that can be realized on-chip at low-SWaP using CMOS technology [167, 168]. Thus an analog RC-active circuit realizations of a current-mode second-order APF is proposed for approximating the required delays [168]. According to [167], an ideal unit delay of τ can be approximated as shown in (7.10). Therefore, the TTD can be realized in an analog RC-active topology using a cascade of M second-order all-pass filters.

$$e^{-j\Omega_t\tau} \approx \left(\frac{1 - j\Omega_t\tau/2M}{1 + j\Omega_t\tau/2M} \right)^M, \quad M \in \mathbb{Z}^+, \quad (7.10)$$

Typically, $M = 3$ is sufficient for approximation of τ [167]. Let $\psi(s) = \left(\frac{1 - j\Omega_t\tau/2M}{1 + j\Omega_t\tau/2M} \right)^M$ denote the transfer function of an APF approximation of the delay τ . Then, the beamforming matrix from sparse factorization of $\overline{\mathbf{W}}_4$ can be approximated by APF matrix $\mathbf{\Psi} \approx \overline{\mathbf{W}}_4$, where the (l, k) -th elements of $\mathbf{\Psi}$ takes the form $\psi^{lk}(j\Omega_t)$. Since, $\overline{\mathbf{W}}_4 = \mathbf{L}_1\mathbf{L}_2\mathbf{L}_3\mathbf{U}_3\mathbf{U}_2\mathbf{U}_1$, each \mathbf{U}_i and \mathbf{L}_i can now be realized using $\psi(j\Omega_t)$ as the unit delay to realize each coefficient. Fig. 7.3 shows the SFG resulting from the factorization which uses all-pass filter blocks having the transfer function $\psi(s)$ to approximate the TTD denoted by α . The 4 beams from the DVM $\overline{\mathbf{W}}_4$ correspond to the beams indicated 1-4 in Fig. 7.3. A 0th beam is also shown in the figure which is the direct sum beam and is independent of the factorization. All the $\psi^i(s)$ where $i \in \{2, 3, 4\}$ can be realized by cascading $i \cdot M$ identical APFs. Note that the realization of the 4th row of the factorization has been further optimized to reduced the number of delay blocks used.

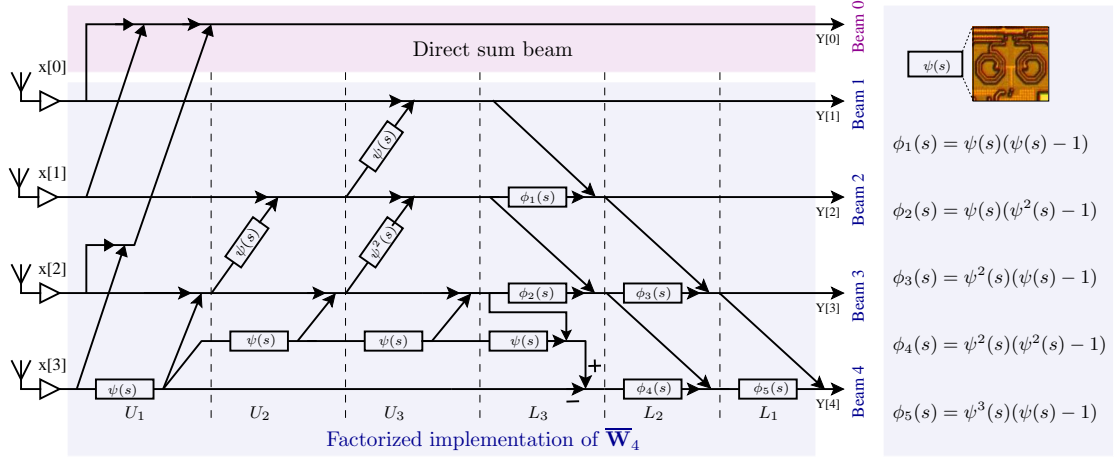


Figure 7.3: SFG of the proposed 4-point DVM factorization algorithms.

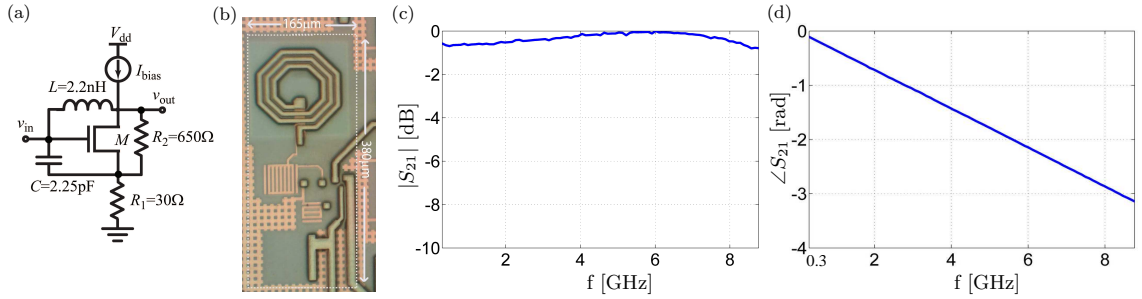


Figure 7.4: (a) CMOS all-pass circuit and the (b) die micrograph of which the measured responses are taken. (c-d) measured magnitude and phase of the APF chip (this chip was designed and developed by Dr. L. Belostotski at University of Calgary, Canada)

7.6 Simulated Beams using Measured APF Data

As a proof of concept, measured responses from an analog CMOS all-pass filter that has been designed and built by one of our collaborators are used to evaluate the performance of the beams resulting from the factorization.

7.6.1 Second-Order Current-Mode CMOS All-pass Filter

The all-pass filter that was used for the simulations was a second-order current-mode CMOS all-pass filter designed using a single-transistor that is a complementary circuit to Type-1 (filter #1) circuit [168]. The circuit of the APF is shown in Fig. 7.4. The APF design employs a capacitor C for the original element Z_1 , a resistor R_2 and the transistor output conductance g_{ds} for Z_2 , and an inductor L for Z_s . The transistor M is biased with a PMOS current source I_{bias} . Without accounting for parasitic effects due to gate-drain capacitance, which tend to increase the order of the filter to three, this circuit is a 2nd order circuit described by the transfer function:

$$\psi(s) = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{s^2 + (1 - K) \frac{\omega_z}{Q} s + \omega_z^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \quad (7.11)$$

where $K = \frac{1+g_m R_2}{1+R_1 R_2 C/L}$ and $Q = \frac{\omega_0 C L}{C R_2 + L/R_1}$. To implement the 2nd-order all-pass filter, the circuit has been designed such that $K = 2$ and $Q < 1/2$ to avoid complex conjugate poles and zeros. The group delay of the resultant filter is:

$$t_0(\omega) = \underbrace{\frac{2\omega_0 C L / Q}{1 + R_2 (R_1^{-1} + g_m)}}_{t_0} \times \frac{\left(\frac{\omega^2}{\omega_0^2} + 1\right)}{\left(\frac{\omega^2}{\omega_0^2} - 1\right) + \frac{t_0^2 \omega^2}{4}}, \quad (7.12)$$

where t_0 is the low frequency delay. The input resistance of this circuit is $R_{\text{in}} \approx R_1 + 2(CR_1/L + 1/R_2)$. The output resistance is determined by the signal-source resistance R_s and is $R_{\text{out}} \approx R_s \parallel (g_m^{-1} \parallel R_2 + R_1)$. In this work both R_{in} and R_{out} have been designed to be near 50Ω to allow measurements with standard laboratory equipment. The schematic of the APF circuit is shown in Fig. 7.4(a), and results in $g_m = 62 \text{ mA/V}$, $\omega_0 = \omega_z \approx 6 \text{ GHz}$, and $Q \approx 0.36$. The die micrograph of the chip that has been used to obtain the measured responses are shown in Fig. 7.4(b). Corresponding measured magnitude and phase of the all-pass filter chip is shown in Fig. 7.4(c) and (d), respectively. The power consumption of the filter has been

calculated to be 18.5 mW from a 1.5 V supply. In Section 7.6.2, the measured results of the APF chip are used to obtain the wide-band squint free beams based on the efficient factorization of DVM.

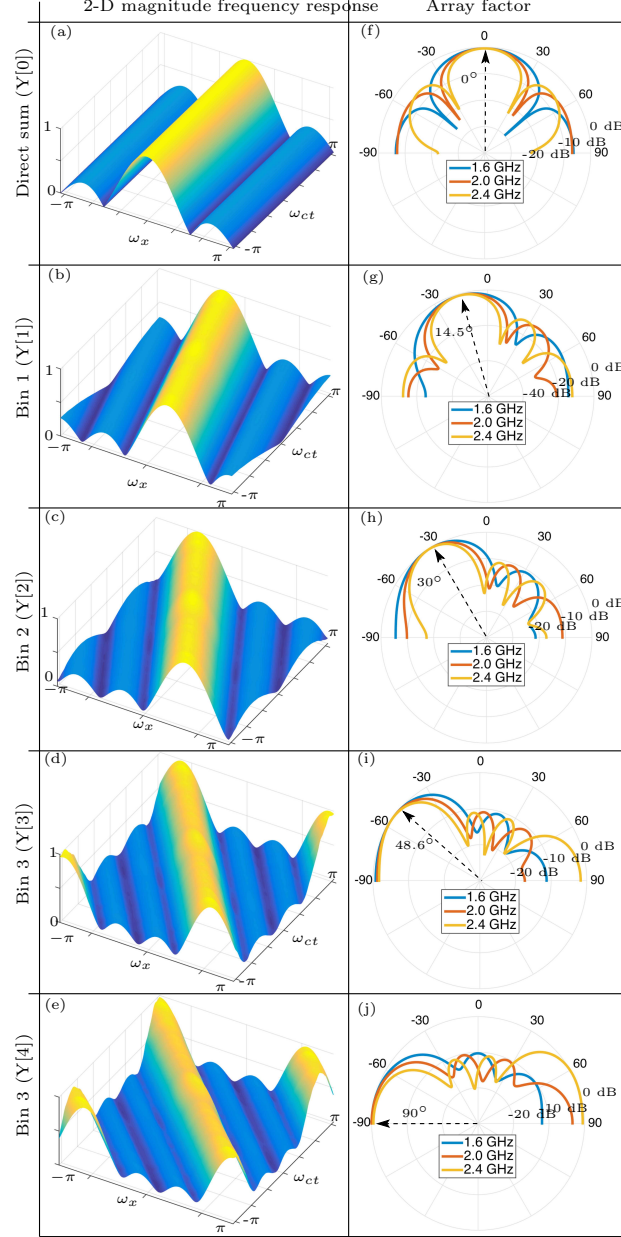


Figure 7.5: 2-D frequency response of (a-e) beams corresponding to $Y[0]$, $Y[1]$, $Y[2]$, $Y[3]$ and $Y[4]$; (f-h) corresponding array patterns for temporal frequency values 2.4, 2.0, and 1.6 GHz.

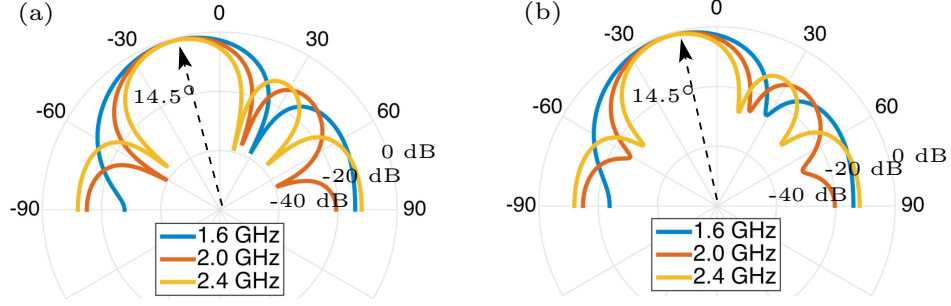


Figure 7.6: Comparison of the array factors corresponding to beam no. 1 (a) using ideal TTD and (b) measured APF data.

7.6.2 Simulated 5-Beams using Measured APF Data

The five beams given by the full SFG shown in Fig. 7.3 were simulated in Matlab using the measured APF data. The group delay T_{GD} of the APF was calculated as $57ps$. The antenna spacing is determined such that $\Delta x = c T_{GD} N$. For $N = 4$, this spacing is $68mm$. Fig. 7.5 shows the magnitude 2D frequency response and the corresponding array factors of the simulated beams. Fig. 7.5 (a) and (f) show the magnitude 2D frequency response of the direct sum beam and the corresponding array factors, respectively. The array factors have been simulated for the frequencies 2.4, 2.0, and 1.6 GHz. Fig. 7.5 (b-e) respectively show the 2D magnitude frequency response for the beams corresponding to factorized \mathbf{A}_4 , obtained using the measured APF data. In Fig. 7.5 the simulated squint-free array factors obtained for each of the beams are depicted. Fig. 7.6 (a-b) compares the simulated array factor from of the 1st beam for both measured and ideal APF responses.

7.7 Using Factorized DVM for Achieving Wideband Multibeam at IF

Performing the multibeam beamforming in analog-IF stage rather than the RF can be advantageous in some scenarios. Specially, for cases like mmW systems, performing the beamforming in the RF can be much costlier than doing it in IF or baseband. These mmW systems may realize multi-beams using IF analog micro-electronics that support the required bandwidths.

As described in Chapter 6, the use of DFT/FFT along the spatially sampled signals in IF/baseband (in an N element ULA) would sample the spatial frequency axis to N number of points yielding N beam outputs pointing to unique look directions (corresponding to the respective spatial frequency) at each output bin of the DFT [169]. The use of the FFT provides the lowest hardware complexity for realizing a simultaneous N independent beam architecture [169] in such systems. Such systems has a computational circuit complexity of $\mathcal{O}(N \log N)$. In Chapter 6, methods of achieving simultaneous multibeam in analog at much lower circuit complexity (lower than that of using FFT) with the use of DFT approximations were investigated.

Albeit of these methods being less hardware complex, as described earlier in this chapter, the FFTs do not provide squint-free wideband beams. This is in fact true for any wideband beamforming approach either at RF or IF. This section will analyze the algorithmic and circuit level ideas that is needed to obtain squint free N simultaneous beams in analog IF. Thus, a low complexity, wideband IF beamforming architecture having the overview architecture shown Fig. 7.7 that extends the theory proposed in the previous sections is investigated. Lower complexity is achieved by introducing a sparse factorization to the TTD multi-beam matrix, which leads to a

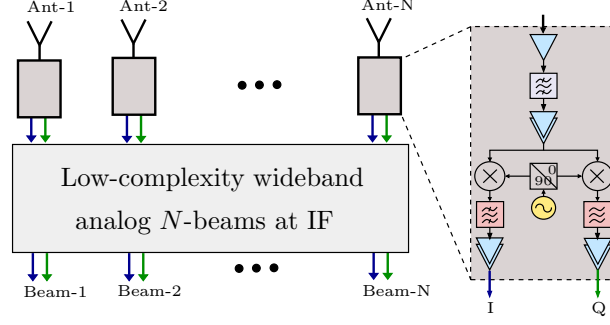


Figure 7.7: Overview architecture of a wideband N -beam array at IF.

lower number of required TTD elements and phase compensators. TTD elements are proposed to realize using analog CMOS APF circuits, which can be efficiently implemented.

7.7.1 Proposed TTD IF Multi-Beamformer Model

Let's consider a uniform linear array of antennas where the elements are placed at the Nyquist spacing Δx (i.e. $\Delta x = \lambda_{\min}/2$ where λ_{\min} corresponds to the highest frequency of interest). Assume that the signal of interest that impinges on the array is assumed to have a bandwidth of B centered around the modulated carrier f_c . Therefore, $\lambda_{\min} = \frac{c}{f_c + B/2}$ where c is the speed of propagation of the waves. Following (2.19), the frequency response of a beamformer that forms a beam at a direction ϕ is given by,

$$H(e^{j\omega_x}, \Omega_t, \psi) = \sum_{k=0}^{N-1} e^{-jk(\omega_x + \frac{\Delta x}{c}\Omega_t \sin \psi)}. \quad (7.13)$$

Here, ω_x stands for the normalized spatial frequency ($-\pi \leq \omega_x < \pi$) and $|f - f_c| \leq B/2$ where $f = \frac{\Omega_t}{2\pi}$ is the temporal frequency in Hz. A system having an IF stage with synchronous mixers $\Omega_{IF} = \Omega_t - \Omega_{LO}$, where Ω_{IF} denotes the down-converted frequencies of the signal and Ω_{LO} is the local oscillator frequency is assumed. For direct down-conversion receivers, Ω_{LO} is selected as Ω_c . Thus, in this model, $\Omega_{IF} =$

$\Omega_t - \Omega_c$. The equivalent IF response is given by,

$$H(e^{j\omega_x}, \Omega_{IF}, \psi) = \sum_{k=0}^{N-1} \alpha^k e^{-jk\omega_x}, \quad (7.14)$$

where $\alpha = e^{-j\frac{\Delta x}{c}(\Omega_{IF} + \Omega_c) \sin \psi}$.

The model in (7.14) is equivalent to (7.13) unless the fact that the weights at each k th antenna element in the frequency domain needs to realize a TTD delay and phase rotation of the signal for generating the beam. The multibeam network for generating N beams in IF also follow (2.24) where the multibeam matrix is equivalent to (2.25) with each $\mathbf{w}_k = [1, e^{-j\Omega_{IF}\tau_k} e^{-j\Omega_c\tau_k}, \dots, e^{-j\Omega_{IF}(N-1)\tau_k} e^{-j\Omega_c(N-1)\tau_k}]^\top$, $1 \leq k \leq N$, where $\tau_k = \frac{\Delta x \sin \psi_k}{c}$. Following the discussion in Section 7.3, for a realizable unit TTD t_{GD} , by making the multi-beam look directions to be $\psi_k = \sin^{-1} \frac{c \cdot k \cdot t_{GD}}{\Delta x}$, $1 \leq k \leq N$, the multibeam network can be represented as given in (7.15) where $\alpha = e^{-j\Omega_{IF}\tau} e^{j\Omega_c\tau}$.

$$\overline{\mathbf{W}}_N = \begin{bmatrix} 1 & \alpha & \dots & \alpha^{(N-1)} \\ 1 & \alpha^2 & \dots & \alpha^{2(N-1)} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & \alpha^N & \dots & \alpha^{N(N-1)} \end{bmatrix} \quad (7.15)$$

Realization of $\overline{\mathbf{W}}_N$ an analog IF requires $\frac{N^2(N^2-1)}{4}$ realizations of the delay elements ($e^{-j\Omega_{IF}\tau_{kl}}$) and phase compensators ($e^{-j\Omega_c\tau_{kl}}$). However, using the same approach in Section 7.4, the realization of the factorized version $\overline{\mathbf{W}}_N$, reduces the number of TTD and phasing elements in the whole N -beam realization and therefore becomes much SWaPC efficient compared to a direct implementation of $\overline{\mathbf{W}}_N$. The specific case of $N = 4$ will be used to show how reduced complexity analog IF circuit realization can be done to achieve the multibeam in analog CMOS and also how the design can be extended to get a 9 beam network covering both boresight quadrants of the array.

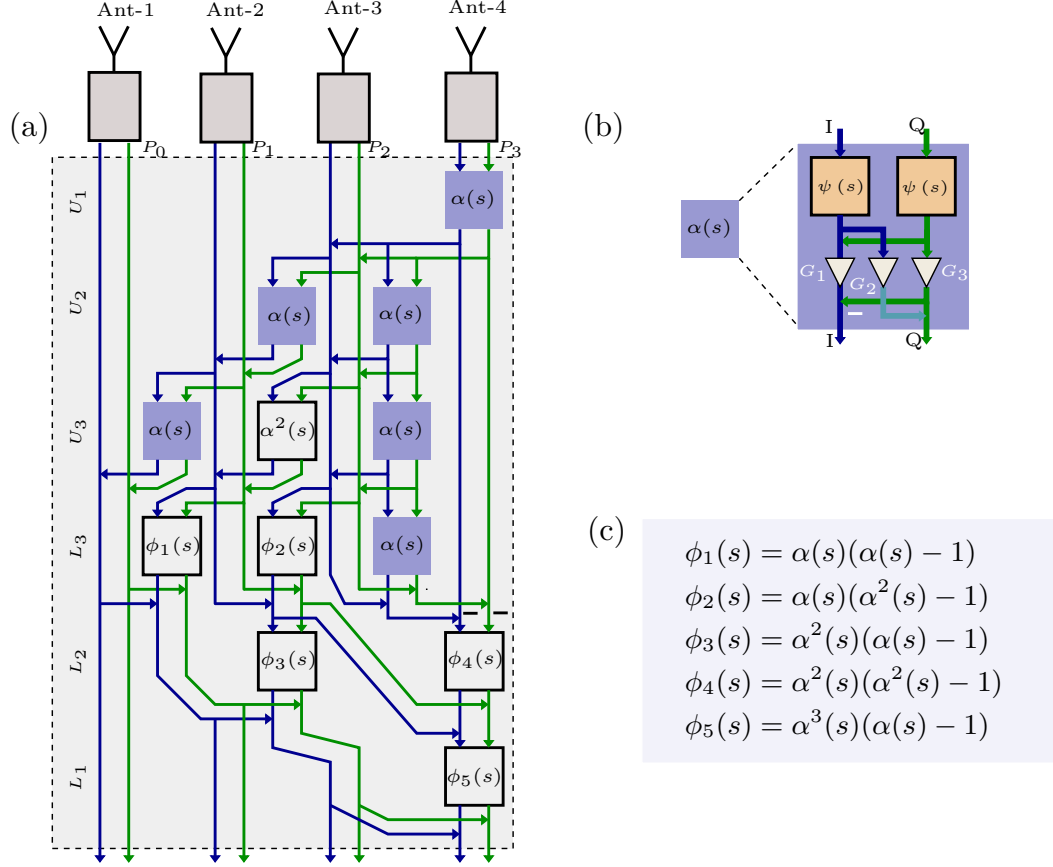


Figure 7.8: (a) Overview of the system architecture of the 9 beam multi-beamformer; (b) signal flow graph for realizing 4 beams having look directions at $\sin^{-1} \frac{l}{4}$, $l \in \{1, 2, 3, 4\}$; (c) analog-IC realization of the $\alpha(s)$ block using APFs.

7.7.2 All-Pass-Filter Based 4-Beam Analog IF Beamformer

The IF multibeam model in (7.15) for $N = 4$ is given in (7.16). Here, $\alpha = e^{-j\Omega_{IF}\tau} e^{-j\Omega_c\tau}$.

$$\overline{\mathbf{W}}_4 = \begin{bmatrix} 1 & \alpha & \alpha^2 & \alpha^3 \\ 1 & \alpha^2 & \alpha^4 & \alpha^6 \\ 1 & \alpha^3 & \alpha^6 & \alpha^9 \\ 1 & \alpha^4 & \alpha^8 & \alpha^{12} \end{bmatrix} \quad (7.16)$$

From (7.8) it is clear that the $\overline{\mathbf{W}}_4$ in (7.16) can be factorized as $\overline{\mathbf{W}}_4 = \mathbf{L}_1 \mathbf{L}_2 \mathbf{L}_3 \mathbf{U}_3 \mathbf{U}_2 \mathbf{U}_1$. The factorization is equivalent unless the fact that the α ar-

gument is now $\alpha = e^{-j\Omega_{IF}\tau}e^{-j\Omega_c\tau}$. Therefore, it can be seen that the 4-beam IF network will be different than that of the RF implementation in Section 7.5. But the implementation of \mathbf{U}_i 's and \mathbf{L}_i 's significantly reduces the amount of $\alpha(s)$ blocks required in the signal flow graph and provide the same gain in complexity reduction with respect to the direct implementation to realize $\overline{\mathbf{W}}_4$.

Since $e^{-j\Omega_c\tau}$ can be approximated by $\psi(s) = \left(\frac{1-j\Omega_c\tau/2M}{1+j\Omega_c\tau/2M}\right)^M$, where $M \in \mathbb{Z}^+$, the ideal unit delay τ can be approximately realized in an analog RC-active topology using a cascade of M second-order all-pass filters as described in Section 7.5. Therefore, the beamforming matrix from sparse factorization of $\overline{\mathbf{W}}_N$ can be approximated by an approximately equivalent APF matrix $\Psi \approx \overline{\mathbf{W}}_N$, where the (k, l) -th $(k, l \in [0, \dots, N-1])$ element of Ψ takes the form $\psi^{kl}(j\Omega_{IF}) \cdot e^{-j\Omega_c\tau kl}$ and approximates the transfer function $\alpha^{kl}(s)$. A possible implementation of $\alpha(s)$ is shown in Fig. 7.8(b). Fig. 7.8(a) shows the the SFG for realizing Ψ from the proposed factorization in (7.8). Fourth row of the factorization has been further optimized to reduce the number of delay blocks used. The blocks denoted as $\psi^i(s)$ in the SFG where $i \in \{2, 3, 4\}$, can be realized by cascading $i \cdot M$ identical realizations of $\alpha(s)$.

As illustrated in Fig. 7.8(b), the outputs of the APFs are followed by a weighted sum to realize the phase compensation corresponding to $e^{-j\Omega_c\tau}$ term required in IF beamforming. Fixing the multibeam directions to be $\psi_k = \sin^{-1} \frac{1}{N}$ makes the required unit TTD $\tau = \frac{\Delta x}{cN}$. Since for a critically sampled array $\Delta x = \frac{c}{2(f_c+B/2)}$, that makes $e^{-j\Omega_c\tau} = e^{\frac{-j\pi}{N} \cdot \frac{f_c}{f_c+B/2}}$. The analog integrated circuit architecture needed for realizing $e^{\frac{-j\pi}{N} \cdot \frac{f_c}{f_c+B/2}}$ is illustrated in Fig. 7.8(b). Both in-phase and quadrature signals at the output of the APFs can be scaled three CMOS gains (G_1, G_2, G_3) according to Gauss complex multiplication algorithm [170] to obtain the complex phase rotation of the signal by $e^{\frac{-j\pi}{N} \cdot \frac{f_c}{f_c+B/2}}$. If $\gamma = \frac{-\pi}{N} \cdot \frac{f_c}{f_c+B/2}$, these gains can be calculated as $G_1 = \cos \gamma$, $G_2 = \sin \gamma - \cos \gamma$, and $G_3 = \sin \gamma + \cos \gamma$.

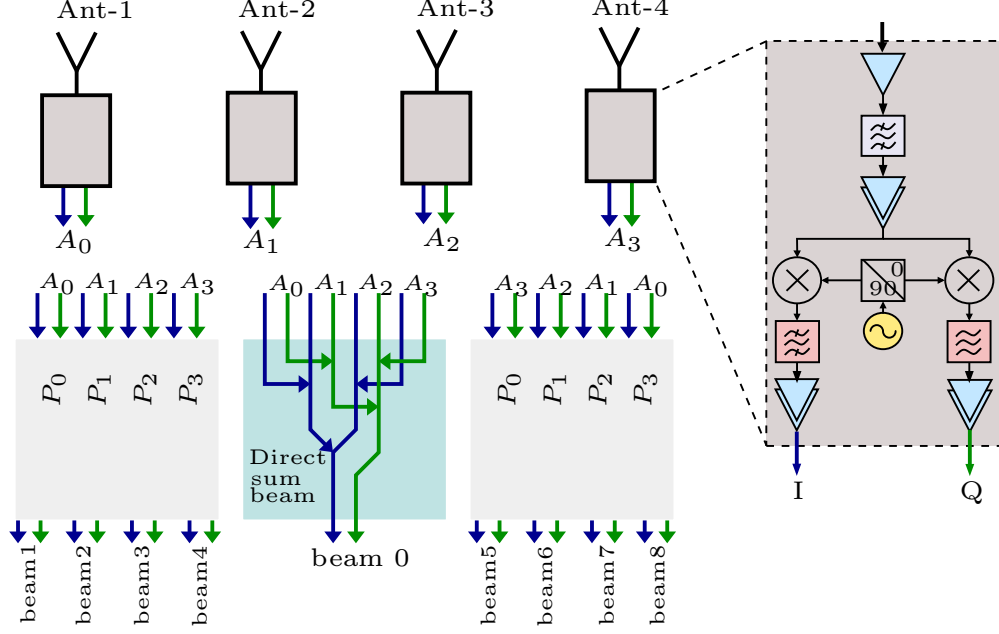


Figure 7.9: Overview of the system architecture of the 9-beam multi-beamformer.

It has to be noted that the direct implementation of the BFN denoted by $\Psi(s)$ would require 120 unit TTD and phase compensation hardware blocks. The implementation through the DVM factorization provides a 60% reduction in hardware by making it viable to implement the BFN using only 48 TTD elements phase compensation hardware.

7.7.3 Extending the 4-Beam Algorithm to Generate Simultaneous 9-Beams

In this section we propose a 9-beam analog IF beamforming architecture extending the 4-beam realization in Section 7.5. Due to the causal nature of the TTD beamforming network, the beams realized (using a ULA) are confined to a single quadrant of the boresight. For a given TTD beamformer that forms a beam in the

direction ψ measured from the array broadside where $-90^\circ \leq \psi_l \leq 0^\circ$, the order of the antenna outputs that is fed to a TTD beamformer can be reversed to achieve a beam at $-\psi_l$ direction. Therefore, a separate copy of the circuit that realizes the SFG shown in 7.8(a) can be used with the reversed order of antenna inputs to create a similar set of beams in the adjacent quadrant. Also, as mentioned in 7.5 the direct sum beam that generates a broadside beam can be generated independent of the factorization with only using summing circuits. These concepts can be used to achieve 9-beams all together pointing at non-uniformly spaced directions given by $\sin^{-1}\left(\frac{l}{N}\right)$ for l given by $l = 0, \pm 1, \pm 2, \pm 3, \pm 4$ and $N = 4$. Fig. 7.9 illustrates the architecture of such beamforming network that generates 9-wideband beams in analog IF.

7.8 Simulated Beams Using Ideal APF Responses

A high bandwidth (up to 16 GHz) APF has been designed in [167] which has a group delay of 57 ps using 65 nm CMOS. Therefore, realizing a APF that has a matching group delay for a specific beamformer is possible in CMOS [168, 171]. Wireless systems that operates at K_a or V bands would require an APF implementations that realizes a shorter delay (than in [167]). But such filters doesn't have to operate at such high RF as the proposed architecture deals with analog IF implementations. Therefore, design of a CMOS circuit (to approximate the transfer function for the ideal delay) that can realize an APF with a shorter delay that satisfies the group delay requirements in a mmW wireless system is assumed. As a proof of concept, ideal APF response are used to simulate the beams and to verify the functional correctness of the proposed 9-beam beamformer. A bandpass system in RF with $f_c = 60$ GHz, $B = 10$ GHz is assumed where the signals are down-converted to

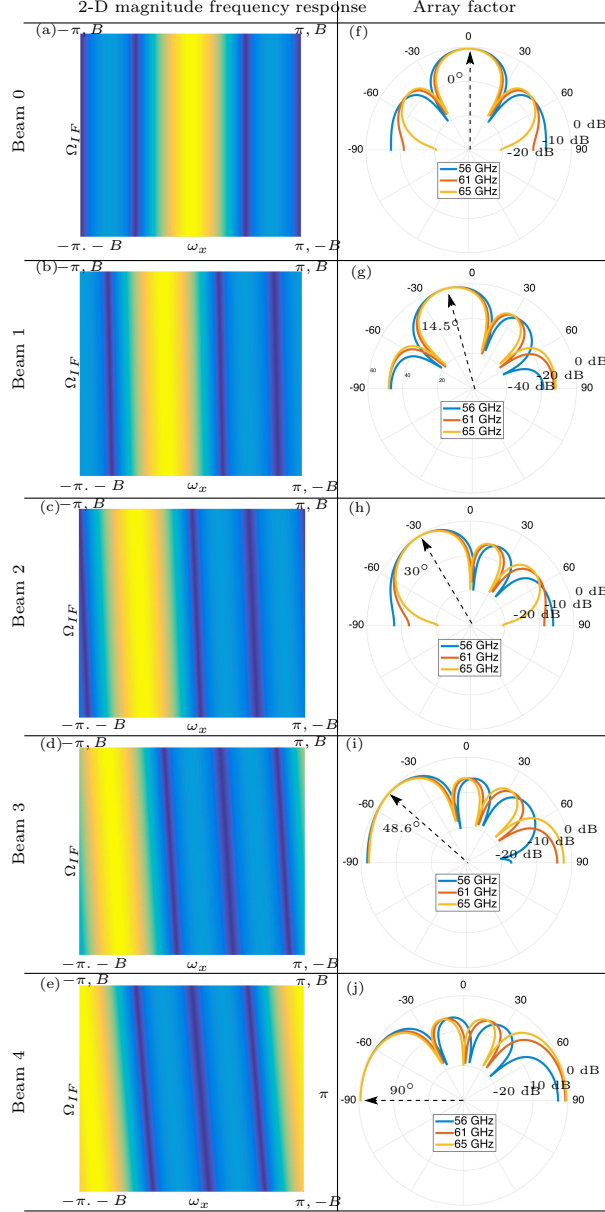


Figure 7.10: Simulated 2-D frequency response of (a-e) beams in the IF stage corresponding to beam 0 to beam 4 respectively using ideal APF responses; (f-h) corresponding array patterns for temporal frequencies 56, 61 and 65 GHz.

$-5 \leq f_{IF} \leq 5$ GHz. Thus for achieving grating lobes free beamforming in the band 55 – 65 GHz, the required group delay T_{GD} of the APFs (the minimum TTD needed in the system) can be calculated as $T_{GD} = \frac{\Delta x}{cN}$ where Δx is the inter-element spacing chosen to satisfy Nyquist spatial sampling. Therefore, $\Delta x = \frac{c}{2f_{max}}$ and thereby

$t_{GD} = \frac{1}{2f_{max}N}$ where f_{max} is the highest frequency of interest in the system which is given by $f_c + B$. In such case t_{GD} can be calculated as 1.92 ps. Fig. 7.10 shows the simulated beam patterns obtained using the factorization of $\overline{\mathbf{W}}_4$. Figs. 7.10 (a-e) shows the 2-D magnitude frequency of the individual IF beams and the Figs. 7.10(f-j) depicts the corresponding array factors obtained for different temporal frequencies $f \in \{56, 61, 65\}$ GHz. Since a mirrored copy of the signal flow graph is used to achieve multi-beams in ++ and -+ quadrants, beams and the array factors are only shown for the -+ quadrant.

7.9 Conclusion

Low-SWaP squint-free wideband multibeam beamforming networks have been investigated. A low-complexity TTD implementation method of wideband N beam beamforming network has been derived and analyzed. By using the proposed method, the required number of TTD elements for implementing the N -beam networks in both RF and IF can be reduced through the use of sparse factorization of the DVM. A theoretical analysis of complexity bounds in the proposed algorithm has been conducted.

To confirm the validity of the proposed method, 4-point DVM has been considered. Sparse factorization of the DVM $\overline{\mathbf{W}}_4$ that realizes 4-simultaneous wideband beams at RF reduces the required TTD elements from 60 to 24 achieving 60% hardware reduction to obtain a low complex realization. The 4-beam beamforming network has been simulated using measured all-pass filter responses and The measured results from a CMOS APF have been used to simulate the wideband beams that have bandwidths exceeding 2.4 GHz.

Low complexity, squint-free simultaneous multiple beams are proposed for wide-band IF beamforming. All-pass filters are employed as the true-time delay elements. Factorization of the DVM is proposed to reduce the complexity associated with the beamformer, where each element of the matrix corresponds to the compound phased compensation. Proposed multi-beamformer provides a 60% reduction in TTD elements (from 120 to 48) and the required phased compensation hardware. A simulated example shows squint-free multi-beams for the 55-65 GHz band using down-conversion to 10 GHz IF.

CHAPTER 8

HYBRID BEAMFORMING ARCHITECTURES FOR SQUINT-FREE OPERATION

This chapter extends the discussion of Chapter 7 to investigate a low-complexity hybrid (analog-digital) multibeam beamforming architectures that does not suffer from beam squint. The proposed architectures can be used to achieve low-SWaP beamforming of wideband 5G signals by employing hardware and power efficient beamforming at both analog and digital thereby reducing the required number of ADCs in the array leading to ultra-low power consumption. The analog beamforming architecture is based on the sparse factorization of the N -beam TTD DVM that was proposed in Chapter 7.4 which can be efficiently realized at RF (mmW) using analog circuits; in particular as APFs in CMOS. A low-complexity digital beamforming method is proposed to perform wideband digital beamforming as the 2nd level low-dimensional beamforming. Actual circuit response of an APF on analog 45 nm CMOS that has been designed and implemented by one of our fellow collaborators in University of Calgary has been used to verify the proposed beamforming architecture at 28 GHz.

8.1 Hybrid Beamforming Systems

A brief review of digital-beamforming (DBF), analog-beamforming (ABF), and hybrid-beamforming (HBF) was provided in Chapter 2.5. As mentioned there, DBF delivers maximum flexibility including multiple beams [172], high dynamic range, and high accuracy using digital calibration [173, 174]. However, DBF requires one RF chain and two ADCs per antenna element (assuming I-Q downconversion), i.e., P RF chains and $2P$ ADCs for P antenna elements. This results in high power consumption because of the large number of ADCs, which are usually the most

power-hungry blocks in receivers [40]. Moreover, the real-time signal processing required to generate beams from the digitized data consumes a large amount of additional power, making large-scale DBF implementations (e.g., for $P = 64$ or 128 elements) challenging and impractical at higher frequencies like mmW [175]. Since wireless systems in 5G and beyond 5G will require large antenna arrays (e.g. with $P = 64$ or 128 elements) to achieve high receiver gains due to the greatly reduced physical array size owing to the decrease in wavelength. Implementing the same number of transceivers as the number of antennas may not be feasible due to excessive demand on real-time signal processing that results in high power consumption, and high cost [175].

HBF networks [41] addresses this challenge by combining low-dimensional digital beamformers (at baseband) with analog beamformers (at RF). A generic overview architecture of a HBF receiver is shown in Fig. 2.11(c). Such architectures can achieve performance similar to fully-digital schemes at lower cost and power. They typically use RF phase-shifters, TTDs, or lenses for level-1 analog beamforming [41–43] to form a beam in all sub-arrays and the beamformed outputs from all the subarrays are sampled to perform level-2 beamforming in digital baseband processing. Considering the needs of future beamforming systems, beamforming arrays that can produce squint-free multiple simultaneous beam are of high interest. Therefore, following these ideas, a novel optimized hybrid beamforming scheme is proposed in this chapter targetting 5G mmW base stations. Fig. 8.1 shows the overview of the proposed architecture.

Consider a P -element antenna array consisting of L N -element sub-arrays where $P = LN$ and inter-element spacing Δx is set to $\frac{\lambda_{min}}{2}$. Here λ_{min} is the wavelength corresponding to the maximum operating frequency, i.e., $f_c + B/2$ where f_c is the center frequency and B is the signal bandwidth. Each antenna output is followed by

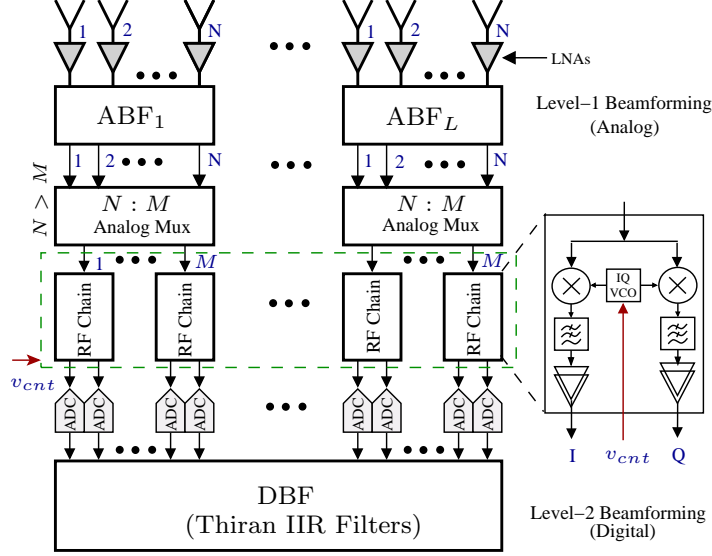


Figure 8.1: System architecture of the proposed hybrid squint-free multi-beam network.

i) a LNA, and ii) level-1 ABFs. The ABFs are proposed to use the wideband squint-free multi-beam algorithm realized at RF to generate level-1 beams. A analog $N : M$ multiplexer is then proposed to select $M \leq N$ outputs from each ABF. These signals are I-Q downconverted and amplified by LM parallel RF chains, and digitized by $2LM$ ADCs. The digitized baseband signals are further processed by a DBF to generate narrow level-2 beams. Since $M < N$, the proposed hybrid architecture reduces the total number of RF chains and ADCs by a factor of M/N compared to a fully-digital beamformer. This is because the digital system picks M analog beams from the N available from each subarray for subsequent processing. The choice of how many are needed is proportional to the capacity of the system. If the application only requires a single channel, then M can be as small as unity. On the other hand, for maximum capacity, the system needs to exploit all available beams (for e.g., if it's used in a base station or access point). In such a situation, one may digitize all N beams, so $M = N$. Therefore, the ratio lies between $1 \geq M/N \geq 1/N$

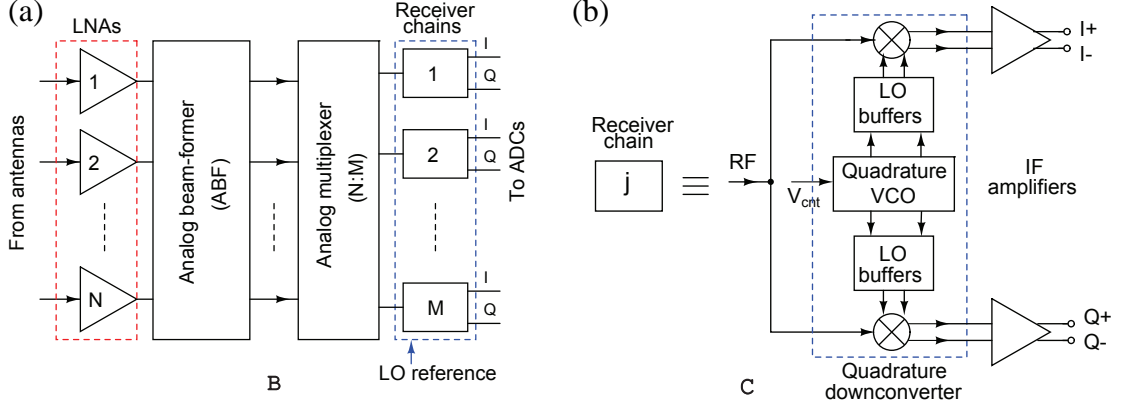


Figure 8.2: (a) High-level block diagram of the overall RF front-end architecture, (b) a more detailed block diagram of a single RF chain, (c) simplified schematic of the proposed LNA.

where M and N are both integers. When a large number of beams is not required, the number of ADC channels are $2LM \ll 2LN$.

8.2 Circuit Design for Multi-Beam Realization

A block diagram of the overall receiver architecture is shown in Figs. 8.2 (a) and (b). This section focuses on the circuit architectures of the RF front-ends; the design of ABF block is discussed in section 8.3. Each RF chain consists of i) a quadrature frequency downconverter realized using two mixers and a quadrature local oscillator (LO), and ii) IF amplifiers and low-pass filters. The outputs of the IF amplifiers are fed into parallel ADCs for digitization. Independent RF chains are used to process the M parallel outputs of the analog multiplexer. The LOs of these M receiver channels should be synchronized in order to obtain coherent outputs for digital beamforming. Thus, the LO duty cycle, skew, and jitter (both random and deterministic) has to be controlled across the array in the presence of variable routing length (μm to mm) in the power divider network. In particular, the LO distribution network often dominates out-of-band phase noise (i.e., at large offset frequencies),

making its design critical for broadband systems [176]. There are three main design approaches: i) distributing a single LO generated by a central PLL; ii) injection-locking individual LOs in each channel to that of a central PLL, resulting in a distributed PLL; and iii) distributing a low-frequency reference signal to local PLLs at each channel. Each approach results in a different trade-off between the power consumed by LO generation and distribution [177]. The local PLL option provides good performance, flexibility, and scalability at the cost of the highest power and area consumption. Thus, the central and distributed PLL options are more suitable for smaller arrays. Of these two, the central PLL is favored for broadband systems, for which injection locking becomes less power-efficient.

8.3 Level-1 Analog Multi-Beam Beamformer

The factorization of DVM based analog multibeam architecture discussed in sections 7.3 and 7.4 is proposed for level-1 analog beamforming in the mmW arrays. The linear phase shift $e^{-j\Omega_t\tau}$ associated with $\overline{\mathbf{W}}_N$ (or its factorization) can be efficiently approximated on-chip by CMOS APFs [167, 168]. It was shown in Section 7.5 that $\overline{\mathbf{W}}_N$ can be approximately realized by using APFs as building blocks. Moreover, it was discussed that the beamforming matrix from sparse factorization of $\overline{\mathbf{W}}_N$ can be approximated by the APF network matrix $\mathbf{\Psi}_N \approx \overline{\mathbf{W}}_N$. Here, an APF implemented using 45 nm CMOS technology is used to realize $\mathbf{\Psi}_N$. A direct approach to implementing $\mathbf{\Psi}_N$ would require cascading of $l \cdot k$ such APFs for realizing each (l, k) -th node. Subsequently, an example realizations of level-1 beamforming networks for $N = 4$ and 8 are analyzed and compared using the proposed DVM factorization.

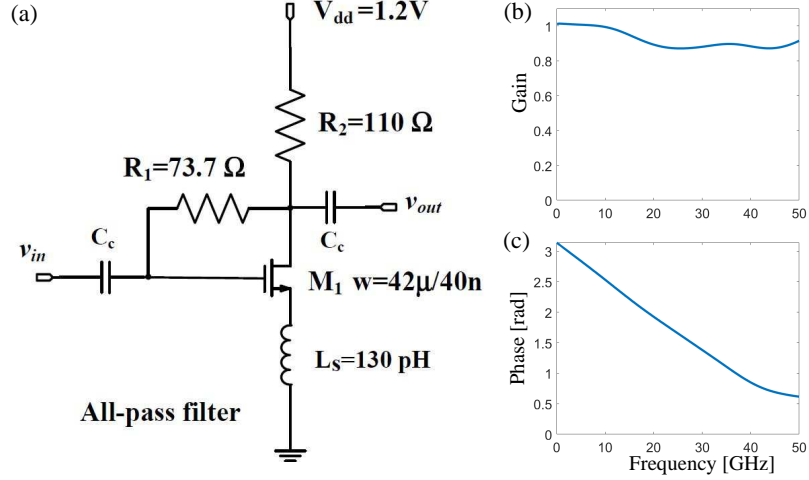


Figure 8.3: (a) APF schematic; its (b) gain and (c) phase profile.

8.3.1 28-GHz Current-Mode CMOS All-Pass Filter

The 28 GHz CMOS APF that is used to simulate the beams of the proposed HBF is a current-mode single-transistor circuit which is shown in Fig. 8.3. The APF was designed by Dr. L. Belostotski at University of Calgary and the original work can be found in [171]. Ignoring parasitic poles and zeros due to C_{gs} and C_{gd} and assuming $g_m \gg g_{ds}$, the transfer function of the circuit is given in equation (8.1).

$$H(s) = \frac{v_{out}}{v_{in}} = -\frac{R_2(R_1g_m - 1)}{R_1 + R_2} \cdot \frac{1 - s\frac{L_sg_m}{R_1g_m - 1}}{1 + sL_sg_m}, \quad (8.1)$$

where g_m is the transconductance of M_1 , L_s is a source degeneration inductor, R_1 is a feedback resistor between gate and drain of M_1 , and R_2 is a load resistor to convert current to voltage. For (8.1) to represent an APF, the left-plane pole and right-side zero should have the same frequencies. This is achieved in [171] by setting $R_1g_m - 1 = 1$, resulting in

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1 + R_2} \cdot \frac{1 - sL_sg_m}{1 + sL_sg_m}. \quad (8.2)$$

The pole and zero frequencies are $\omega_{p1} = -\omega_z = -(L_sg_m)^{-1}$, the phase response is $\phi(\omega) = -2 \tan^{-1}(\omega/|\omega_{p1,z}|)$ and the group delay $t_d = \frac{2}{\omega_{p1,z}} \cdot \frac{\omega_{(p1,z)}^2}{\omega_{(p1,z)}^2 + \omega^2}$ where ω

is the angular frequency and $\omega_{p1,z}$ denotes the pole or the zero frequency. At low frequencies $t_d \approx 2/\omega_{p1,z}$, and the term $\frac{\omega_{(p1,z)}^2}{\omega_{(p1,z)}^2 + \omega^2}$ captures the high-frequency t_d dispersion associated with all first-order APFs. Once the parasitic parameters of M , which mainly include C_{gd} and C_{gs} , are considered, high frequency poles will be generated. According to [171], the small-signal analysis confirms a dominant parasitic pole at $\omega_{p2} = -(R_1 C_{gd})^{-1}$ and to reduce the effect of ω_{p2} on the APF, R_1 is kept small and large g_m is used to ensure $\omega_{p1} = -\omega_z$. Large g_m has been achieved by providing a large overdrive voltage to M_1 while keeping M_1 's size fixed, which increases ω_{p2} while keeping C_{gd} constant.

8.3.2 Simulated 4- and 8-Beam Networks using 28 GHz APF Measured Responses

This section will use the DVM factorization that is proposed in the Section 7.4 along with the 28 GHz measured APF responses to simulate and analyze the low-complexity beam outputs. The DVM factorization for the 4-beam case ($\overline{\mathbf{W}}_4$) is given by (7.8). The signal flow graph corresponding to the factorized implementation for this case will also be similar to that is illustrated in Fig. 7.3 unless the fact that the $\psi(s)$ response now corresponds to the simulated responses of the 28 GHz APF given in Fig. 8.3. The unique look-directions θ_k s of this beamformer where $1 \leq k \leq N$, are a function of both APF group delay t_d and antenna spacing Δx . For a given t_d and Δx , the look-directions of the beams are given by $\theta_k = \sin^{-1} \frac{c \cdot k \cdot t_d}{\Delta x}$, $1 \leq k \leq N$. As mentioned in Section 7.5, the SFG in Fig. 7.3 uses only 24 APF blocks. A similar 4-beam network using a direct synthesis of TTD phased array would involve 60 such blocks. Thus the proposed approach achieves a 60% reduction in hardware complexity.

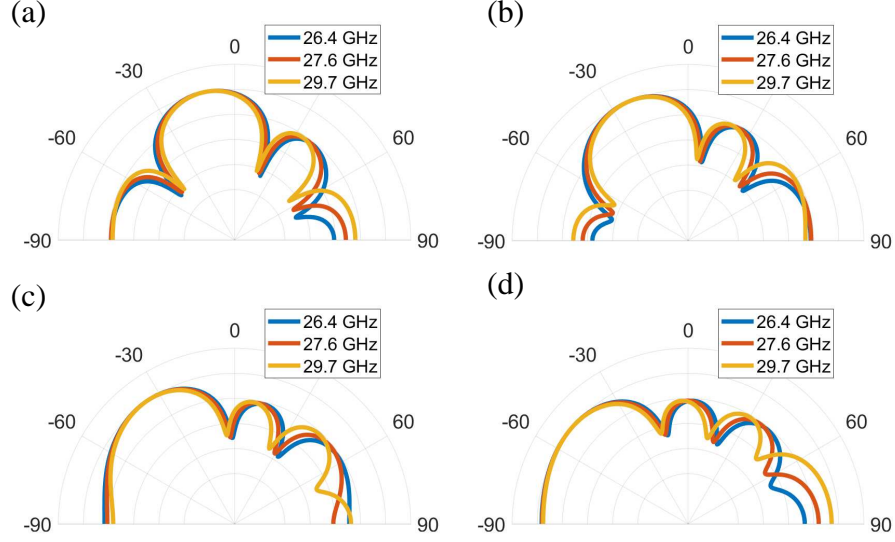


Figure 8.4: Simulated beam responses resulting from the SFG in Fig. 7.3 using the 28 GHz APF simulated frequency responses at frequencies $\{26.4, 27.6, 29.7\}$ GHz. Beams (a-d) have look-directions 11.1° , 22.6° , 35.2° , and 50.2° , respectively.

To simulate the SFG shown in Fig. 7.3, a 2 GHz signal bandwidth around a $f_0 = 28$ GHz carrier and an antenna spacing $\Delta x = \lambda_{min}/2$ to eliminate grating lobes are assumed. The APG group delay required for the beams to be within ϕ° from array broadside is $t_d = \frac{\Delta x \sin^{-1}\{\phi\}}{c \cdot N}$. The required delay was first estimated using this relationship taking $\phi = 50^\circ$, which leads to $t_d \approx 3.2$ ps for $N = 4$, resulting in four beams directed at 11.1° , 22.6° , 35.2° , and 50.2° . Next, the APF design in Section 8.3.1 was tuned in Cadence to obtain the desired group delay over the 26-30 GHz range. Average group delay was calculated as 3.202 ps using the Cadence simulated data. The simulated APF frequency response was exported to MATLAB to simulate beam responses resulting from the SFG in Fig. 7.3. Fig. 8.4 shows the array factors corresponding to beam outputs $Y[1]$, ..., $Y[4]$.

The SFG of the factorized stages for $\overline{\mathbf{W}}_8$ is shown in Fig. 8.5 (same conventions used as in Fig. 7.3). This network only requires 224 APF blocks, whereas

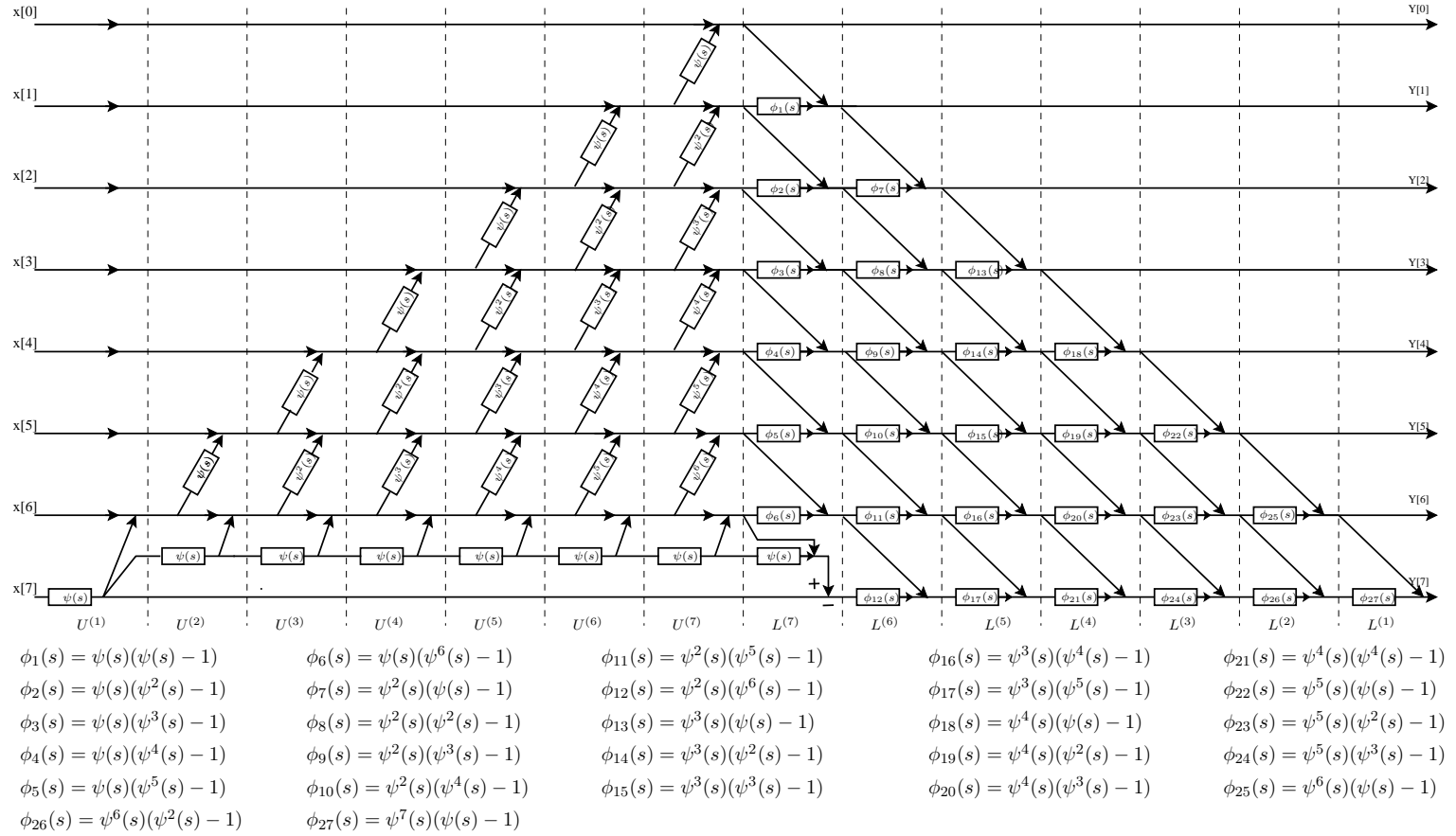


Figure 8.5: SFG for the proposed low-complexity 8-beam wideband beamformer.

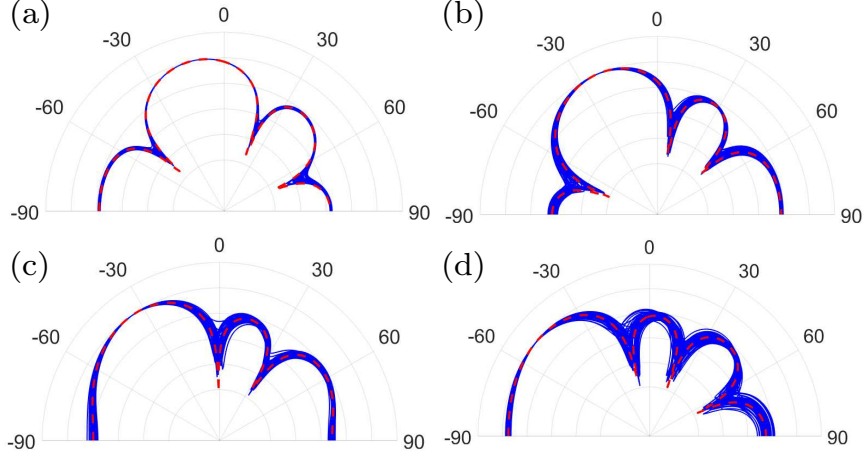


Figure 8.6: Monte-Carlo simulations for each beam of the $N = 4$ network (50 runs). The red curve represents the beam pattern for the nominal value of APF gain (unity).

a direct 8-beam network would require 1008 blocks. As for the $N = 4$ case, t_d of the APF was selected such that all 8-beams are within 50° from array broadside; this required $t_d \approx 1.6$ ps. The tuned APF circuit as simulated in Cadence had an average group delay of 1.606 ps which ideally should generate beams at 5.5° , 11.1° , 16.7° , 22.6° , 28.7° , 35.2° , 42.2° , and 50.2° . The simulated gain and phase values of the APF tuned to $t_d = 1.60$ ps are shown in Fig. 8.3 (b) and (c) respectively. The same procedure as described for $N = 4$ was followed. Fig. 8.10 shows the simulated results for beams 2, 4, 6, and 8 in two cases: Figs. 8.10 (a) and (b) show 2-D frequency magnitudes and array factors (AFs) using ideal delays, while Figs. 8.10 (c) and (d) show similar plots using simulated APF data. The two sets of simulated beams are in good agreement where the maximum beam deviation was $< 0.8^\circ$ with respect to the direction corresponding to the use of ideal delay. Note that while the algorithm provides N beams, the direct sum beam (look-direction to array broadside) only requires summing circuits. Also, beams pointing to $-\theta_k$ s can use an identical network with reversed antenna inputs.

8.3.3 Analysis of Variations in Beams due to Circuit Imperfections

Depending on the technology, all APF blocks that are used to construct the beam-forming network will not be identical due to PVT variations; in practice, gain mismatches of up to 10% are expected between them. A probabilistic approach was taken to analyze the impact of such mismatch on the final beam outputs. The gain variation of the APF blocks was assumed to be distributed uniformly between unity and the maximum error margin. Monte-Carlo simulations were conducted using these randomly-distributed gains to see how the beam shapes were affected. Fig. 8.6 shows that the simulated beam patterns of the 4-beam network are relatively robust to the assumed amount of mismatch.

8.4 Level-2 Digital Beamforming

The goal of the level-2 DBF is to generate narrow beams that maximize the link budget. The $N : M$ analog multiplexers after the ABF dynamically select the level-1 beam(s) fed into the DBF. Since the objective is to produce squint-free beams, delay-and-sum beamforming (that uses TTD) which is wideband in digital is required. Each m^{th} , $m \in [1, M]$ output beam from the L sub-array ABFs creates a spatially undersampled input to the DBF and thus, its array factor will contain grating lobes. The latter are removed by the ABF array factors, thus allowing the hybrid system to generate sharp output beams.

Different digital filter delay-and-sum structures are proposed in literature as discussed in Chapter 2. FIR fractional delay approximation filters are generally used for this [178]. For this work, the use of Thiran digital APFs is proposed

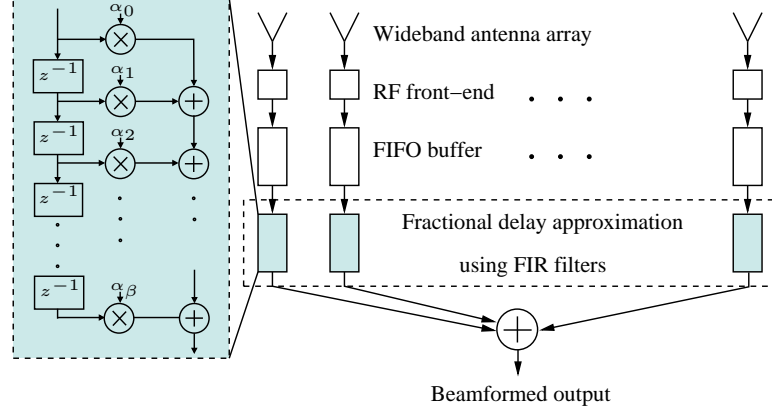


Figure 8.7: Wideband digital beamforming using FIR fractional delay approximation filters.

to approximate the required TTD and digitally beamform the signals (beams) from each analog sub array [179]. The Thiran APF is a IIR filter that can approximate the required TTD with a much lower hardware complexity than FIR filter counterparts. Ideally, M number of such digital filters would be needed to process each of the M beams sampled in to the digital.

Consider an $L \in \mathbb{Z}^+$ input digital TTD beamforming filter. In such filter, the signals at each filter input is needed to be delayed by T_l amount at the l^{th} , $l \in [1, L]$ input where,

$$T_l = \frac{(l-1)\Delta d \sin \psi}{c}, \quad (8.3)$$

and c is the wave speed, Δd is the physical distance between two adjacent elements and ψ is the angle of the beam formed. Filter and sum beamformers approximate the required true-time delay T_l using a high order FIR filter. Wideband delay and sum beamformers realize integer and fractional delays (compared to the sample period of the digital system) using separate sub systems. Delays which are multiples of the sampling period is obtained via clocked registers. Fractional delays are approximated via numerical methods implemented as digital FIR filters. Consider the system shown in Fig. 8.7, where each element is followed by a first-in first-out

(FIFO) memory and an FIR filter. The time delay T_l

$$T_l = i_l T_s + \tau_l, \quad (8.4)$$

where T_s is the sampling period, $i_l T_s$ is an integer multiple of the sample delay with $i_l \in \mathbb{Z}^+$. τ_l is a fractional delay where $0 \leq \tau_l \leq T_s$.

The accuracy of the fractional delay approximation (set by the FIR filter coefficients) determines the wideband performance of the beamformer [180]. Frequency response of the ideal fractional delay system with a delay of τ_l can be expressed as,

$$H_l(e^{j\omega}) = e^{-j\omega\tau_l}, \quad (8.5)$$

which has an unity magnitude response and a phase response of $-\omega\tau_l$. Corresponding impulse response can be approximated by,

$$h_l[n] = \text{sinc}(n - \tau_l/T_s). \quad (8.6)$$

Windowing methods, such as the Kaiser window and the Chebyshev window, can be employed to obtain the FIR filter coefficients [181,182]. The Lagrange interpolation method yields maximally flat approximation of the fractional delay for the FIR implementation [180]. In order to scan the environment by producing an electronically steerable RF beam, filter coefficients need to be changed accordingly. Such applications require tunable fractional delay filters, which may be realized using recomputation of coefficients, lookup tables and polynomial coefficient approximation (Farrow structure) [180,183].

8.4.1 Thiran APFs

Thiran filters are a special class of low-complexity IIR filters that have similar numerator and denominator coefficients, but in reverse order. They are the recursive

counterpart of the FIR Lagrange interpolation method, which provides maximally flat group delay at zero frequency [184]. Thiran fractional delay filters thus realize APFs with maximally flat group delay compared to other fractional delay implementation methods [180]. A significant gain in hardware complexity can be achieved without compromising accuracy by replacing FIR fractional delays with Thiran APFs [179]. Their transfer function is,

$$H_T(z_{ct}) = \frac{z_{ct}^{-\beta} Q(1/z_{ct})}{Q(z_{ct})}, \quad (8.7)$$

where $Q(z_{ct}) = \sum_{i=1}^{\beta} \alpha_i z_{ct}^{-i}$ and $z_{ct} = e^{-j\omega_{ct}}$ is the temporal \mathbf{z} domain variable, and β is the filter order. Thiran APF coefficients can be expressed in closed form as

$$\alpha_i = (-1)^i \binom{\beta}{i} \prod_{n=0}^{\beta} \frac{D - \beta + n}{D - \beta + i + n}; \quad i = 0, 1, \dots, \beta \quad (8.8)$$

which approximates the required delay D , where β is the filter order and $\binom{\beta}{i} = \frac{\beta!}{i!(\beta-i)!}$ are binomial coefficients. Also $\alpha_0 = 1$, and stability requires $D > \beta - 1$ [180, 184].

8.4.2 Digital Implementation of the Thiran Filter based Beamforming

The architecture of the proposed wideband beamformer is shown in Fig. 8.8. The 2D \mathbf{z} domain transfer function of the Thiran beamformer can be expressed as,

$$H(z_x, z_{ct}) = \sum_{l=0}^{L-1} H_T^l(z_{ct}) z_x^{-(L-l)} z_{ct}^{-i_l} \quad (8.9)$$

where L is the number of spatial input channels, z_x is the spatial \mathbf{z} domain variable and $H_T^l(z_{ct})$ is the Thiran filter transfer function at the l^{th} element, which realizes the required fractional delay τ_l (i.e., the actual delay in the system is $(\beta - 1)T_s + \tau_l$ where T_s is the sampling period of the digital system).

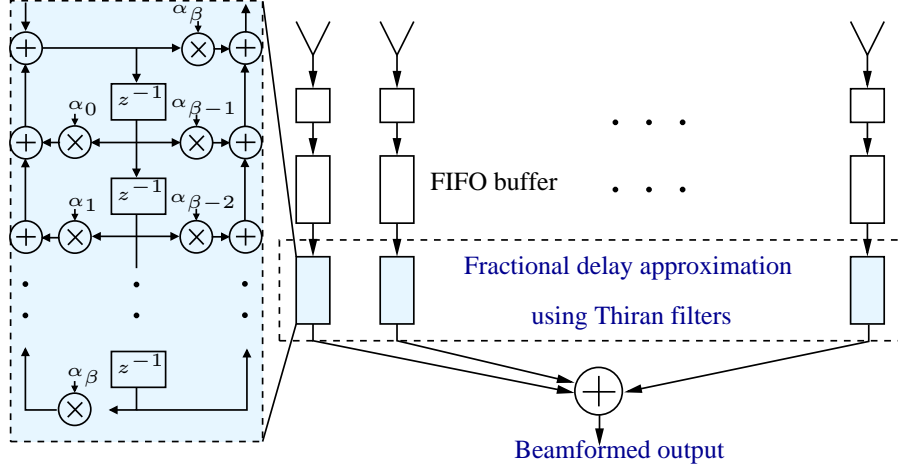


Figure 8.8: Proposed wideband delay-sum beamforming architecture using Thiran all-pass fractional delay filters.

The τ_l of each element is realized using a β order Thiran filter. Note that the Thiran filter provides additional integer number of sample delays D_i instead of the fractional delay τ_l which leads to a total delay of $D_l T_s + \tau_l$. Here, the integer delay $D_l \geq \beta - 1$ due to the stability condition and $D_l \in \{\beta - 1, \beta\}$. The Thiran filter provides better performance in terms of the flatness of the group delay when the necessary delay is less than the filter order (i.e. $D_l < \beta$) [180]. Thus, D_i is selected as $\beta - 1$ in the proposed beamformer, which leads to $(\beta - 1) T_s + \tau_l$ delay from the Thiran filter instead of the required fractional delay τ_l . Since all branches delay the same amount of $\beta - 1$ sample delays, this does not affect the required total delay T_l , other than the final delay at the l^{th} element becomes $(\beta - 1) T_s + T_l$. Required integer sample delay $i_l T_s$ is obtained similarly as the standard delay-sum beamformer by tapping off the correct delay position from the FIFO buffers.

To efficiently calculate the filter coefficients in real time, the relationship,

$$\alpha_i = \alpha_{i-1} \frac{(N - i)(N - i - \tau_k)}{(i + 1)(i + 1 + \tau_k)} \quad (8.10)$$

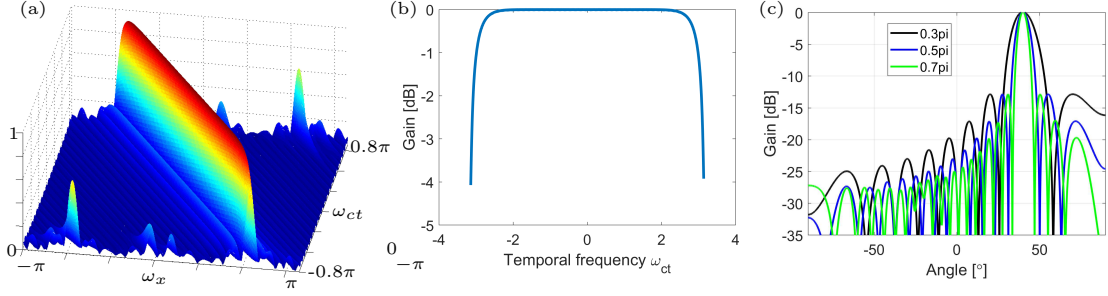


Figure 8.9: (a) 2D frequency response of the Thiran filter based 32-element beamformer where beam angle is set to 40° ; (b) magnitude response in (a) of the beamformers along the line shaped passband against the temporal frequency; (c) the array factors of the Thiran filter based simulated beamformer tuned at 40° at different temporal frequency values. .

can be used instead of the equation given in (8.8). By setting $z_x = e^{j\omega_x}$ and $z_{ct} = e^{j\omega_{ct}}$ in (8.9), the 2D space-time frequency domain transfer can be obtained as,

$$H_T(e^{j\omega_x}, e^{j\omega_{ct}}) = \sum_{k=0}^{N_x-1} H_T^k(e^{j\omega_{ct}}) e^{-j\omega_x(N_x-k)} e^{-j\omega_{ct}ik}. \quad (8.11)$$

Here, ω_x and ω_{ct} are the spatial and temporal domain frequencies, respectively. To illustrate the frequency response of a Thiran filter based beamformer the 2D frequency response of the $H_T(e^{j\omega_x}, e^{j\omega_{ct}})$ for $N_x = 32$ that is Nyquistly spaced and the where the beam direction is set to 40° is shown in Fig. 8.9(a). It can be seen that the passband of the beamformer is line-shaped oriented at θ angle to ω_{ct} axis where $\tan \theta = \sin \psi$ and ψ is the beamforming angle. Therefore, the Thiran beamformer represents wideband nature which does not suffer from beam squint. Fig. 8.9(b) shows the magnitude response of the beamformers along the line shaped passband and Fig. 8.9(c) shows the array factors of the Thiran filter based simulated beamformer for different temporal frequency values.

The TTD delay T_l in (8.3), for the m^{th} digital beamformer processing the m^{th} beam from the ABF stage can be calculated by setting $\delta d = N \times \Delta x$ and $\psi = \psi_m$

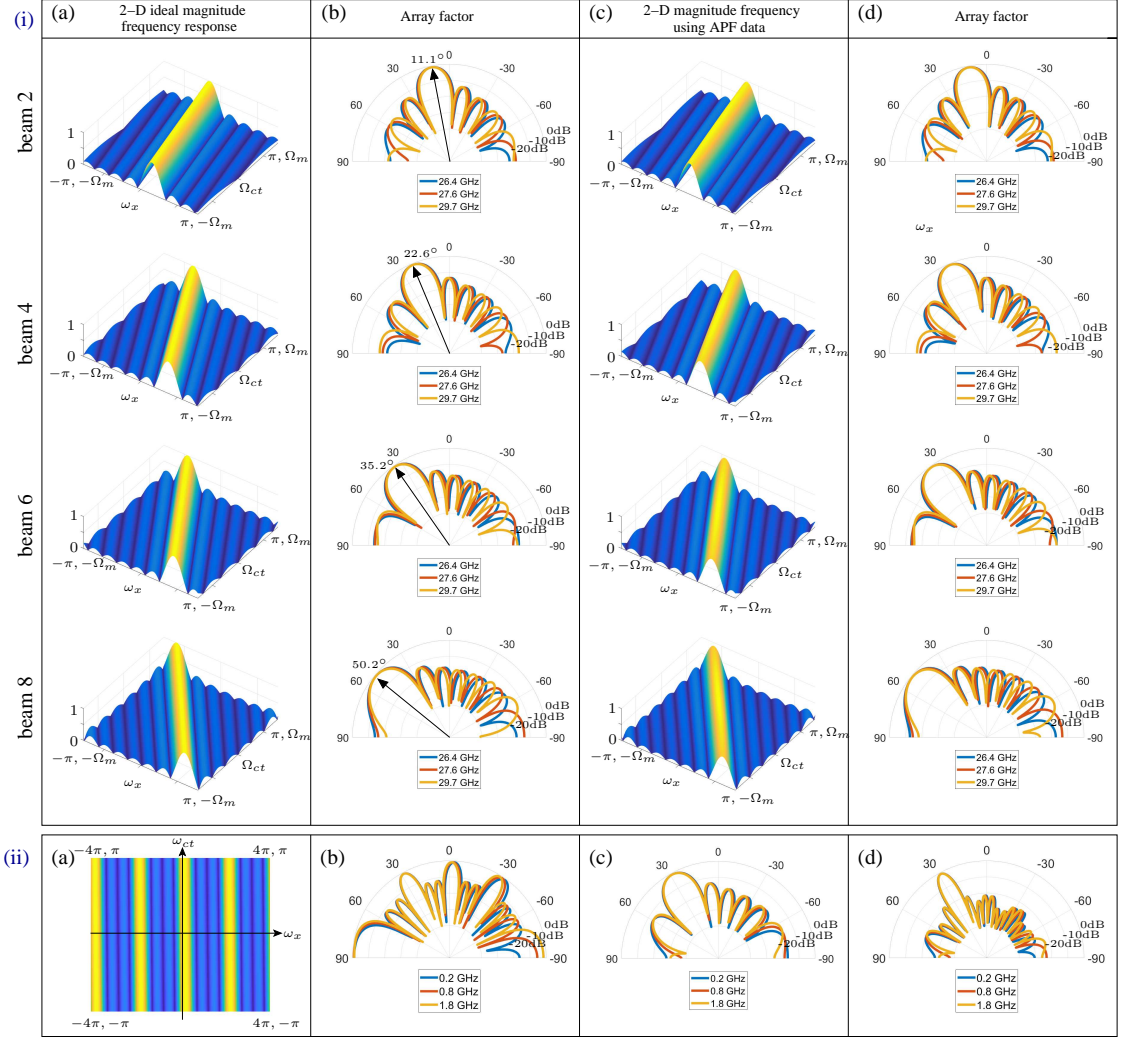


Figure 8.10: (i-a) 2-D magnitude frequency domain plots of $H_l(e^{j\omega_x}, \Omega_t)$ for $l = 2, 4, 6$, and 8 generated by the proposed 8-beam wideband beamformer assuming ideal time delays, and (i-b) the corresponding AFs. (i-c) and (i-d): Same as (i-a) and (i-b) but using simulated APF data. 2-D magnitudes (ii-a) 2-D magnitude frequency domain plot of the digital filter transfer function tuned to $\theta_5 = 28.7^\circ$; (ii-b) AF of the DBF in (ii-a) for different IF frequencies; (ii-c) AF of the 5th beam of the ABF; (ii-d) composite AF obtained by combining the ABF and DBF.

where N is the number of antenna elements in the sub array and ψ_m is the direction of the m^{th} beam from the array.

8.4.3 Analog Digital Hybrid Simulations

A 32-element ($P = 32$) system with four 8-element ABFs ($N = 8, L = 4$) is assumed for the simulation purpose. The effective DBF element spacing is $N \times \Delta x$, and its 2-D magnitude frequency response using a 3rd order Thiran filter (connected to the 5th ABF beam, which points at $\theta_5 = 28.7^\circ$) is shown in Fig. 8.10 (ii-a). Fig. 8.10 (ii-b) shows the DBF array factor for different IF frequencies. Fig. 8.10 (ii-c) shows the array factor of the 5th beam generated by the level-1 sub-array ABF, while Fig. 8.10 (ii-d) shows the resultant hybrid array factor, i.e., the combination of level-1 and level-2 beamformers.

8.5 Conclusion

A hybrid beamforming architecture is proposed for emerging 5G wireless communication systems requiring a variable number of sharp steerable mmW beams. The beam sharpness is proposed to be achieved in a power- and circuit-optimal way using the hybrid combination of both mmW-analog as well as digital beamforming via sub-arrays. The analog beamforming is proposed to use the DVM multibeam algorithm for obtaining squint-free RF beams. The analog sub-arrays support from 1 to N fixed TTD wideband mmW beams, depending on required capacity, which makes the architecture flexible for use in both mobiles and base stations. The analog beamforming is simulated using a Cadence APF model at 28 GHz. The gain and phase responses of the CMOS APF has been used to simulate the DVM SFG for both 4-element and 8-element sub-arrays and the the corresponding beam responses have been reported. The proposed hybrid beamformer contains several analog circuit components that are subject to on-chip PVT variations. The resulting delay and gain shifts in each receiver cause errors in the spatial orientation of the beams.

Calibration methods to compensate for such shifts include variable-gain amplifiers for gain, tunable APFs for delay, and reference input signals for training the algorithm. Development of such methods and associated circuitry are beyond the scope of this work.

Digital beamforming is proposed to achieve via low-complexity digital delay-and-sum beamformer based on Thiran IIR fractional delay filters. Thiran filters provide the same performance as FIR fractional delay filters in much lower multiplier complexity. The Thiran filter based beamforming strategy is analyzed. Finally, digital beamforming example is simulated along with the beam responses from the ABF stage.

CHAPTER 9

GENERATION OF N SIMULTANEOUS BEAMS AT $\mathcal{O}(N \log N)$ COMPLEXITY IN UNIFORM CIRCULAR ARRAYS

Most of the research on smart antennas, MIMO arrays have primarily concentrated on rectilinear arrays of either ULAs or URAs. The spectral properties of the planar waves that are captured by such arrays were discussed in detail in Chapter 2 and different beamforming algorithms and real-time implementations targeting ULAs/URAs were discussed in the previous chapters. Having mentioned that, only a little attention has been paid to circular array geometries despite their number of advantages. Arrays with circular geometry can be seen commonly in applications like Wi-Fi access-points [185] and radar front-ends [186, 187]. Although literature on single beam synthesis in UCAs exists, surprisingly, there is limited work available which discusses multibeam generation algorithms using circular array that does not involve $\mathcal{O}(pN)$ hardware complexity where N is the number of antenna elements in the array and p is the number of beams generated. Therefore, this chapter will investigate low hardware complexity methods of generating multiple simultaneous beams using UCAs. The simultaneous beams are preferable in most cases to be uniformly spaced in the angular domain, around the circumference of a circular array of elements, and be electronically adjustable in both the planes. The primary application of such uniformly spaced multibeam circular array processing systems is expected to be in ceiling mounted wireless network access points, 5G base-stations, and other location-based tracking systems that require a full 360 degree field of view. UCAs have a greater potential in being used by low-cost millimeter wave nodes as UCA geometries can provide the antenna gain while being able to electronically steer in the 3D space with much low complexity than URAs.

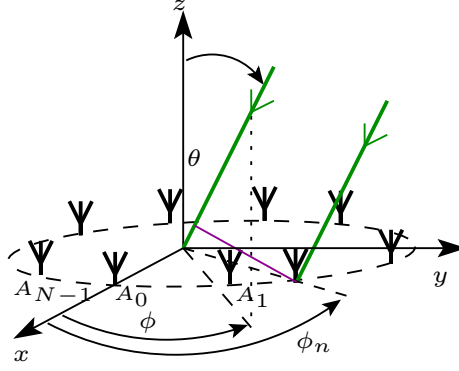


Figure 9.1: Circular array signal model.

9.1 Review of Array Factors of Circular Arrays

Circular arrays fall into the category of 1D linear arrays but in circular form. Unlike linear arrays, circular arrays can provide a 2D angular scan, both azimuthal (ϕ) and elevation (θ) angles. The ability of being able to scan horizontally in full 360° is a significant plus point of circular arrays over linear arrays with no distortions near the end-fire directions [188]. Also, distortions in the array pattern of a circular array due to mutual coupling effects are same for each element and this makes it easier to deal with the mutual coupling.

Consider a circular array of N -elements. Let the inter element angular separation of the elements be $2\pi/N$ and the radius of the circular array be a . The n^{th} element of the array is at $\phi = \phi_n$ where $0 \leq n < N$. Such setup is shown in Fig. 9.1. Let $\mathbf{x} = [x_0(t), x_1(t), \dots, x_{N-1}(t)]^\top$ be the representation of received (or transmitted) narrowband signal vector of the circular array either at RF ($x_n(t) \in \mathbb{R}$) or baseband ($x_n(t) \in \mathbb{C}$) where $x_n(t)$ is the signal at the n^{th} element. If \mathbf{w} as given in (9.1) denotes the complex weighting vector applied to output array signal vector \mathbf{x} ,

$$\mathbf{w} = [\alpha_0, \alpha_1, \dots, \alpha_{N-1}]^\top, \quad (9.1)$$

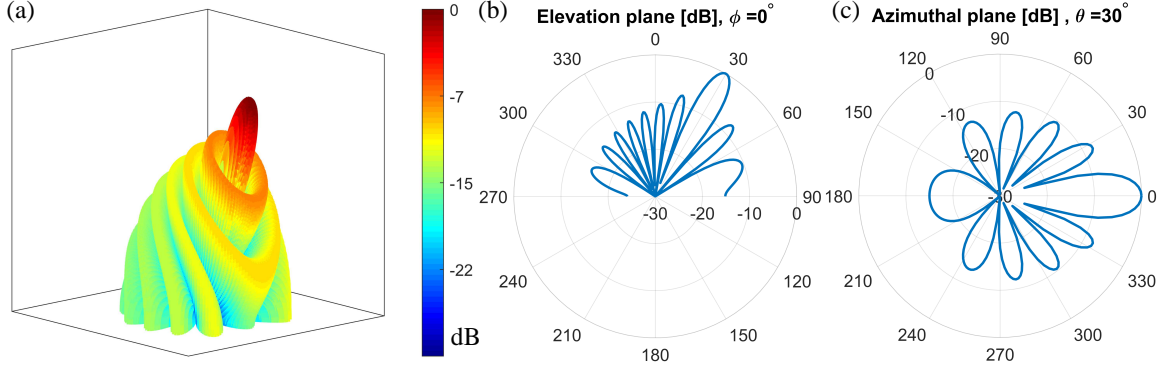


Figure 9.2: (a) 3D Beam pattern generated to point the beam at $\phi = 30^\circ$ and $\theta = 30^\circ$ by setting the array weights as given in (9.3). (b) Elevation plane pattern at $\phi = 30^\circ$; (c) azimuthal plane pattern at $\theta = 30^\circ$.

and $\alpha_n \in \mathbb{C}$ is the weight at the n th antenna output, then a beam output $y(t)$ is realized in the far-field by implementing the operation $y = \mathbf{w}^\top \mathbf{x}$. The array factor $A(\phi, \theta)$ generated from the array corresponding to the weights in \mathbf{w} (assuming omnidirectional antenna elements) is given by (9.2) [44],

$$A(\phi, \theta) = \sum_{n=1}^N e^{j[ka \sin \theta \cos(\phi - \phi_n) + \alpha_n]}. \quad (9.2)$$

The term k here is the wave number which is equal to $2\pi/\lambda$ where λ corresponds to frequency of operation. By observing (9.2) it can be seen that the maximum sensitivity/radiation direction $(\phi_{max}, \theta_{max})$ is achieved when (9.3) is satisfied.

$$\alpha_n = \pm 2m\pi - ka \sin \theta_{max} \cos \left(\phi_{max} - \frac{2\pi n}{N} \right), \quad m \in \mathbb{Z}. \quad (9.3)$$

One possible method to achieve maximum sensitivity at $(\phi_{max}, \theta_{max})$ direction is to compute α_n such that m is chosen to make $\alpha_n \in [0, 2\pi)$ [44]. Fig. 9.2 shows a numerically simulated array factor for a 32-element UCA in θ and ϕ planes where the desired maximum direction is set to $\phi_{max} = 0^\circ$ and $\theta_{max} = 30^\circ$.

9.2 Generation of N Beams using a UCA

As described, future wireless access points serving femto/pico cells in mmW and above frequencies will imperatively need shaper steerable beams and preferably multiple simultaneous beams uniformly spaced in the angular domain around the circumference while being able to electronically steer the beam in both elevation and azimuth planes. Following (2.25), producing N beams requires realizing N complex weighting vectors. As described in (2.25), this involves realizing the linear transform in (9.4),

$$\mathbf{y} = \mathbf{W}_N \mathbf{x}, \quad \text{where,} \quad (9.4)$$

$$\mathbf{W}_N = [\mathbf{w}_0, \mathbf{w}_1, \dots, \mathbf{w}_{N-1}]^\top \quad (9.5)$$

is an $N \times N$ matrix where each \mathbf{w}_i can be computed as given in (9.1) and (9.3). The vector \mathbf{y} here represents the beam outputs where $\mathbf{y} = [y_0(t), y_1(t), \dots, y_{N-1}(t)]^\top \in \mathbb{C}^{N \times 1}$.

For obtaining equally spaced symmetric beams in the ϕ direction (azimuthal plane), each i th row of the matrix \mathbf{W}_N becomes a circular shift of the $(i-1)$ th row, and thus \mathbf{W}_N takes the form of a circulant matrix [189] as given in (9.6).

$$\mathbf{W}_N = \begin{bmatrix} \alpha_0 & \alpha_1 & \dots & \alpha_{N-2} & \alpha_{N-1} \\ \alpha_{N-1} & \alpha_0 & \dots & \alpha_{N-3} & \alpha_{N-2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \alpha_1 & \alpha_2 & \dots & \alpha_{N-1} & \alpha_0 \end{bmatrix} \quad (9.6)$$

Direct realization of the \mathbf{W}_N in (9.6) consumes $\mathcal{O}(N^2)$ of hardware complexity. But the circulant matrices have a special property where they can be diagonalized by a DFT. This follows as a result of the eigen values of circulant matrices being

equal to Fourier modes. Although DFTs are also of $\mathcal{O}(N^2)$ complexity when computing in their raw form, the FFT algorithms drastically reduce this complexity to $\mathcal{O}(N \log N)$. This fact is explored in this chapter to propose a novel low-complexity circuit architecture for generating N circular symmetric simultaneous beams that are uniformly spaced in the azimuthal direction using an N -element UCA.

9.2.1 Proposed N -Beam Algorithm

Since \mathbf{W}_N of our interest is a circulant matrix, the expression in (9.4) can be written as a circular convolution given in (9.7)

$$\mathbf{y} = \mathbf{w} \star \mathbf{x}, \quad (9.7)$$

where \mathbf{w} is the first column of \mathbf{W}_N . The vectors \mathbf{w} , \mathbf{x} and \mathbf{y} are cyclically extended in each direction. Referring to the circular convolution theorem [189], the DFT can be used to transform the cyclic convolution into component-wise multiplication where,

$$\mathcal{F}_N(\mathbf{w} \star \mathbf{x}) = \mathcal{F}_N(\mathbf{w}) \circ \mathcal{F}_N(\mathbf{x}) = \mathcal{F}_N(\mathbf{y}), \quad (9.8)$$

in which the $\mathcal{F}_N(\cdot)$ denotes the N -point DFT operation and \circ denotes the Hadamard product. Thus, the N -beam output vector \mathbf{y} can be calculated as,

$$\mathbf{y} = \mathcal{F}_N^{-1}\{\mathcal{F}_N(\mathbf{w}) \circ \mathcal{F}_N(\mathbf{x})\} \quad (9.9)$$

In other words, this computation yields an orthogonal decomposition of \mathbf{W}_N such that,

$$\mathbf{W}_N = \mathbf{F}_N^{-1} \mathbf{D} \mathbf{F}_N, \quad (9.10)$$

where \mathbf{F}_N is the N -point DFT matrix, and \mathbf{D} is a diagonal matrix containing diagonal coefficients s.t. $\mathbf{D} = \text{diag}\{\mathcal{F}_N(\mathbf{w})\}$.

9.2.2 Complexity Analysis of the Proposed N -Beam Algorithm

The computation of the DFT via a vector-matrix product with \mathbf{F}_N using the FFT and the inverse DFT computation involving \mathbf{F}_N^{-1} via the inverse FFT transform, each has a computation complexity of $\mathcal{O}(N \log N)$. Therefore, counting the matrix multiplication with diagonal \mathbf{D} as N -multiplications, the entire algorithm has multiplication complexity $\mathcal{O}(N \log N)$. The complexity of the direct computation of \mathbf{W}_N would have been $\mathcal{O}(N^2)$. The use of the fast algorithms based on FFTs would therefore lead to a saving of the order of $\frac{N - \log N}{N}$. For $N = 8$, the brute-force computation leads to a multiplier count (real) of 192. On the other hand, since an 8-point CooleyTukey FFT involves a real multiplier count of 48 [81, p. 76], the total real multipliers needed for the proposed algorithm to produce 8-beams is 120. This is a 37.5% reduction of multiplier circuits needed. For a 16-element UCA, this saving climbs up to 60% (counting 128 real multipliers per 16-FFT [81, p. 76]) and the hardware saving becomes much more significant for larger array sizes (N). Following Table 9.1 summarizes the multiplier counts required for proposed algorithm based multibeam synthesis and the direct computation approaches for $N = 8, 16, 32$ cases.

Table 9.1: Multiplier counts required for proposed algorithm based multibeam synthesis and the direct computation approaches

N	Multipliers required– direct implementation	Multipliers required– proposed method	Saving
8	192	120 (48 per 8-point FFT [81, p. 76])	37.5%
16	768	304 (128 per 16-point FFT [81, p. 76])	60%
32	3072	960 (320 per 16-point FFT [81, p. 76])	69 %

9.3 Proposed Hardware Realization Architectures

The algorithm in (9.9) can be implemented in different approaches. Fig. 9.3 shows the overview architectures of analog and digital realization approaches of the algorithm.

9.3.1 RF Analog Architecture

The analog implementation as shown in Fig. 9.3(a) would require a analog Butler matrix [57] type implementation that implements the spatial DFT operation in analog as the first stage. The outputs of the Butler matrix then shall be phase rotated and gain adjusted depending on the γ_i complex constant where $\gamma_i = \mathcal{F}_N(\mathbf{w})[i]$. Since γ_i s vary depending on i , a variable gain amplifier in series with a variable phase shifter architecture can be used in an actual implementation. Alternatively, a variable group delay APF circuit architecture which has a programmability of the gain could be used for such implementation. Once the FFT outputs are scaled with γ_i coefficients, then a spatial IDFT operation has to be performed across the scaled output to produce the beam outputs. Since, Butler matrix is a passive reciprocal network, a Butler matrix network can be used in its so called “transmit” (or the reciprocal) mode to achieve this.

9.3.2 Digital Architecture

Fig. 9.3(b) shows the digital implementation architecture of the proposed algorithm. A conventional direct-conversion receiver architecture is shown in the figure to obtain N IQ baseband received signals from a UCA. The sampled N spatial IQ signals from the array are then subjected to a digital N -point FFT core and each output bin of

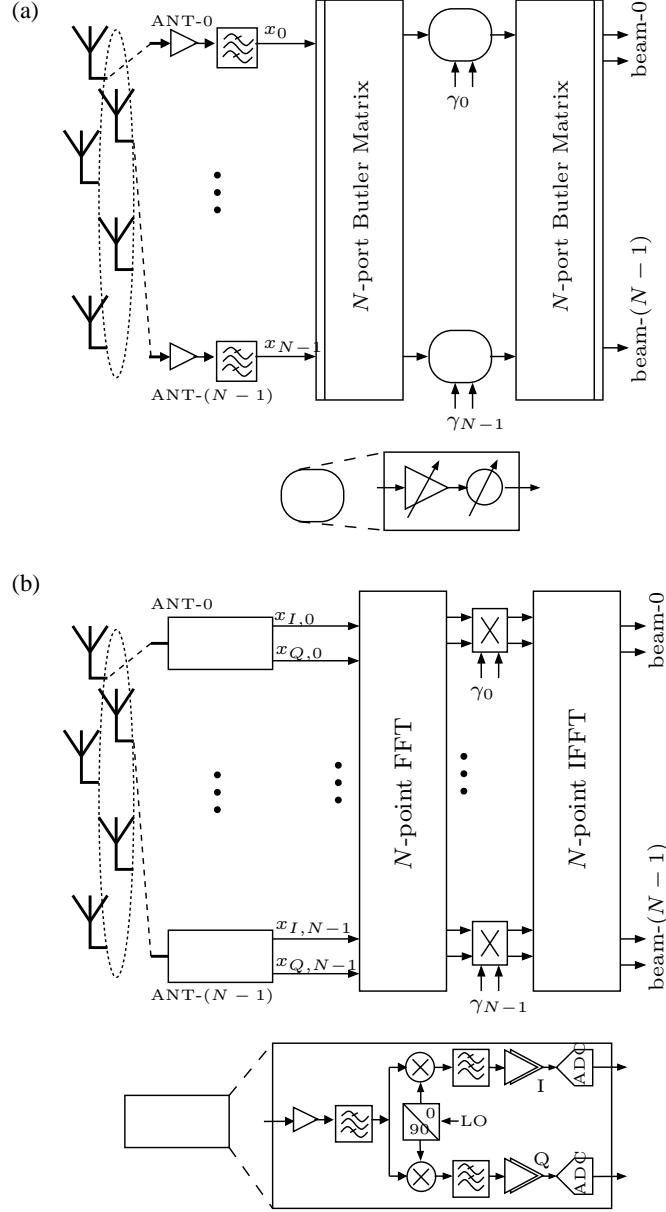


Figure 9.3: (a) Analog-RF architecture for realizing the proposed multibeam beam-forming system. (b) Digital baseband architecture for realizing the proposed algorithm.

the FFT is scaled by the set of complex constant γ_i ($0 \leq i < N - 1$) using a set of complex multipliers. Here, $\gamma_i = \mathcal{F}_N(\mathbf{w})[i]$. Each output frame is then subjected to an N -point IFFT operation to produce N simultaneous beam outputs that will be equi-spaced in the azimuthal plane. Let \mathbf{x} be the N -point input vector to the DFT

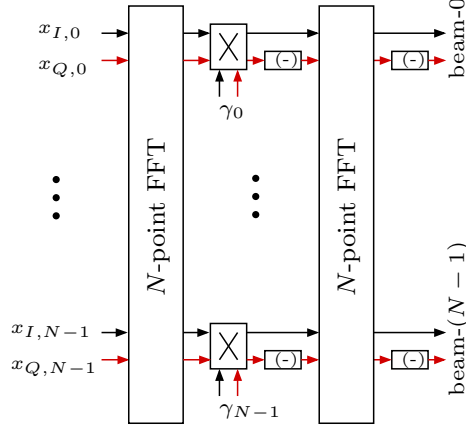


Figure 9.4: Digital circuits for realizing the N -beams using a UCA.

and \mathbf{y} be the output N -point vector. Since the DFT matrix \mathbf{F}_N is a unitary matrix (with the normalization by a factor of N), it obeys the following relationship,

$$\mathbf{F}_N \mathbf{F}_N^H = N \mathbf{I}_N, \quad (9.11)$$

$$\therefore \mathbf{F}_N^{-1} = \frac{\mathbf{F}_N^H}{N}. \quad (9.12)$$

Thus the IFFT operation $\mathbf{y} = \mathbf{F}_N^{-1} \cdot \mathbf{x}$ can be expressed as $\mathbf{y} = \frac{1}{N} \mathbf{F}_N^H \cdot \mathbf{x}$. The conjugation of the above relationship yields $\mathbf{y}^* = \mathbf{F}_N^T \cdot \mathbf{x}^*$ and since $\mathbf{F}_N^T = \mathbf{F}$ by the definition of the DFT matrix, $\mathbf{y}^* = \frac{\mathbf{F}_N}{N} \cdot \mathbf{x}^*$. This shows that the FFT core can be used to perform the IFFT by changing the input vector to its complex conjugate and then performing the FFT operation on the modified input vector with the appropriate normalization by N to produce the complex conjugate of the actual anticipated IDFT output corresponding to the original input. The normalization required here is trivial operation in digital for N that are powers of two. This implies that the N -point IDFT operation can be performed using the N -point DFT operation and therefore the same digital FFT core that's used for obtaining the DFT can be configured to perform the IDFT computation. The overview of such digital architecture is shown in Fig. 9.4. The α_i coefficients shown in the diagram would be

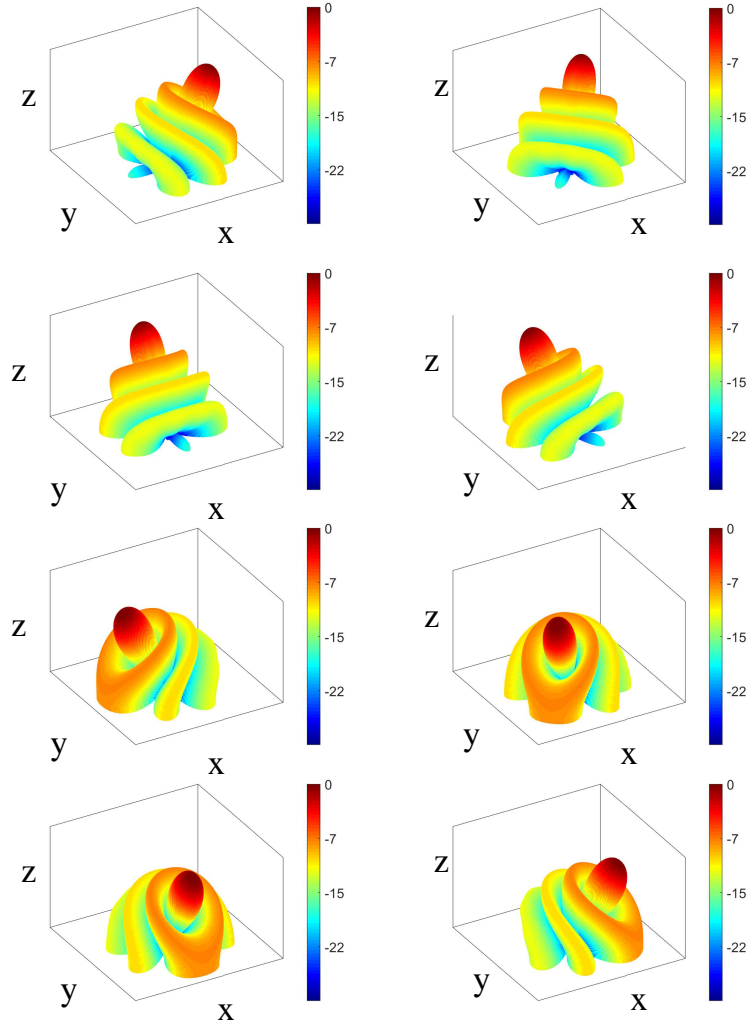


Figure 9.5: Simulated circular beams resulting from the proposed N -beam algorithm. Simulation assumes $N = 16$ and the beams are equally spaced at 22.5° in the azimuthal plane (only even indexed 8 beams are shown here out of 16).

required in an actual hardware implementation to achieve narrowband calibration of receivers.

9.4 Simulated N -Beam Patterns

The proposed N -beam algorithm was simulated in Matlab assuming a 16-element UCA spaced at 0.5λ . The coefficient vector \mathbf{w} in (9.1) was calculated using

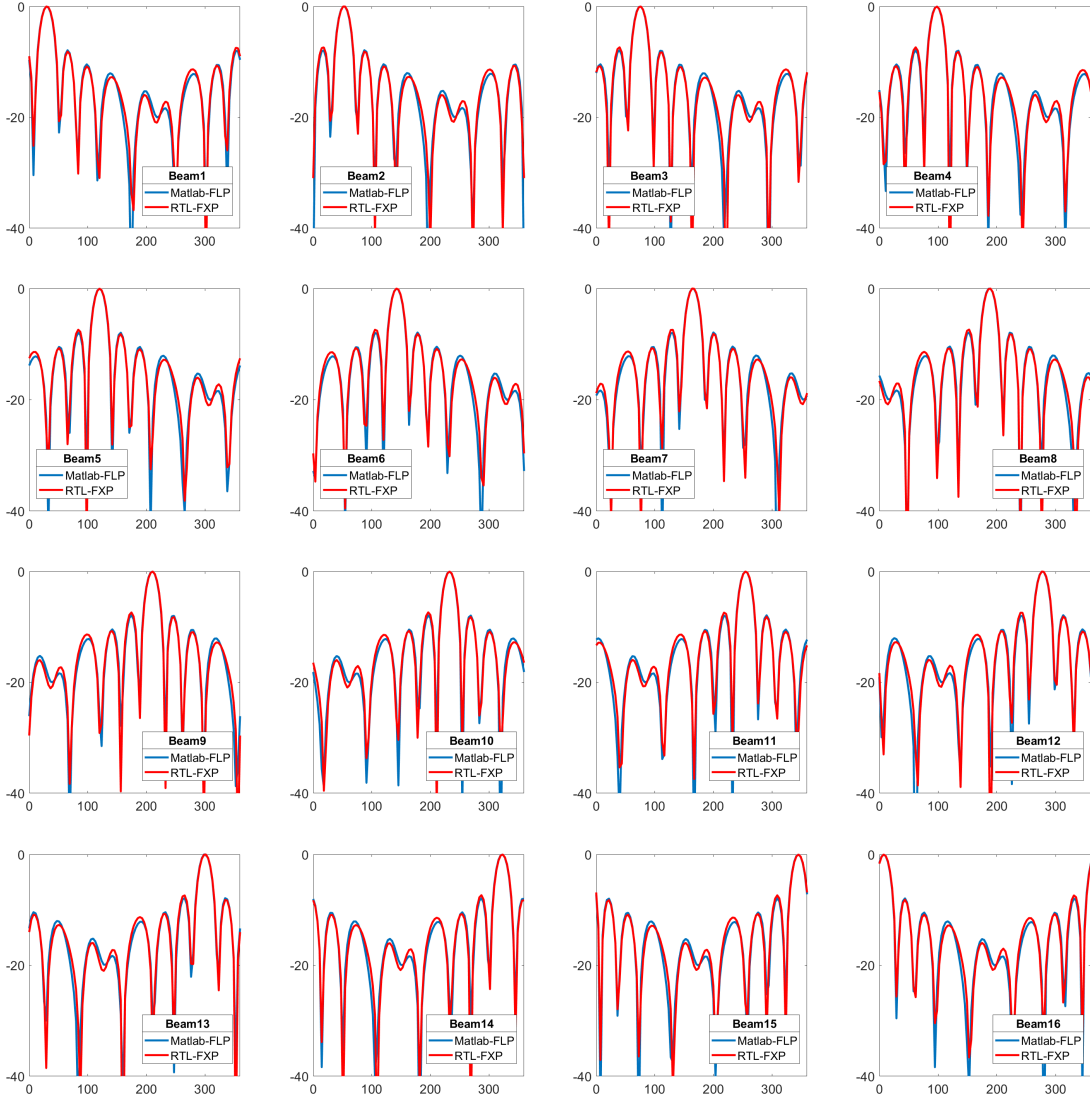


Figure 9.6: Comparison of array-factors corresponding to fixed-point digital core computed beams and Matlab floating-point simulated beams. The x -axis represents ϕ [°] and y -axis correspond to the beamforming gain.

$\theta_{max} = 30^\circ$. The 3D beam plots in Fig. 9.5 show the even indexed 8-beams out of the 16 equi-spaced beams spaced at 22.5° in the azimuthal plane. The digital architecture in 9.4 was implemented using Xilinx System Generator tools targeting FPGA implementation. The design assumes 16-element UCA inputs. The input world length corresponding to the ADC resolution was assumed to be 8-bits. A

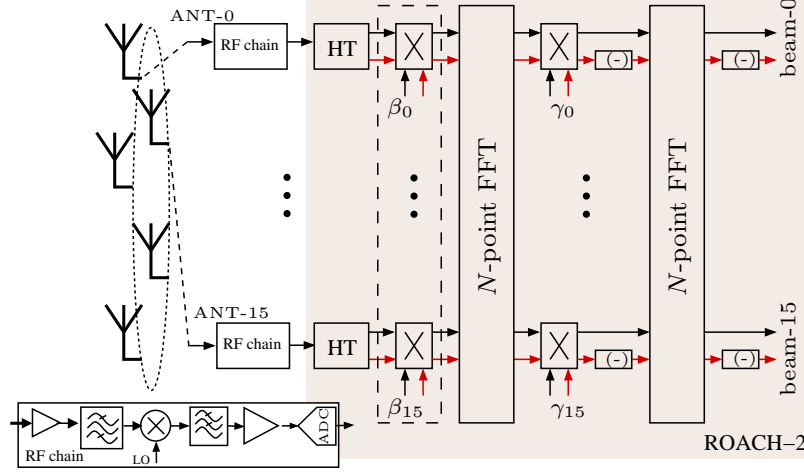


Figure 9.7: The overview of architecture of the 2.4 GHz digital circular array receiver.

parallel input 16-point spatial DFT core was also designed following the Radix-2 structure. The twiddle factors of the FFT was chosen to as 8-bits after different trials to achieve a trade-off between hardware resources and precision. A precision of 8-bits was also used to represent the diagonal multiplicands γ_i . The fixed-point digital core was then simulated by sending in Matlab generated inputs plane waves to compute the resulting array factors. Fig. 9.6 show the fixed-point core generated beam patterns with a comparison of the Matlab floating-point simulated beam patterns in the azimuthal plane (θ is fixed at 30°). Here the γ_i coefficients were selected by setting $\theta_{max} = 30^\circ$.

9.5 Real-Time Experimental Verification of the Proposed Algorithm

For the real-time experimental verification of the proposed algorithm, a 2.4 GHz 16-element receiver array was built. The overview architecture of the hardware that was designed is shown in Fig. 9.7.

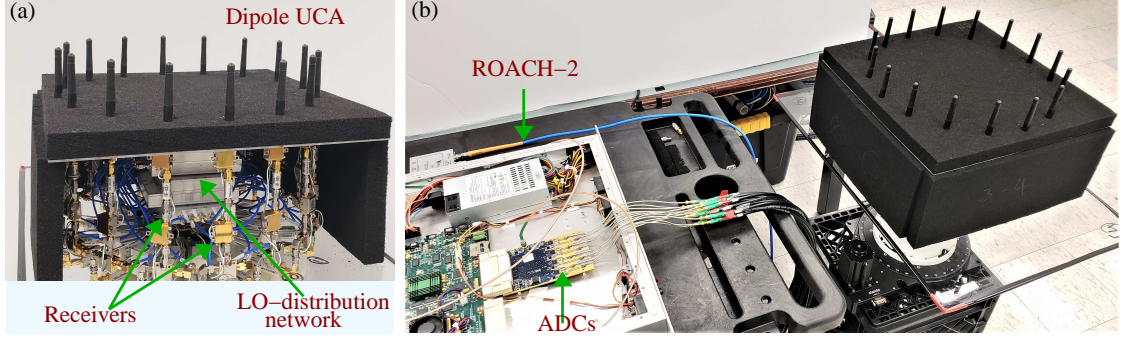


Figure 9.8: (a) The receiver array consisting of a 16-element 2.4 GHz dipole array and the receiver chains. (b) The array front-end and the ROACH-2 FPGA based digital back-end.

9.5.1 16-Element UCA

A 16-element UCA was built using commercially available dipole antennas. The specifications of the dipoles can be found here [190]. The antennas resonate in the range of 2.4 GHz to 2.5 GHz. The element power patterns shown in the data sheet in [190, p. 6] indicate that the element pattern is omni directional in the azimuthal plane as expected for a dipole. The radius a of the antenna array was set to 159 mm (the arc separation was 0.51λ where λ corresponds to 2.45 GHz). The antenna array built is shown in Fig. 9.8.

9.5.2 RF Receivers

The receivers were designed and built using the commercially available off-the-shelf components. A single mixer based receiver architecture was used as shown in Fig. 9.7. A centerlized LO based scheme was used to bring down the RF to IF. Shown in Table 9.2 are the model numbers of the components used for the design and their key-parameters. Two LNA stages were used in the design for improved gain performance of the receivers. An RF bandpass filtering stage was used to reject the out of band signals. The cascaded gain for the receiver was calculated to be 42

dB. The cascaded noise figure (NF) was 2.2 dB. It has to be noted that the receiver chains have not been optimally designed for noise performance and have been designed only to demonstrate the real-time synthesis of the circular multibeam using the proposed algorithm.

Table 9.2: Components used in the RF receiver chain (all components are from Mini-Circuits [191])

Component	Model number	Gain (dB)	NF (dB)	OIP3 (dBm)
LNA	ZX60-P105LN+	15	2.0	33
RF BPF	VBF-2435+	-1.6	≈ 1.6	NA
Mixer	ZX05-83LH-S+	-6	≈ 6	4
LPF	SLP-550+	-0.1	≈ 0.1	NA
IF amplifier	ZFL-1000LN+	20	3	14

9.5.3 Digital Back-End

The ROACH-2 FPGA platform that was introduced and used for the works in Chapters 3 and 4 has been used for implementing the digital back-end for this system. One ADC16x250-8 card [132] (which was also used for the work in Chapters 3 and 4) has been used to sample the 16-IF signals into the FPGA from the array. The overview architecture of the digital back-end is illustrated in Fig. 9.7. FIR filter-based Hilbert transform is employed in each sampled channel to perform the IQ decomposition. Next as shown in Fig. 9.7, the sampled low-IF signals are subjected to a narrowband gain phase calibration to equalize the gain and phase mismatches of the receiver chains. The $\beta_i \in \mathbb{C}$ where $i \in [0, 15]$ coefficients are precomputed by measuring the gain and phase deviation of each channel by sending a reference signal through receiver chains.

The rest of the digital design contains the multibeam computation circuit. The circuits have been designed to accept samples having 8 bits precision. The precision

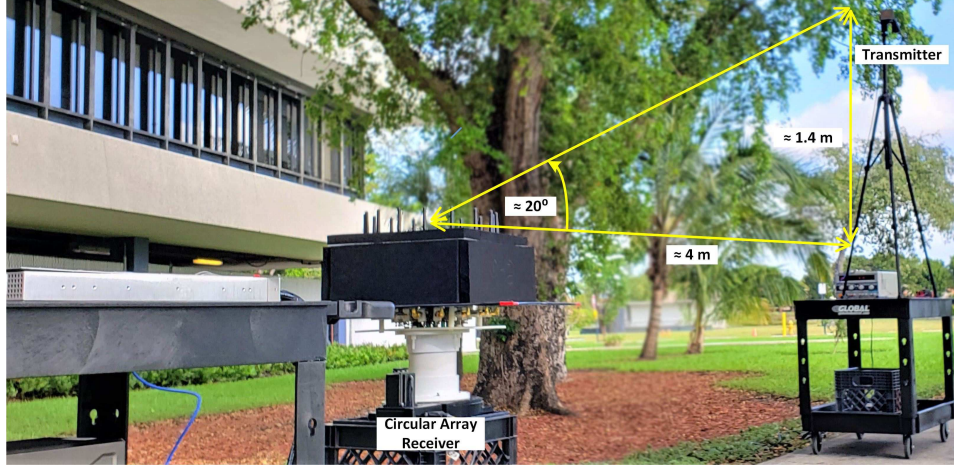


Figure 9.9: The outdoor measurement setup for experimental verification of the proposed circular multibeam algorithm.

of the twiddle factors and the γ_i coefficients have been set to 8 bits. At each beam output, a digital power calculation circuit similar to that of Fig. 3.10 was employed to aid in array factor measurement in the real-time experimental setup.

9.5.4 Measurement Setup

The setup was used to measure the actual digital RF receive-mode beams. The γ_i coefficients in the digital design was set to achieve a maximum sensitivity at $\theta = 70^\circ$. Then, the setup was taken outside to an open space to measure the 16 receive-mode multibeam generated from the algorithm. A patch-antenna was used to send an 2.49 GHz carrier wave. The LO frequency of the receivers was set to 2.47 GHz. The digital circuits were clocked at 200 MHz. Fig. 9.9 shows the measurement conditions used for the real-time beam measurement experiment. As shown in Fig. 9.9, the transmitter was placed in the highest sensitivity direction approximately of the receive-mode beams in the elevation plane. The transmitter and the receiver separation was set to approximately 4 m. The real-time beam measurement was conducted by rotating the receiver-array in the entire azimuthal

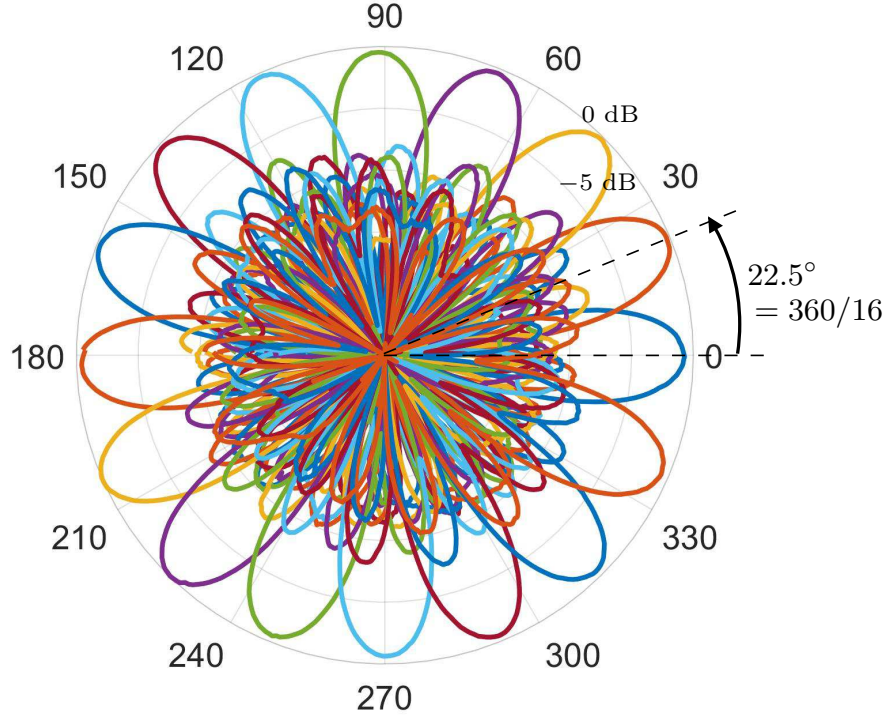


Figure 9.10: All 16 measured beams in single polar plot.

plane from $\phi = 0^\circ$ to $\phi = 360^\circ$. The received energy (for a fixed time window) at each beam for each different emulated direction of arrival was recorded for generating the measured array factors. Fig. 9.10 shows the measured 16 beam patterns in the polar domain. It can be seen that the beams are approximately spaced at 22.5° confirming equi-spaced 16 multibeam in the azimuthal plane. Figs. 9.11 and 9.12 show a beam by beam comparison of the measured beam patterns with the corresponding numerically simulated theoretical beam patterns. The measured plots indicate that the maximum deviation (upward) in the highest sidelobe level is below 1 dB. The maximum deviation of all array factor measurements with respect to the expected beam patterns were below 3 dB.

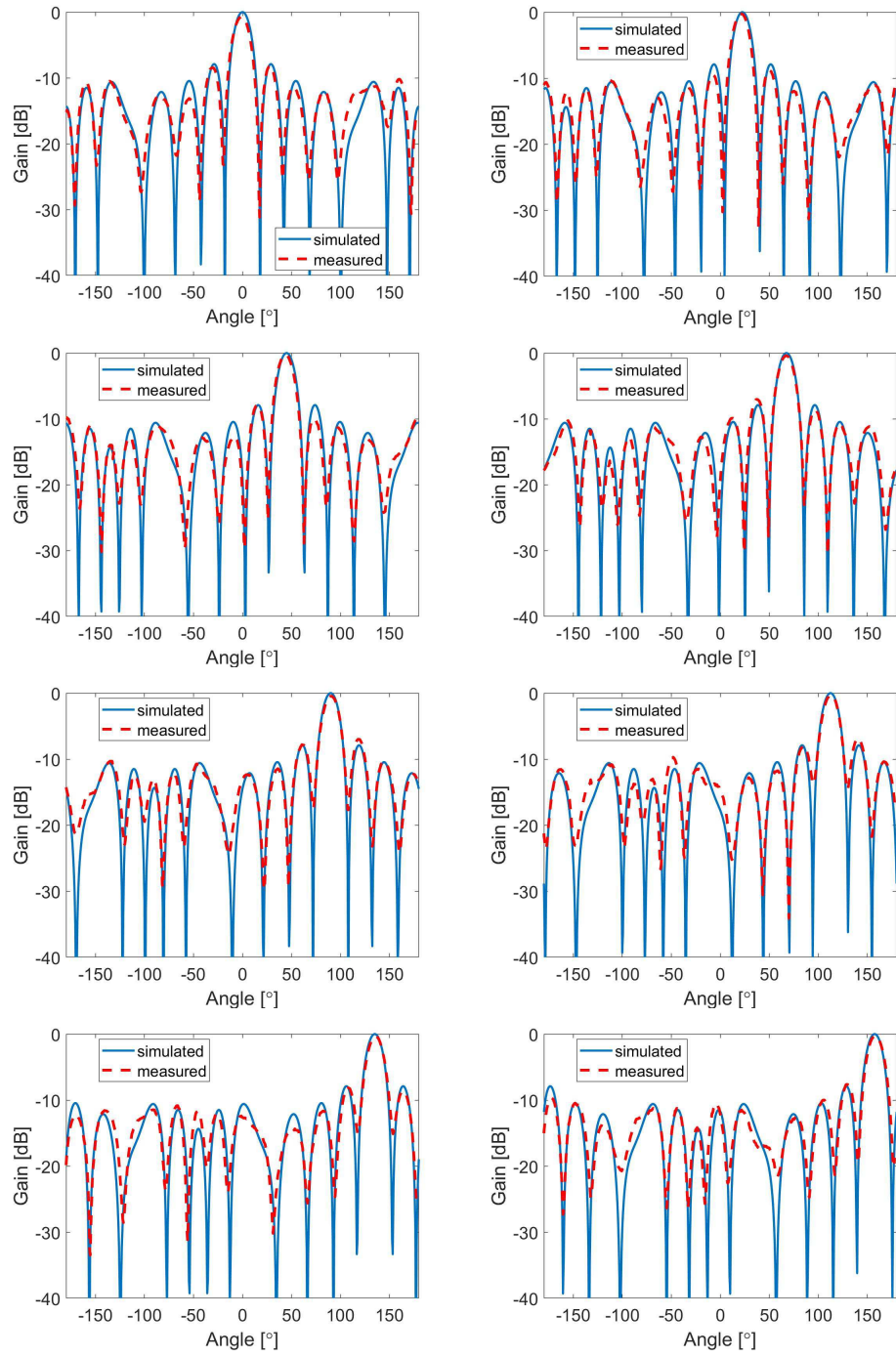


Figure 9.11: Comparison of measured and simulated beam patterns corresponding to beam 0 through beam 7.

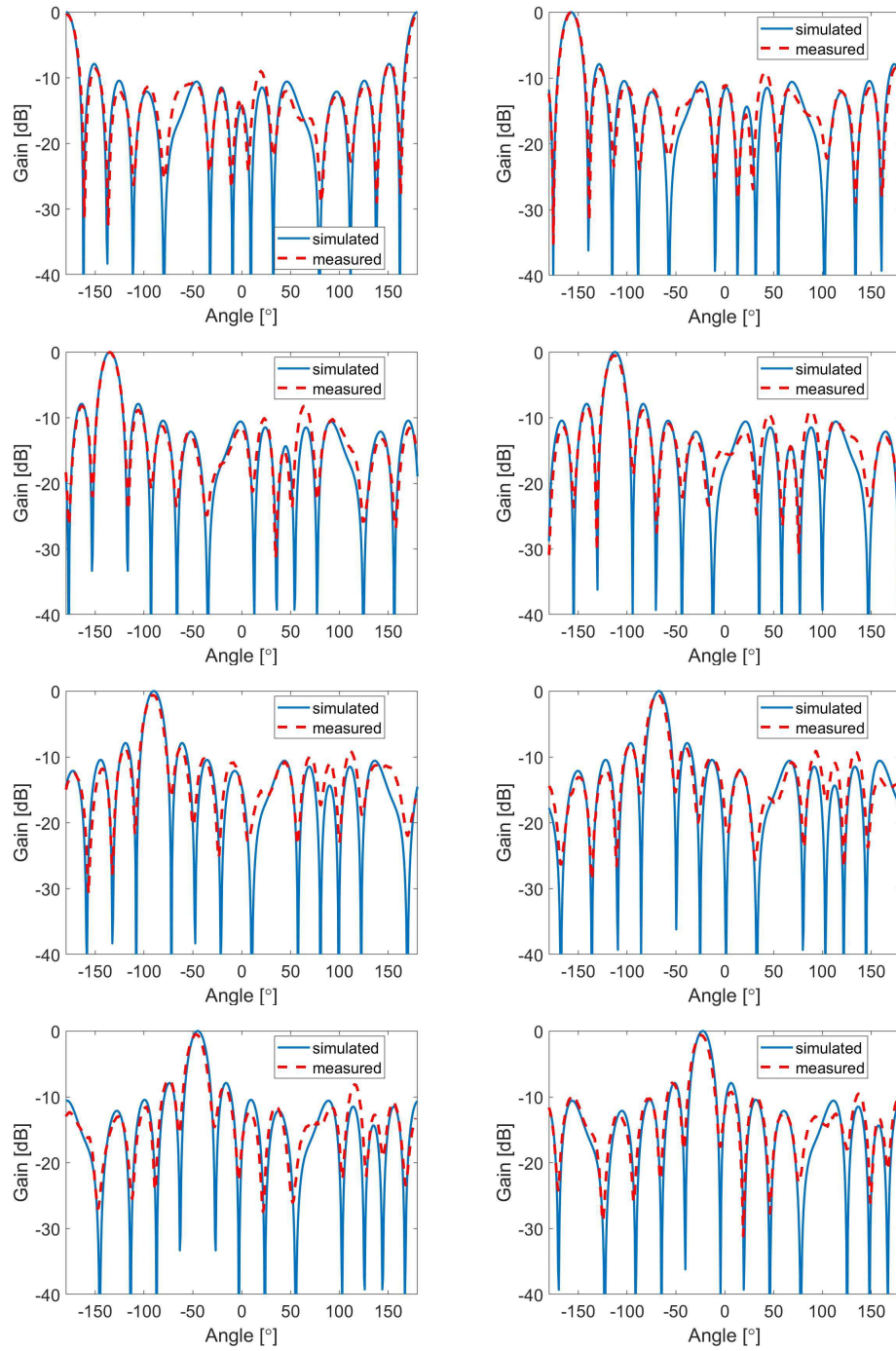


Figure 9.12: Comparison of measured and simulated beam patterns corresponding to beam 8 through beam 15.

9.6 Mitigating Mutual Coupling in UCAs for Multibeam Generation

MC between the antenna elements in an antenna array is unavoidable. The near-field coupling that takes place between the neighboring elements in the array show up as unintended distortions in the array captured signal vector [134]. The coupling between two antenna elements depends on the inter element distance, orientation and the element patterns of them. The coupling between antenna elements reduces with the distance between antenna and therefore MC is significant only in the few nearest neighbors of the array.

Different approaches for modeling MC in ULA can be abundantly found in literature [134, 192, 193]. According to [192], the effect of the MC in a N -element ULA is generally expressed as a linear transform which is termed as a coupling matrix $\mathbf{K}_c \in \mathbb{C}^{N \times N}$. Such transform models the outputs of a particular antenna element as a linear combination of its output and others. The same concept is applicable to UCAs as well and if \mathbf{x} denotes the ideal antenna sampled output from the ULA, due to mutual coupling what is actually observed is a different vector $\bar{\mathbf{x}} \in \mathbb{C}^{N \times 1}$ where,

$$\bar{\mathbf{x}} = \mathbf{K}_c \mathbf{x}. \quad (9.13)$$

The coupling matrix \mathbf{K}_c here in this model will capture the MC between the elements in the UCA. For uncoupling the MC, and remove that unintended distortions, the above transformation should be reversed and ideally, the computation $\therefore \mathbf{x} = \mathbf{K}_c^{-1} \bar{\mathbf{x}}$ should be performed. Having known \mathbf{K}_c apriory the above computation has a complexity of the order N^2 .

According to [44, 134, 194], the MC of a P -element sub-array from an N -element ULA where $\{P : P = 2p + 1, p \in \mathbb{Z}^+\}$ can be characterized by the linear trans-

form $\mathbf{K}_c^\dagger \in \mathbb{C}^{P \times P}$ by using the measured S-parameters of the P -element sub-array. Following [134, Sec. II-A], \mathbf{K}_c^\dagger of a P -element sub-array can be computed using,

$$\mathbf{K}_c^\dagger = \mathbf{Z}_A (\mathbf{Z}_M + \mathbf{Z}_A)^{-1}, \quad (9.14)$$

where $\mathbf{Z}_A = Z_A \mathbf{I}_N$, $\mathbf{Z}_M = (\mathbf{I}_N - \mathbf{S})^{-1} (\mathbf{I}_N + \mathbf{S}) \mathbf{Z}_0$, and $\mathbf{Z}_0 = Z_0 \mathbf{I}_N$. Here, \mathbf{S} is the measured S-parameter matrix and the \mathbf{I}_P denotes $P \times P$ identity matrix. Z_0 corresponds to the characteristic impedance of the transmission line connecting the antenna to LNA and Z_A is the LNA input impedance. This \mathbf{K}_c^\dagger matrix can then be used model the coupling matrix \mathbf{K}_c of the N -element array forming a P -diagonal Toeplitz matrix [134]. The same analogy can be applied to a circular array by obtaining the \mathbf{K}_c^\dagger matrix of P -adjacent elements (sub-array) of a UCA. Once the \mathbf{K}_c^\dagger is calculated using (9.14) the coupling matrix \mathbf{K}_c for the UCA can be formulated by (assuming identical antenna elements) having its i th row to be $T^{i-1} \mathbf{r}$ where,

$$\mathbf{r} = \begin{bmatrix} a & b_1 & b_2 & \dots & b_{\frac{P+1}{2}} & 0 & \dots & 0 & b_{\frac{P+1}{2}} & \dots & b_2 & b_1 \end{bmatrix}_{1 \times N}, \quad (9.15)$$

and $T^{i-1} \mathbf{r}$ is a shift operator defining a right handed circular shift of \mathbf{r} , $i - 1$ times. The diagonal coefficients $a \in \mathbb{C}$ of \mathbf{K}_c correspond to self-coupling and the off diagonal coefficients $b_k \in \mathbb{C}$, $k = 1, 2, \dots, \frac{P+1}{2}$ correspond to mutual coupling from the P neighboring elements.

It is noted that \mathbf{K}_c for UCA takes the special structure of a circulant matrix which also takes the form of in (9.16). Equation (9.16) shows the structure of the

coupling matrix for $P = 2$ scenario.

$$\mathbf{K}_c = \begin{bmatrix} a & b_1 & 0 & 0 & \dots & 0 & b_1 \\ b_1 & a & b_1 & 0 & \dots & 0 & 0 \\ 0 & b_1 & a & b_1 & \dots & 0 & 0 \\ 0 & 0 & b_1 & a & \dots & 0 & 0 \\ 0 & 0 & 0 & b_1 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \\ b_1 & 0 & 0 & 0 & \dots & b_1 & a \end{bmatrix}_{N \times N} \quad (9.16)$$

Since \mathbf{K}_c is circulant, exploiting the discussion in Section 9.2, \mathbf{K}_c can be expressed as,

$$\mathbf{K}_c = \mathbf{F}_N^{-1} \mathbf{D}_{MC} \mathbf{F}_N, \quad (9.17)$$

where $\mathbf{D}_{MC} \in \mathbb{C}^{N \times N}$ is a diagonal matrix given by $\mathbf{D}_{MC} = \text{diag}\{\mathcal{F}_N(\mathbf{v})\}$. The column vector \mathbf{v} here contains the first column of \mathbf{K}_c . Now therefore, the mutually uncoupled output vector from the array can be synthesized as,

$$\mathbf{x} = \mathbf{F}_N^{-1} \mathbf{D}_{MC}^{-1} \mathbf{F}_N \bar{\mathbf{x}}. \quad (9.18)$$

Interestingly, it can be seen that multibeam using the algorithm in Section 9.2 generated while removing the distortions of mutually coupling of the array at the same time by merging the two operations together without increasing the computational complexity. The above computation in (9.18) has the same complexity as of the N -beam algorithm in Section 9.2 and the original computation complexity in the order of $\mathcal{O}(N^2)$ can be brought down to order $\mathcal{O}(N \log N)$.

The circular multibeam beam network $\mathbf{y} = \mathbf{W}_N \mathbf{x}$ in Section 9.2 where \mathbf{W}_N is given in (9.6) assumed an ideal mutual coupling free output vector \mathbf{x} from the UCA. The equation (9.19) re-expresses the multibeam network using factorization

in (9.10).

$$\mathbf{y} = \mathbf{F}_N^{-1} \mathbf{D} \mathbf{F}_N \mathbf{x}. \quad (9.19)$$

From (9.18), the above expression in 9.19 can be re-written with respect to the mutually coupled array outputs $\bar{\mathbf{x}}$ as,

$$\mathbf{y} = \mathbf{F}_N^{-1} \mathbf{D} \mathbf{F}_N \mathbf{F}_N^{-1} \mathbf{D}_{MC}^{-1} \mathbf{F}_N \bar{\mathbf{x}}. \quad (9.20)$$

The above expression for the circular multibeam network can be simplified to the following form,

$$\mathbf{y} = \mathbf{F}_N^{-1} \bar{\mathbf{D}} \mathbf{F}_N \bar{\mathbf{x}}. \quad (9.21)$$

where $\mathbf{F}_N \mathbf{F}_N^{-1} = \mathbf{I}_N$ and $\bar{\mathbf{D}} = \mathbf{D} \mathbf{D}_{MC}^{-1}$ is a diagonal matrix. Therefore, mutual coupling effect in UCA multibeam generation can be eliminated without any hardware overhead in digital implementations by changing the weights γ_i appropriately in Fig. 9.4.

9.7 Conclusion

A novel algorithm that can produce multiple simultaneous beams uniformly spaced in the angular domain and that are also electronically adjustable in both azimuthal and elevation planes using UCAs is proposed in this chapter. The proposed approach achieves N simultaneous beams in $\mathcal{O}(N \log N)$ hardware complexity using an N -element array. The proposed approach have primary applications in ceiling mounted wireless network access points, 5G base-stations, and other location-based tracking systems that require a 360 degree field of view. A 2.4 GHz 16-element digital UCA receiver has been built using commercial off-the-shelf components to experimentally verify the circular multibeam using the proposed method. The measured beam

patterns resemble the expected theoretically simulated beam patterns quite well. The maximum deviation (upward) in the highest sidelobe level of the measured patterns are below 1 dB. The maximum deviation of all array factor measurements with respect to the expected beam patterns were noted to be below 3 dB.

In addition, a new method is proposed to get rid of the mutual coupling effect on the receive mode at a hardware complexity of $\mathcal{O}(N \log N)$. It is further shown how the mutual coupling uncoupling can be simultaneously achieved in the multibeam realization without any added complexity.

The beams that are generated through the weight realization approach in Section 9.1 gives higher side-lobe levels. This can be alleviated by using appropriate windowing techniques with the UCAs. Future work can be directed towards combining side-lobe reduction techniques with the proposed N -beam algorithm. Hardware verification of the proposed N -beam algorithm and the mutual coupling uncoupling method can be conducted as future work.

CHAPTER 10

CONCLUSIONS AND FUTURE WORK

Large-scale multibeam arrays will be a pressing requirement in future communication systems at mmW and higher frequencies to overcome the channel impairments. This dissertation is focused on algorithms, circuits and implementation verification of the proposed approaches towards reduced hardware complexity in multibeam arrays. Analog, digital, and hybrid approaches for reduced hardware complexity, power consumption of larger multibeam algorithms have been proposed for ULA and URA processing. A method to efficiently generate N multiple simultaneous beams using an N -element circular array configuration has also been investigated.

Fully digital beamforming is still not widely adopted due to the high hardware complexity and the associated computational cost. This dissertation proposes low-complexity N -beam digital beamforming algorithms based on the spatial DFT-based beamforming approach to generate similar beams with no multiplications involved in digital circuits. Such an approach leads to low-SWaPC digital VLSI implementations. Chapter 3 presents the work on low-complexity generation of 8 and 16 digital RF beams using a ULA with an analysis of their performance. The proposed 8- and 16-beam low-complexity beamforming algorithms that generate independent simultaneous beams have been digitally implemented and experimentally verified using a real-time 16-element phased array at 2.4 GHz with the baseband DSP performed using FPGAs. The beams realized using the proposed algorithms have been compared against the beams realized using fixed-point exact-DFT digital implementations. Chapter 4 proposes a 32-point ADFT algorithm for generating 32 simultaneous beams. The algorithm yields a multibeam processor with 46% less chip area and 55% less dynamic power consumption. The 32-beam algorithm has

been verified using a 32-element receiver array setup that was built at 5.8 GHz with the baseband DSP performed using FPGAs. The digitally measured beams perform same as the corresponding measured beams that are generated using fixed-point exact FFT circuits. Both the setup at 2.4 GHz and the setup at 5.8 GHz confirm that the hardware implementation imperfections such as front-end mismatches, phase incoherences, and phase noise of the local oscillator, make the system far from the ideal behavior which is impossible to achieve. Thus, there is sufficient room available to develop approximate algorithms, that can avoid high precision digital circuits that are optimized for reducing power and area costs to suit the performance of the RF front-end. Further, the complexity bounds associated in obtaining multiple simultaneous beams with URAs and the use of proposed ADFTs to achieve 2D beamforming in URAs without using digital multipliers in an ultra low-SWaP manner have been presented. The 32-beam linear array beam measurements at 5.8 GHz have been used to synthesize the corresponding 2D beams of a equivalent 2D array made of similar 32, 32-element subarrays.

The research described in this dissertation demonstrates, for the first time, fully digital multibeam beamforming across a full 800 MHz of bandwidth using a 28 GHz 4-element receiver array that has been custom built. The digital back-end uses Xilinx RFSoc to sample the full bandwidth into digital and to perform digital multibeam beamforming. The real-time measured beam responses have been given for different frequencies across the full processing baseband bandwidth.

The DFT approximations that were proposed for digital multibeam beamforming have also been proposed to design analog circuits that generate multibeams. The sparse factorization of the ADFTs that contain only small Gaussian integers have been used to realize beamforming circuits by employing analog CMOS current mirror-based implementations. Instead of realizing the small integer coeffi-

cient ADFT matrices directly, the proposed approach realizes N -beam beamforming network in analog using current mirrors in the order of the N . A schematic implementation of the 16-point ADFT algorithm that generates 16 high bandwidth analog beams was carried out in Cadence using 65 nm TSMC BSIM4 models. The simulated beam patterns of the current-mode circuit show that the analog CMOS schematic can handle high bandwidths up to 1.5 GHz without significant deviation in the expected beam patterns. The schematic-level analysis shows the worst-case and average sidelobe levels of -10.17 dB and -12.2 dB at a bandwidth of 1 GHz as well as -9.08 dB and -11.32 dB at a bandwidth of 1.5 GHz. The proposed multi-beam architectures have the potential to reduce circuit area and power requirements while meeting the bandwidth requirements of emerging 5G baseband systems.

A low-complexity DVM algorithm having sparse factors has been proposed for wideband squint-free beamforming. Arithmetic complexities of the proposed algorithm show that it is much more efficient than the direct computation of DVM-vector multiplication. The proposed algorithm is used to realize a squint-free wideband multi-beam beamforming architecture using mixed-signal CMOS integrated circuits. The architecture is useful for emerging 5G wireless communication systems requiring a variable number of sharp steerable beams. The proposed algorithm has been verified in simulations using CMOS APF circuit responses in the S-band and Ka-band. The analysis of the SFGs of the proposed algorithm for the 8-beam case uses only 24 APF blocks, whereas a similar 4-beam network using a direct TTD phased array would involve 60 such blocks; thus, the proposed approach achieves a 60% reduction in hardware complexity. The 8-beam network only requires 224 APF blocks, whereas a direct 8-beam network would require 1008 blocks owing to 77% reduction overall in terms of hardware required.

An analog-digital hybrid beamforming architecture is also proposed targeting mmW implementations via sub-arrays. The analog sub-arrays support from 1 to N fixed TTD wideband mmW beams, depending on the required capacity, which makes the architecture flexible to use in both mobile units and base stations. A novel low-complexity wideband digital beamforming method is proposed for the level-2 digital beamforming stage. Simulations verify that the similar array factor performance of a order 22 FIR implementation can be achieved by using a second-order Thiran filter based beamformer which approximately saves a 63.6% of multipliers (counting 11 multipliers for the 22nd-order FIR system due to the symmetry in the impulse response). Thus, the overall hybrid beamformer leads to ultra low-complexity implementations supporting wide bandwidth and squint-free operation. The proposed analog beamformer contains several analog circuit components that are subject to on-chip PVT variations. The resulting delay and gain shifts in each receiver cause errors in the spatial orientation of the beams. Calibration methods to compensate for such shifts include variable-gain amplifiers for gain, tunable APFs for delay, and reference input signals for training the algorithm. Development of such models, methods and associated circuitry can be studied as future work.

A new method that uses UCAs to produce multiple simultaneous beams that are uniformly spaced in the angular domain which are also electronically adjustable in both azimuthal and elevation planes has been proposed. The proposed approach can generate N simultaneous beams in $\mathcal{O}(N \log N)$ hardware complexity using an N -element arrays compared to $\mathcal{O}(N^2)$ complexity in direct synthesis approach. The proposed approach has promising applications in ceiling-mounted wireless network access points, 5G base-stations and other location-based tracking systems that require a full 360 degree field of view. A 2.4 GHz 16-element receive-mode digital UCA setup has been build to experimentally verify the proposed algorithm. Real-

time beam measurements are in well agreement with the expected theoretical beam patterns with only 1 dB of upward deviation in the sidelobe levels. In addition, a new method has been proposed to eliminate the mutual coupling in receive mode at a hardware complexity of $\mathcal{O}(N \log N)$. It is further shown how the mutual coupling uncoupling can be simultaneously achieved in the multibeam realization without any added complexity. The beams that are generated through the weight realization approach described in Section 9.1 gives higher side-lobe levels. This can be alleviated by using appropriate windowing techniques with the UCAs. Future work can be directed towards combining side-lobe reduction techniques with the proposed N -beam algorithm. Hardware verification of the proposed N -beam algorithm and the mutual coupling uncoupling method can be conducted as future work.

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