Low level rf system for the European Spallation Source's Bilbao linac

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(Received 26 May 2010; published 31 May 2011)

Design and some performance results of the pulsed digital low level radio frequency (LLRF) for the radio frequency quadrupole (RFQ) systems of Rutherford Appleton Laboratory–front end test stand and the future European Spallation Source Bilbao linac are presented. For rf field regulation, the design is based on direct rf-to-baseband conversion using an analog in-phase quadrature (IQ) demodulator, high-speed sampling of the I/Q components, baseband signal processing in a field-programmable gate array (FPGA), conversion to analog, and IQ modulation. This concept leads to a simple and versatile LLRF system which can be used for a large variety of rf frequencies and virtually any LLRF application including cw, ramping, and pulsed. In order to improve the accuracy of the probe voltage measurement, errors associated with the use of analog IQ demodulators have been identified and corrected by FPGA algorithms and proper setting of the feedback loop parameters. Furthermore, a baseband-equivalent model for the rf plant is developed in MATLAB-SIMULINK to study the RFQ transient response under beam loading in the presence of phase and delay errors. The effect of the unwanted resonant modes on the feedback loop stability and the LLRF considerations to avoid such instabilities are discussed and compared to some other machines such as the ILC and the European free electron laser . The practical results obtained from tests with a mock-up cavity and an RFQ cold model verify that amplitude and phase stabilities down to a fraction of one percent and one degree and phase margins larger than $\pm 50°$ can be achieved with this method preserving the linearity and bandwidth of the feedback loops.

DOI: 10.1103/PhysRevSTAB.14.052803 PACS numbers: 29.20.Ej

I. INTRODUCTION

The pulsed European Spallation Source (ESS)-Bilbao light-ions linac which is jointly funded by the Spanish and Basque governments and planned to be built in Leioa (Spain) will consist of two ion sources for light ions such as a Penning trap source for negatively charged H^- and a proton source based upon the electron cyclotron resonance (ECR) principle. The sources are meant to be able to generate beams of 60 mA for H^- and 100 mA for protons. Strong focusing into a four-vane radio frequency quadrupole (RFQ) at present under detailed engineering studies is then achieved by means of a four-solenoid low energy beam transport system, specifically designed to cater for multi-ion beams. Finally, a chopping device, still within conceptual design stages, will deliver beams into a drift tube linac (DTL) similar to the one from CERN linac-4 followed by two series of superconducting double-spoke and triple-spoke cavities driven by several 2.8 MW klystrons.

Applicationwise, the installation has been dimensioned to host a 40 MeV neutron converter, rotating solid target, where neutron production takes place as the result of direct reactions with light nuclei, and several proton extraction lines devoted to experiments on materials processing, radiobiology, or nuclear astrophysics.

The total linac length is estimated at 125 m and the commissioning of the normal-conducting part (until the end of the DTL) is foreseen for 2015. The linac will eventually be part of an accelerator research facility for fundamental and applied research using neutron and proton beams.

Table I summarizes the main parameters of the ESS-Bilbao (ESS-B) RFQ system which is being built in collaboration with Rutherford Appleton Laboratory (RAL)–UK.

Such an effort is geared to the design and construction of a state-of-the-art accelerating structure aiming to circumvent current tuning, spark generating, and mechanical problems found at present on structures of this kind in operation in high-power machines [1].

As part of this collaboration, a pulsed digital LLRF system has been designed and developed by the ESS-Bilbao rf group in collaboration with RAL to be used for the RAL front end test stand (FETS) and also the future ESS-Bilbao rf plant [2].

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TABLE I. Tentative list of the properties of the ESS-Bilbao RFQ system.

Parameter	Value	Unit
rf frequency	352.209	MHz
rf pulse rate (max)	50	Hz
rf pulse width (max)	1.5	ms
Peak klystron power	2.8	MW
Beam energy at the RFQ entrance	95	keV
Beam energy at the RFQ exit	3	MeV
Emittance	0.2π	mm mrad
Unloaded Q	9000	
Ratio of copper to beam power	5 to 1	
Amplitude stability	± 0.5	%
Phase stability	± 0.5	°
Settling time	≤ 100	μs

In order to improve the formation of the beam, avoid an additional beam chopper, and reduce operational costs, it is planned to pulse the ion source and the high-power rf system. As the beam pulse will be narrower than the rf pulse, the RFQ field should have settled before the beam pulse enters the RFQ so that the beam sees the right voltage and phase. That puts new requirements on the dynamic range, bandwidth, and transient response of the LLRF. The LLRF system should also provide a large phase margin to avoid loop instabilities in addition to being compact, modular, and easy to operate.

LLRF systems for linacs with similar applications have been built in the past at SNS and J-PARC. In the implementation of the SNS LLRF, a large effort has been made to keep the latency below 150 ns so that the required bandwidth can be achieved by an all-digital LLRF system. Also, mechanical modes of the superconducting cavities have been successfully damped out using adaptive feed-forward (AFF) compensation resulting in a significant decrease of the amplitude and phase errors [3]. In the case of J-PARC, a digital LLRF system utilizing feedback and feed-forward control has been made and tested with amplitude and phase stabilities of 0.3% and 0.2° under beam loading [4].

The LLRF system described herein consists of an analog front end for direct rf conversion to baseband IQ (and vice versa) and an field-programmable gate array (FPGA) unit running error compensation and control algorithms. LLRF systems based on the same or similar design principle have been developed for PEP-II B Factory [5], S-DALINAC-Darmstadt [6], and SCSS [7] and successfully put into operation, even for very high rf stability requirements of European free electron lasers (XFELs) [8]. As the accuracy of the probe voltage conversion to I/Q plays an important role in the rf stability, errors associated with the use of analog IQ demodulators have been identified and some FPGA algorithms have been proposed to compensate them thus meeting the rf stability requirements. Details of the LLRF design for amplitude/phase regulation and cavity tuning are given followed by a description of how the feedback loop parameters should be set to achieve the best performance. Also, a baseband-equivalent model in MATLAB-SIMULINK is presented to study the time-domain performance of the feedback loop under beam loading in the presence of phase and delay errors. These simulation results and the practical tests performed with a pill-box cavity and an RFQ cold model confirm the ability of the LLRF system to meet the requirements in addition to having a linear response, a configurable bandwidth, and an excellent phase margin for loop stability. Furthermore, the effect of the unwanted resonant modes of the ESS-B accelerating structures on the stability of the feedback loop is studied and the LLRF considerations to avoid such instabilities are described verifying that, due to the frequency separation of these modes, the klystron bandwidth, and the adopted control scheme, such instabilities are very unlikely.

II. RF CONVERSION TO DIGITAL I AND Q

When high rf stabilities are required, the accuracy of the probe voltage conversion to I and Q becomes of great importance as any errors acting on it will have a direct effect on the cavity field without being removed by the feedback loop.

Methods for rf conversion to digital I (in phase) and Q (quadrature phase) components in baseband can be generally classified in three categories: In the first category, the rf signal ($f = f_{\mathrm{rf}}$) is mixed with a reference signal with fixed amplitude and frequency ($f = f_{\mathrm{rf}} - f_{\mathrm{IF}}$) and low-pass filtered to suppress the upper sideband generated during the mixing process. The obtained signal ($f = f_{\mathrm{IF}}$) then conveys, within its bandwidth, the amplitude and phase information originally present on the rf signal. The principal reason for this down-conversion is to reduce the rf signal frequency so that it can be conveniently sampled and converted to digital. In the next stage, the IF signal is sampled by an analog-to-digital converter (ADC) running at $f = 4f_{\mathrm{IF}}$ (or a submultiple of it) generating a digital stream of I, Q, −I, −Q, …. This stream, after being demultiplexed and sign corrected, will finally result in two data streams being the I and Q components of the rf signal [9]. This method has been widely used in the past years and has become standard for digital LLRF. An extension of this method has been adopted at J-PARC where up to four different intermediate frequencies are mixed together and sampled by one ADC with the advantage of reducing the number of required ADC channels [10]. The main drawback of sampling in IF is the need for a precise and complex timing system generating the clock signals needed for down-conversion and ADC sampling. As these clocks must be in tight synchronization, they are usually generated using a phase locked loop or a digital data synthesis (DDS) adding to the total cost and complexity of the

LLRF system. A few limitations will be imposed on the clock signals generated in this way: The f_{IF} should be determined taking the sample rate of the ADC into account. As this is usually much smaller than the f_{rf}, it implies that the f_{rf} and $f_{\mathrm{rf}} - f_{\mathrm{IF}}$ should be relatively close making the generation of $f_{\mathrm{rf}} - f_{\mathrm{IF}}$ from f_{rf} more complex due to filtering issues. On the other hand, f_{IF} should be large enough so that the required LLRF bandwidth can be achieved. The other drawback of this method is that the generated clocks are not reconfigurable as changing any of the clock frequencies will probably imply modifying part of the hardware of the timing system.

The second category includes methods in which sampling is done directly on rf without down-conversion to IF. Direct sampling has been tested for the superconducting cavities of the International Linear Collider (ILC) with rf frequency of 1300 MHz, sampling frequency of 270.83 MHz, and stability requirements of 0.3% and 0.3° [11]. The I and Q signals are obtained by integrating the sampled values over several rf periods using a trigonometric function [12,13]. Although sampling in rf has advantages such as increasing the measurement bandwidth and eliminating errors caused by the rf-IF conversion, it still needs precise clock generation and careful choice of the sampling rate so that a reasonable compromise between latency and error can be made [12]. Moreover, such a scheme needs a very fast data acquisition system (both ADC and FPGA) with extremely low clock jitter.

Finally, the third category consists of methods in which sampling is done in baseband. This implies using an analog IQ demodulator for rf conversion to baseband and arbitrarily sampling the I/Q signals at a rate large enough to achieve the required bandwidth. Although sampling in baseband requires two ADC channels for each rf measurement (instead of one for sampling in IF/rf), it is advantageous because of its low latency and simplicity of the front end and its timing system. With this scheme, the only synchronized clock for down-conversion is either f_{rf} or $2f_{\mathrm{rf}}$ depending on the IQ demodulator type. This method has been used at LHC-CERN using a passive IQ demodulator (Merrimac IQG-20E-400) for the compensation of the transient beam loading (revolution frequency sidebands of the rf carrier) [14] and at J-PARC where a local analog loop has been used as a complement to the main digital loop to compensate ripples of the high voltage power supply (HVPS) supplying the klystron [15]. Nevertheless, an analog IQ demodulator, when not compensated, can suffer from some inherent errors such as noise, DC offsets, and amplitude/phase imbalance of the I and Q channels.

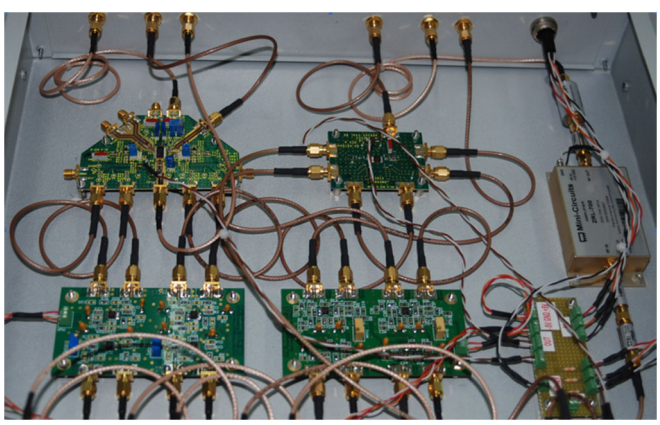

FIG. 1. Picture of the interior of the analog front end for rf-baseband and baseband-rf conversion; the upper left board is the IQ demodulator.

For the LLRF system of the future ESS-Bilbao RFQ, it has been decided to sample in baseband after simultaneous IQ demodulation and down-conversion due to the simplicity and versatility of this method (see Fig. 1). However, in order to make sure that the LLRF system will be able to meet the requirements, the IQ data has been further processed in an FPGA to compensate the errors mentioned earlier. The adopted algorithms for these error compensations give better results when applied to modern IQ demodulators which are normally available in the form of rf integrated circuits as they provide the user with less linearity errors and more flexibility in choosing the dynamic range, gain, bandwidth, etc. compared to the conventional IQ demodulators which are usually available as passive devices with relatively high insertion losses ([16,17] are examples of the first and second types, respectively).

III. ANALOG IQ DEMODULATOR ERRORS

A few effects usually contribute to the accuracy degradation of an analog IQ demodulator, being gain/phase imbalance between the I and Q channels, DC offsets, noise, and gain variations with temperature. Among these, the first two (gain and phase imbalances) are usually more severe as they are internal to the IQ demodulator while the later three can be compensated fully or partially using appropriate FPGA algorithms counteracting those effects. The datasheet of the AD8348 IQ demodulator which is used in the current design, for example, specifies maximum IQ gain and phase imbalances of ± 0.3 dB and $\pm 0.7°$, respectively [16], resulting in worst-case amplitude and phase errors equal to $\pm 1.75\%$ and $\pm 1°$ which would be unacceptable. In order to minimize the effect of these imbalances on the accuracy of the probe voltage measurement, the phase shifters in the feedback loop are adjusted so that in normal operation, when the cavity phase is desired, the phase of the IQ demodulator input is as close as possible to zero degree (or equivalently any multiple of 90 degrees) as explained in the following section. Then, the gain/phase imbalances will only have negligible effects on the transient response (i.e. before the signals settle) but the steady-state response will be immune to such imbalances improving the IQ demodulator linearity with respect to the input level. In the following, we will also briefly explain the algorithms which were adopted to minimize the effect

of the other types of errors mentioned earlier. Given that most of the signal processing of the LLRF system is done by an FPGA, these improvements are just a matter of adding some more lines to the FPGA code.

A. Gain and phase imbalances

Figure 2 shows a simplified block diagram of an analog IQ demodulator.

Here, A and θ are the gain and phase imbalance of the Q channel with respect to the I channel, respectively. If we represent the actual (i.e. the input) signal in baseband by $(I_{\mathrm{actl}}, Q_{\mathrm{actl}})$, the relation between the measured signal [i.e. $(I_{\mathrm{meas}}, Q_{\mathrm{meas}})$] to the actual one can be established as shown in Eqs. (1) and (2):

$$V_{\mathrm{actl}} = I_{\mathrm{actl}} \cos(\omega_{\mathrm{rf}} t) + Q_{\mathrm{actl}} \sin(\omega_{\mathrm{rf}} t) \tag{1}$$

$$\begin{aligned} V_{\mathrm{meas}} &= I_{\mathrm{meas}} \cos(\omega_{\mathrm{rf}} t) + Q_{\mathrm{meas}} \sin(\omega_{\mathrm{rf}} t) \\ &= I_{\mathrm{actl}} \cos(\omega_{\mathrm{rf}} t) + A Q_{\mathrm{actl}} \sin(\omega_{\mathrm{rf}} t + \theta), \end{aligned} \tag{2}$$

where V_{actl} is the actual rf input and V_{meas} is the rf equivalent of the measured input.

Equation (2) can be rewritten as the following showing how the measured signal is related in baseband to the actual one through the A and θ parameters:

$$\begin{aligned} V_{\mathrm{meas}} = {} & [I_{\mathrm{actl}} + A Q_{\mathrm{actl}} \sin(\theta)] \cos(\omega_{\mathrm{rf}} t) \\ & + A Q_{\mathrm{actl}} \cos(\theta) \sin(\omega_{\mathrm{rf}} t) \end{aligned} \tag{3}$$

$$I_{\mathrm{meas}} = I_{\mathrm{actl}} + A Q_{\mathrm{actl}} \sin(\theta) \qquad Q_{\mathrm{meas}} = A Q_{\mathrm{actl}} \cos(\theta). \tag{4}$$

$A = 1$ and $\theta = 0°$ would therefore be the necessary conditions for an error-free measurement resulting in $(I_{\mathrm{meas}}, Q_{\mathrm{meas}}) = (I_{\mathrm{actl}}, Q_{\mathrm{actl}})$.

The amplitude and phase of the measured signal $[|V_{\mathrm{meas}}|, \mathrm{ph}(V_{\mathrm{meas}})]$ can be calculated as the following:

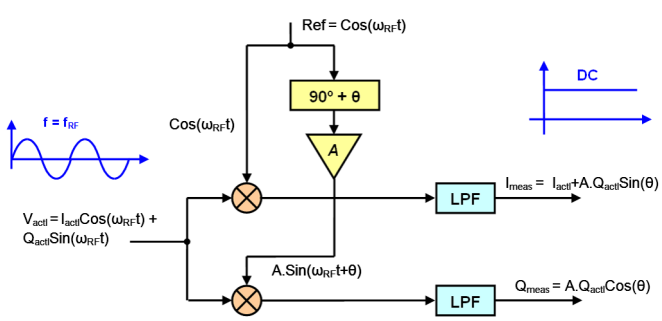

FIG. 2. Simplified block diagram of an analog IQ demodulator; A and θ represent gain and phase imbalances of the Q channel with respect to the I channel.

$$\begin{aligned} |V_{\mathrm{meas}}| &= \sqrt{[I_{\mathrm{actl}} + A Q_{\mathrm{actl}} \sin(\theta)]^2 + [A Q_{\mathrm{actl}} \cos(\theta)]^2} \\ \mathrm{ph}(V_{\mathrm{meas}}) &= \arctan \frac{A Q_{\mathrm{actl}} \cos(\theta)}{I_{\mathrm{actl}} + A Q_{\mathrm{actl}} \sin(\theta)}. \end{aligned} \tag{5}$$

At $\mathrm{ph}(V_{\mathrm{actl}}) = 45°$ (i.e. $I_{\mathrm{actl}} = Q_{\mathrm{actl}} = \frac{\sqrt{2}}{2}|V_{\mathrm{actl}}|$), this will result in

$$\mathrm{ph}\,(V_{\mathrm{actl}}) = 45° \Rightarrow |V_{\mathrm{meas}}| = |V_{\mathrm{actl}}| \sqrt{\frac{1}{2} + \frac{A^2}{2} + A \sin(\theta)}. \tag{6}$$

In order to measure the gain imbalance of the IQ demodulator, the phase of the rf input was once set to 0° and another time to 90° with the same amplitude. The gain imbalance A was calculated from the relative value of the two measurements (i.e. $\frac{|V90|}{|V0|}$). The results of these measurements are shown in Fig. 3 for several input levels.

The mean value (i.e. $A = 1.000\,65$) which is considered as the gain imbalance results in an error of 0.065% in the measured amplitude.

In order to measure the phase imbalance, while the amplitude of the input signal was constant, its phase was changed to sweep the complete 2π period and the amplitude of the measured signal was recorded. Having $A = 1.000\,65$, the phase imbalance was calculated at $\mathrm{ph}(V_{\mathrm{actl}}) = 45°$ using Eq. (6) resulting in $\theta = 0.293°$. Figure 4 shows the results of the amplitude measurements and compares them to the calculated ones obtained with these A and θ values.

As it can be seen in the Fig. 4, the measured amplitude makes two complete oscillations in one period of the input phase. The phases corresponding to the zero crossings (i.e. −90°, 0°, 90°, 180°) result in zero measurement errors

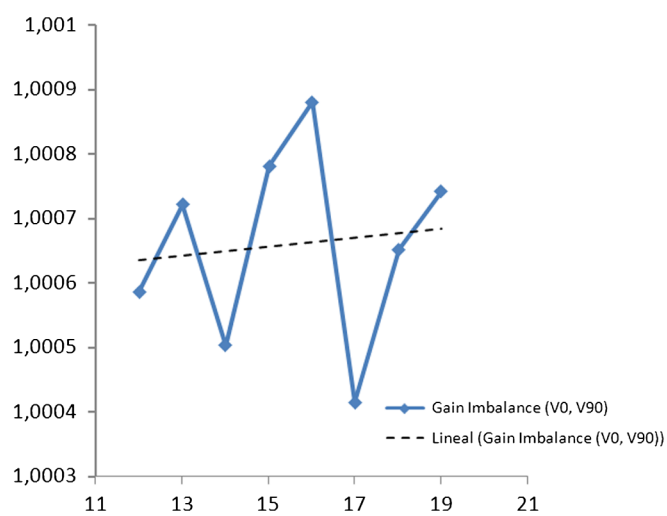

FIG. 3. Measured gain imbalance with several input levels; the horizontal axis is the input voltage in $\mathrm{mV_{RMS}}$ and the vertical one is the measured gain imbalance of the Q channel with respect to the I channel.

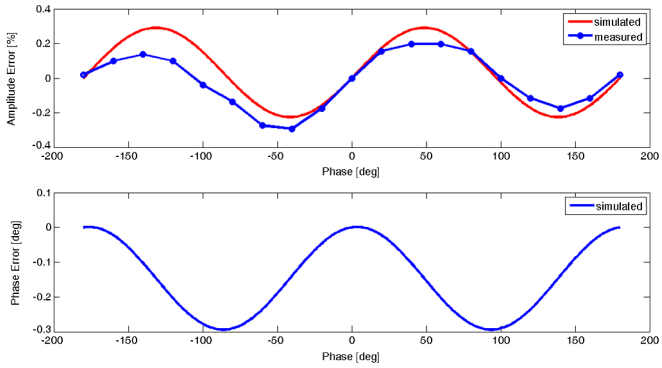

FIG. 4. Top: Comparison between the measured and calculated results of the amplitude error caused by the I/Q gain and phase imbalances, Bottom: Calculated results of the phase error caused by the same gain and phase imbalances.

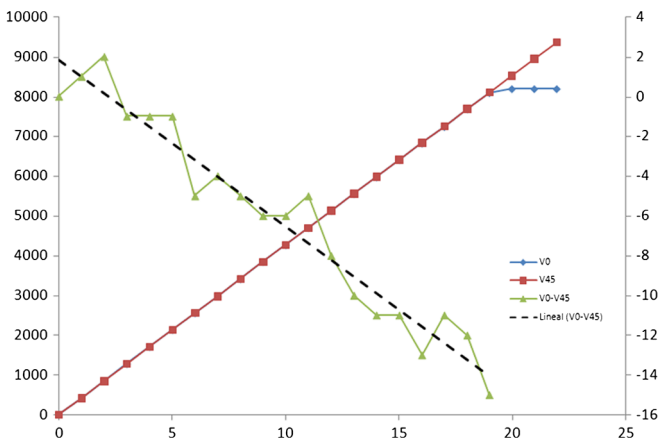

FIG. 5. Comparison between the IQ demodulator linearity with input phase set to 0° and 45°. The horizontal axis shows the input voltage in mV_{RMS}. The vertical axis on the left shows the ADC counts corresponding to the two measurements and the one on the right the difference between the two waveforms.

due to gain and phase imbalances because at these points the information is carried only by either I or the Q channel while the other channel is at zero volt. The relative gain/phase imbalance of the I/Q channels will therefore play no role in the accuracy of the measurements. Likewise, the −135°, −45°, 45°, and 135° points result in maximum measurement error as at these phases the information is equally shared between the I and Q channels.

Figure 5 shows the linearity response of the IQ demodulator with the input phase set to 0° (optimum) and 45° (worst case) and the input level covering all values from zero to the saturation level of the ADC. The maximum difference which occurs at the peak input level is 15 ADC counts corresponding to an amplitude error of 0.183% which is in agreement with the results shown earlier in Fig. 4.

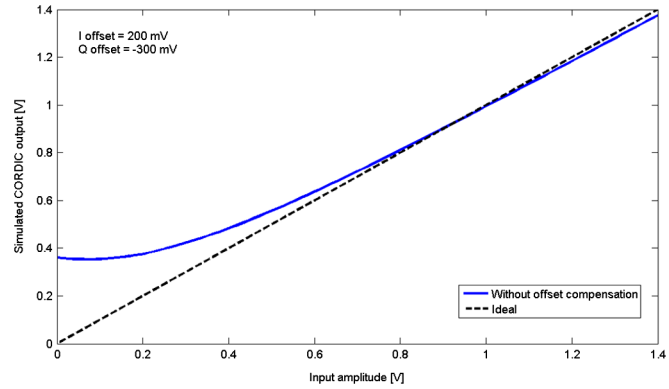

FIG. 6. Simulated linearity response of the IQ demodulator with I and Q offsets of 200 mV and −300 mV, respectively, and input phase of 45°.

B. DC offsets

DC offsets of the I and Q outputs can cause significant nonlinearities in the IQ demodulator response if not compensated. The DC offsets of the AD8348 can be as large as ±300 mV in a dynamic range of ±1400 mV. Figure 6 shows simulated linearity response of the IQ demodulator with I and Q offsets of 200 mV and −300 mV, respectively.

As the LLRF system operates in pulsed mode, the voltage that appears on the I/Q channel during the no-pulse period gives the exact value of the overall DC offset (i.e. sum of the IQ demodulator and ADC offsets) of the corresponding channel. These values are then saved in a buffer which is updated in each rf pulse and subtracted from the measured I and Q values to compensate for the DC offsets. As another option, the DC offsets can be manually adjusted using the LLRF graphical user interface (GUI) (Fig. 7). The maximum variation of the offsets during a period of 100 hours was recorded at five ADC counts corresponding to maximum error of 0.085% in amplitude.

C. Noise

The noise of the I and Q signals without shielding was measured at 10 mV_{pp} approximately in a dynamic range of ±1400 mV. This noise is then reduced significantly in several stages of the LLRF system such as the analog filters of the front end unit, averaging blocks in the FPGA and the integrator part of the proportional-integral (PI) regulator. The cavity noise in the end is dominated not by the IQ demodulator/modulator noise but the rf generator (rf reference) noise as it is shown in the practical results section. In order to protect the electronics against environmental noise, proper enclosures have been designed and built to be used for the final installation.

D. Gain variations with temperature

The AD8348 includes a variable gain amplifier whose gain is controlled by an external voltage [16]. Although

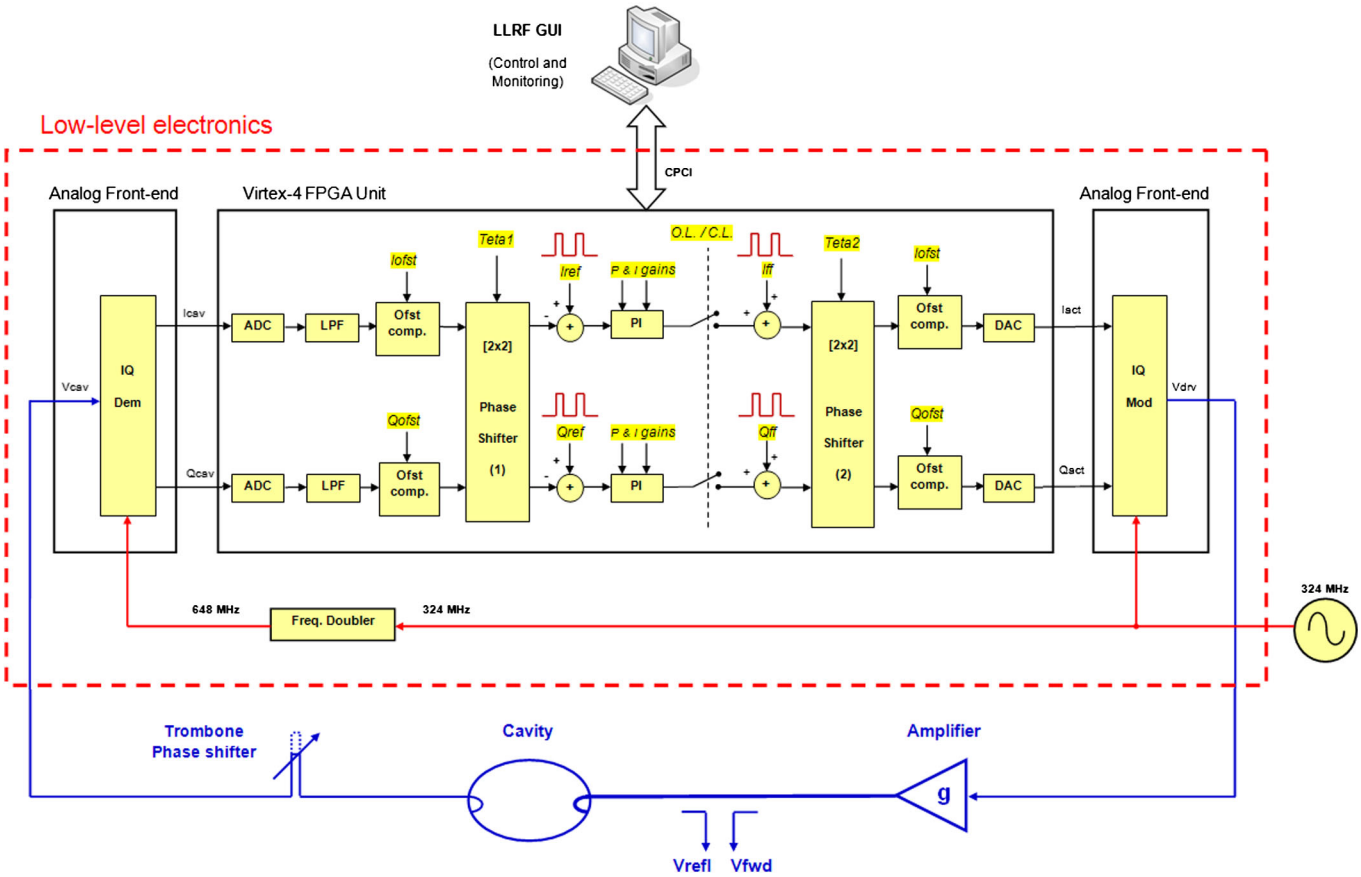

FIG. 7. Simplified block diagram of the FPGA program for amplitude and phase regulation; the parameters marked as *italic* are set from the control terminal.

care was taken to provide this voltage by a reliable source, it was observed that the gain still had some variations due to temperature fluctuations affecting the regulated cavity voltage (see Fig. 16). In order to minimize the gain variations, in the final system setup, it is planned to regulate the electronics temperature and/or fine-tune the demodulator gain based on the measured temperature to compensate these variations.

IV. LLRF DESIGN DESCRIPTION

A. Amplitude and phase loops

Figure 7 shows simplified schematics of the IQ loops for amplitude and phase regulation.

In this design, an analog IQ demodulator is used to convert the measured cavity voltage into baseband I and Q. The I and Q signals are in the next stage sampled by two 14-bit 104 MSPS ADCs and fed into a model-based Virtex-4 FPGA for the subsequent signal processing. In the first stage of the FPGA program, two averaging blocks acting on the last 30 samples are used to filter out the high frequency noise. The I/Q signals are then offset compensated (either manually or automatically) and fed into the first phase shifter. This is basically a rotation matrix acting on the rotation angle of the IQ vector by a user-controlled amount. Then, the I/Q signals are compared to their reference values (Iref and Qref inputs shown in Fig. 7) and the I and Q errors (i.e. the difference between the real and the reference I/Q) are fed into their corresponding PI regulators with controllable P and I gains from the LLRF GUI. At the output of the two regulators, a virtual switch is used to operate the system either in open-loop or closed-loop mode. For closed-loop operation, the switch is closed, therefore all the blocks are active and the cavity field is regulated by the two PIs. For open-loop operation, the switch is opened to break the feedback loop and the amplitude and phase are controlled by the feed-forward inputs (i.e. Iff and Qff) and a second phase shifter which gives the possibility to further rotate the IQ vector. This mode can be particularly useful for test purposes and for making sure that the regulation loops will be stable before they are actually closed. Moreover, by applying appropriate Iff and Qff in addition to the Iref and Qref inputs, one can further improve the step response or compensate for predictable errors such as the beam if needed. In this case the system is put into operation in closed-loop mode and the cavity I/Q is regulated by the feedback loops to be equal to the Iref/Qref. Then, the Iff/Qff inputs can be

used to improve the transient response without affecting the steady-state response. For instance, by applying appropriate feed-forward inputs at the beam arrival, the beam loading effect can be compensated before it is sensed and compensated by the feedback loops. At the output stage, the I and Q signals are converted to analog using two 14 bit digital-to-analog converters (DAC) with maximum sampling rate of 480 MSPS (interpolating). These signals then serve as the baseband inputs for the IQ modulator driving the preamplifier of the klystron.

For normal operation in closed-loop mode, the fractional part of the loop delay must be compensated to avoid loop instability. If, for example, the total loop delay from the LLRF output along the rf transmitter, the RFQ, and back to the LLRF is 512.3 times the rf period, the phase shifters should be adjusted so that the total phase shift they provide compensates 0.3 rf periods (i.e. $-108°$ of phase shift). Then, the total loop delay will be equivalent to 512 rf periods and the two PI controllers see the IQ vector with correct phase. If the phase shifters are not properly adjusted, the response of the I and Q loops will not be the same and some degradations in the transient response might be seen as well. In the extreme case, if the phase error exceeds the phase margin, the loops will become unstable.

The procedure for the adjustment of the phase shifters is as follows: First, the LLRF system is operated in open-loop mode and the Iff and Qff are set so that $\arctan(\frac{\mathrm{Qff}}{\mathrm{Iff}})$ corresponds to the desired cavity phase for beam acceleration. Then phase shifter (2) is adjusted so that the actual cavity phase is equal to the set value. In the next step, the trombone phase shifter is adjusted so that the read-back cavity phase at the input of phase shifter (1) becomes as close as possible to zero degree. Finally, phase shifter (1) is adjusted so that the phase at its output (i.e. the input for the two comparators) is the same as the one set by the feed-forward inputs. Having the three phase shifters so adjusted indicates the fractional part of the loop delay is correctly compensated, the phase corresponding to the I/Q set values is the same as the actual cavity phase, and the IQ demodulator works at zero input phase in steady-state conditions regardless of the voltage amplitude; a condition needed to minimize the effect of the gain and phase imbalance on the regulated cavity voltage as mentioned earlier. Assuming that the loop gain is not too high, the feedback loop can then be closed without loop instability risk. In closed-loop mode, the cavity can be driven only by the reference inputs or these inputs in combination with the feed-forward set values. In both cases, the two PI regulators guarantee that

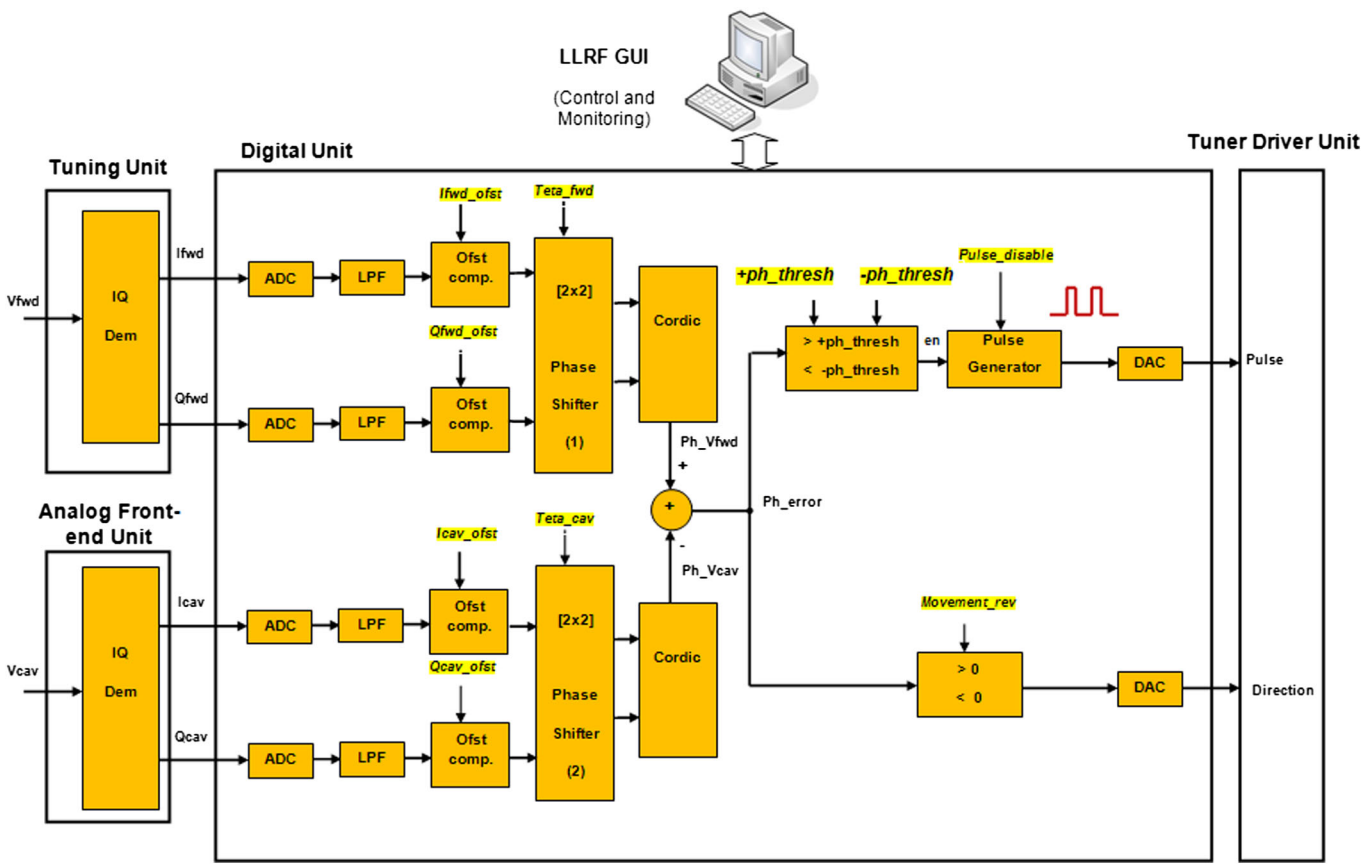

FIG. 8. Simplified block diagram of the FPGA program for cavity tuning; the parameters marked as *italic* are set from the control terminal.

the steady-state cavity voltage will be the same as the reference one.

B. Tuning loop

Figure 8 shows the schematics of the tuning algorithm which is also based on IQ demodulation.

In this case, two IQ demodulators are used to convert the measured forward and probe voltages to baseband. These signals are then sampled and fed into the FPGA where CORDIC algorithms are used to calculate the phase difference between the two rf signals (the FPGA and the IQ demodulator for probe voltage measurement in the tuning loop are physically the same as the ones used for the amplitude and phase loops). RFQ tuning is done by keeping the phase difference as close as possible to its reference where the reference phase is the one giving minimum reflected power from the RFQ in the presence of the beam. This is done by moving the RFQ tuner inward/outward if the phase error (i.e. the difference between the actual phase and the set value) exceeds the upper or the lower thresholds defined by ($+\mathrm{ph}_{\mathrm{thresh}}$, $-\mathrm{ph}_{\mathrm{thresh}}$). If that happens, the tuning loop moves the tuner in the right direction until the error enters the ($+\mathrm{ph}_{\mathrm{thresh}}$, $-\mathrm{ph}_{\mathrm{thresh}}$) again and then leaves the tuner at that position until the next time the error exceeds any of the thresholds. Similar to the amplitude and phase loops, two phase shifters are used in the FPGA to rotate the IQ vectors representing the forward and probe voltages (see Fig. 8). By properly adjusting them, one should satisfy the following two requirements simultaneously: (i) When the RFQ is tuned (i.e. minimum reflected power), the read-back phases of the forward and RFQ voltages are equal. (ii) When the RFQ is tuned, these two phases are as close as possible to zero. The first condition is required for making sure that regulating the phases to be equal corresponds to having minimum reflected power. The second condition is needed to make sure that moving the tuner from one extreme to the other does not cause any phase jump from $+180°$ to $-180°$ or vice versa in the CORDIC algorithms as that can make the tuner move in the wrong direction. This is not a strict

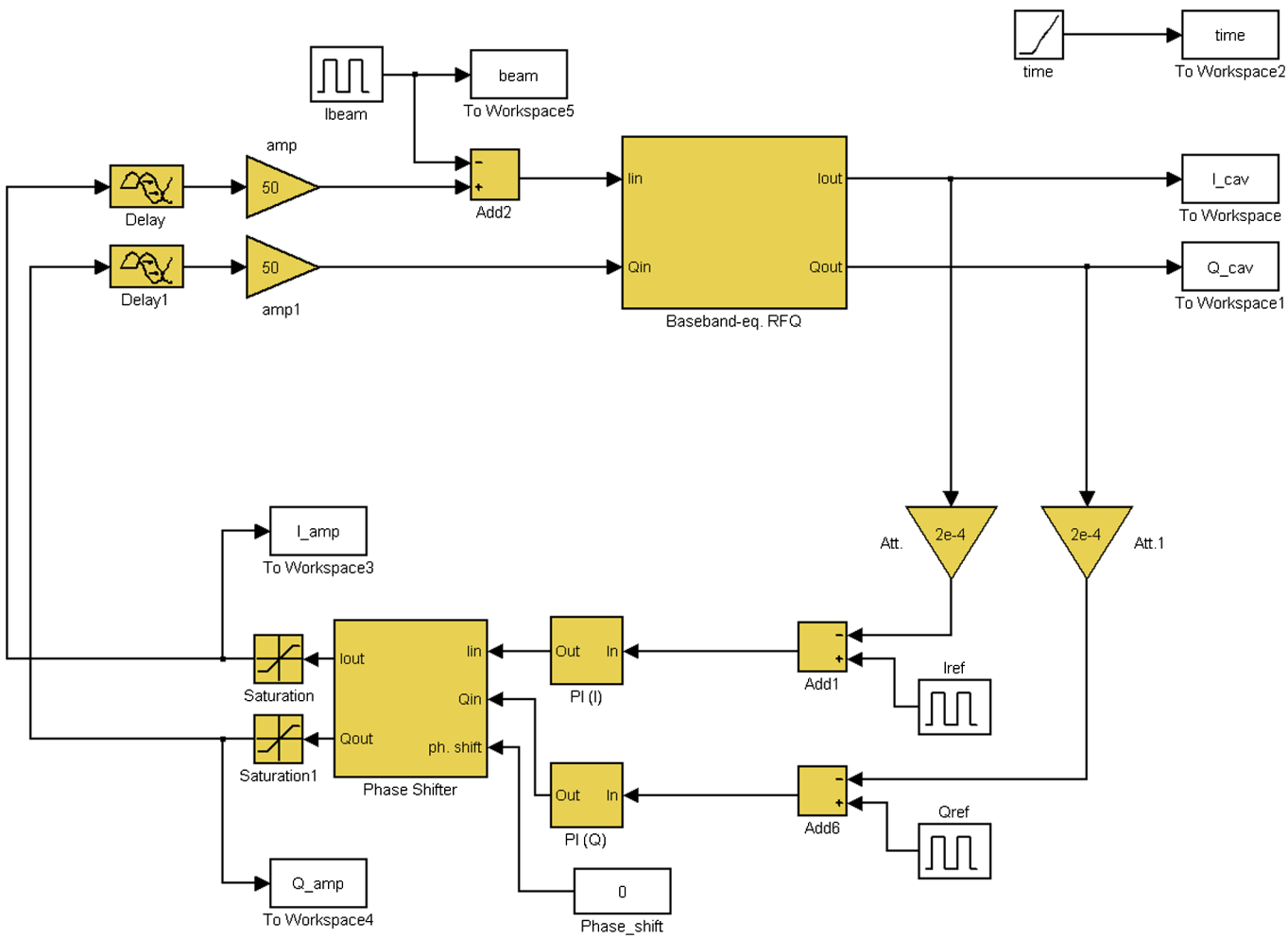

FIG. 9. Baseband-equivalent model of the feedback loop including the RFQ, the LLRF, and the rf amplifier; the model simulates the envelope of the signals in time domain with the advantage of significantly reducing the simulation time compared to the combined rf-baseband model.

requirement though as any phase in the $\pm 30°$ range would also be acceptable provided that the two phases are equal.

In order to prevent the tuner from an early wear-out due to continuous movement in pulsed operation, the tuning loop is only activated during the pulse after the RFQ phase has settled.

V. LLRF SIMULATION IN MATLAB-SIMULINK

Looking at the RFQ from a LLRF perspective, the operating mode can be characterized by its resonance frequency ω_0 and quality factor Q_0; therefore it can be modeled by a resistance-inductance-capacitance circuit. The input coupler is modeled by a step-up transformer where coupling factor β specifies the impedance matching between the amplifier and the operating mode. Figure 9 shows a baseband-equivalent model of the feedback loop comprising the RFQ, the LLRF, and the amplifier in MATLAB-SIMULINK. This model can be used to study the time-domain performance of the loop where all signals (including the RFQ voltage) are translated to baseband. The model then simulates the envelope of the rf signals (without rf carrier) with the advantage of significantly improving the simulation speed compared to the combined rf-baseband model.

Assuming the drive frequency is the same as the RFQ resonance frequency (i.e. $\omega_{\mathrm{rf}} = \omega_0$), the relation between the RFQ voltage V (referred to the primary side) and the amplifier current I can be simplified as the following set of differential equations [18]:

$$\begin{aligned} 2Q_0\frac{dV_i}{dt} + (\beta+1)\frac{dV_q}{dt} + (\beta+1)\omega_{\mathrm{rf}}V_i &= Z_0\omega_{\mathrm{rf}}\beta I_i \\ 2Q_0\frac{dV_q}{dt} - (\beta+1)\frac{dV_i}{dt} + (\beta+1)\omega_{\mathrm{rf}}V_q &= Z_0\omega_{\mathrm{rf}}\beta I_q, \end{aligned} \tag{7}$$

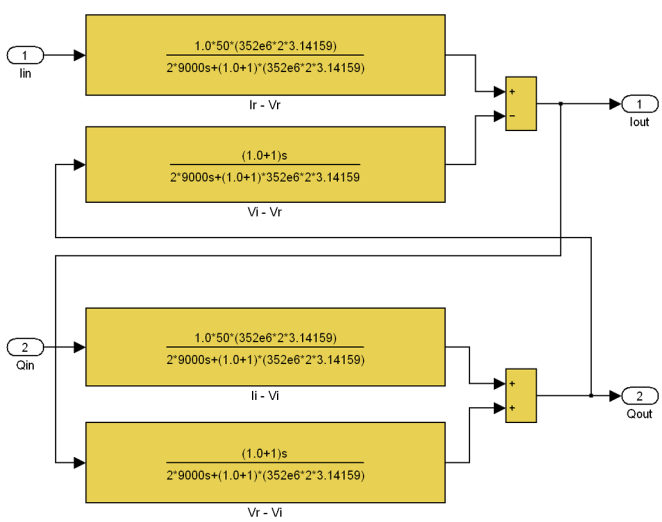

FIG. 10. Baseband-equivalent model of the RFQ represented as a MIMO system in MATLAB-SIMULINK.

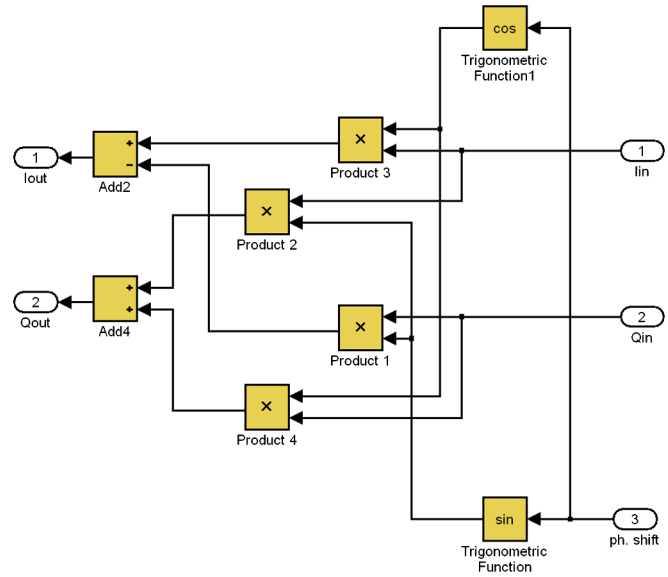

FIG. 11. MATLAB-SIMULINK model of the phase shifter.

where the i and q subscripts denote the in-phase and quadrature-phase component of the relevant variable, respectively. These differential equations can be represented in MATLAB-SIMULINK as a multi-input multi-output (MIMO) system using their equivalent transfer functions shown in Fig. 10.

Figure 11 shows the detailed model of the phase shifter simulating the overall phase shift introduced by the three phase shifters shown in Fig. 7.

In the simulations, the rf frequency was set to 352 MHz, the unloaded quality factor Q_0 was 9000, and the coupling factor β was set to 1. The gain of the rf amplifier (including the transconductance due to voltage-to-current inversion) was assumed to be 50, the total loop delay was set to 500 rf periods, and the voltage attenuation caused by the pickup loop was assumed to be 1×10^{-4}. The P and I gains were adjusted by trial and error until a satisfactory step response

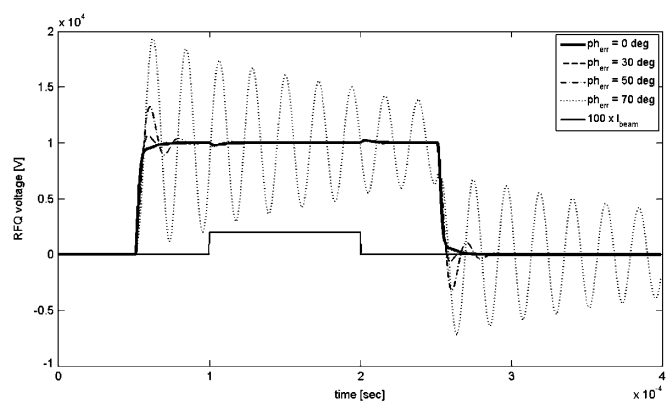

FIG. 12. Simulated RFQ voltage (referred to the primary side) in closed-loop mode; the pulse width was reduced to 200 μs in the simulations, the beam pulse (not in scale) starts at $t = 100$ μs and ends at $t = 200$ μs.

was achieved. With these parameters and assuming a 50 Ω system, setting the reference I (I_{ref}) to 1 V results in 1 MW of peak power in the RFQ.

Figure 12 shows the simulated step response of the loop under beam loading with several values of phase error. Loop instability occurs when the error exceeds ±70° marking the phase margin of the system.

VI. FEEDBACK LOOP INSTABILITIES DUE TO OTHER RESONANT MODES

The stability of the LLRF loop could in principle be affected by possible resonant modes adjacent to the cavity main resonance. For instance, the effect of the unwanted resonant modes of the nine-cell superconducting rf cavities of the ILC on the feedback loop stability has been discussed in [19]. A more detailed study on this topic has also been done for the European free electron laser (XFEL) which is based on the teraelectronvolt energy superconducting linear accelerator (TESLA) technology [20]. In both cases, the control scheme is based on high-gain proportional controllers so that the feedback loop can significantly suppress fast and nonpredictive disturbances. This, however, makes the feedback stability a delicate issue as the other fundamental modes (such as $8/9\pi$ and $7/9\pi$) cause loop instabilities after the introduction of even a small proportional gain. In order to avoid such instabilities, low-pass filters (in addition to well-adjusted digital notch filters in the case of XFEL) have been used to suppress the difference frequencies of these modes with respect to the desired π mode. Also, it has been shown that by increasing the delay of the sampled IF signal, the feedback loop goes through successive stable and unstable regions with an interval depending on the difference frequency of each fundamental mode with respect to the π mode.

In this section, we study these issues and some arising LLRF considerations for the RFQ and the spoke resonators of the ESS-B linac. First of all, it should be noted that the frequency separation of the operating mode to the nearest undesired resonant mode (known to be >8 MHz from the RFQ electromagnetic simulations and about 42 MHz from cold-model measurement on the double-spoke resonator) is much larger than the typical LLRF bandwidth (limited to a few hundred kHz by the averaging blocks in the FPGA). This, basically, makes it impossible for such frequencies to circulate around the feedback loop, hence removes the risk of instabilities due to the other resonant modes. This statement is further reinforced by considering the klystron bandwidth (2 MHz at −1.5 dB [21]) also removing the possibility for such frequencies to get amplified and fed into the cavity.

Contrary to the XFEL and ILC, the adopted control strategy for the ESS-B cavities is based on moderate proportional and integral gains. At the start of each rf pulse, typically 30%–50% of the drive voltage is provided by the proportional controller while the integral controller gradually increases its output (due to error accumulation) until the rf field reaches its desired level. The introduction of the integral controller (a zero-frequency pole in the transfer function) significantly increases the loop gain at low frequencies but still keeps it at moderate levels at higher frequencies. This not only improves the stability margins of the feedback loops (subsequent phase margin of ±55° as reported in the LLRF performance section) but also eliminates flattop steady-state errors in pulsed operation. On the other hand, the design of the LLRF and the adjustment of the P/I gains are so that the feedback loop is able to remove the highest-frequency disturbance (the 8 KHz ripples and the higher harmonics resulting from the insulated-gate bipolar transistor switching of the klystron modulator as known until now) in addition to having the desired rf settling time (< 100 μs).

Contrary to the XFEL and ILC LLRF systems, increasing the digital delay in the current design does not make the feedback loop go through stable and unstable regions. This is because increasing the delay of the sampled baseband signal does not cause any phase shift in the resultant rf signal after IQ modulation, while changing the delay of the IF signal changes the phase of the resultant rf signal, hence, can make the loop unstable. In [19,20], the feedback loop is reported to be made stable by introducing additional digital delays. In this design, however, the loop is made stable by the proper adjustment of the phase shifters as explained in the LLRF design description section without imposing an additional delay on the feedback loop.

VII. LLRF PERFORMANCE

Two series of tests were done in a laboratory environment to evaluate the LLRF performance: (1) low power tests with a mock-up cavity with resonance frequency of 327.14 MHz and unloaded quality factor of 1000 approximately and (2) tests with the RFQ cold model at the Imperial College London with 60 W of rf power. The experimental setup was the same as the one shown in Figs. 7 and 8 except the trombone phase shifter which was missing in the tests. The control loop parameters were adjusted following the procedures explained in the LLRF design description section. In the next subsections, we will discuss the significance of each of the parameters measured in the tests and additionally present the practical results.

A. Tests with the mock-up cavity

Figure 13 shows a photograph of the experimental setup used for these tests.

1. Amplitude and phase stability

The term ‘‘amplitude and phase stability’’ has been used during the past years in a rather naive way to express the overall unwanted variations of the amplitude and phase of

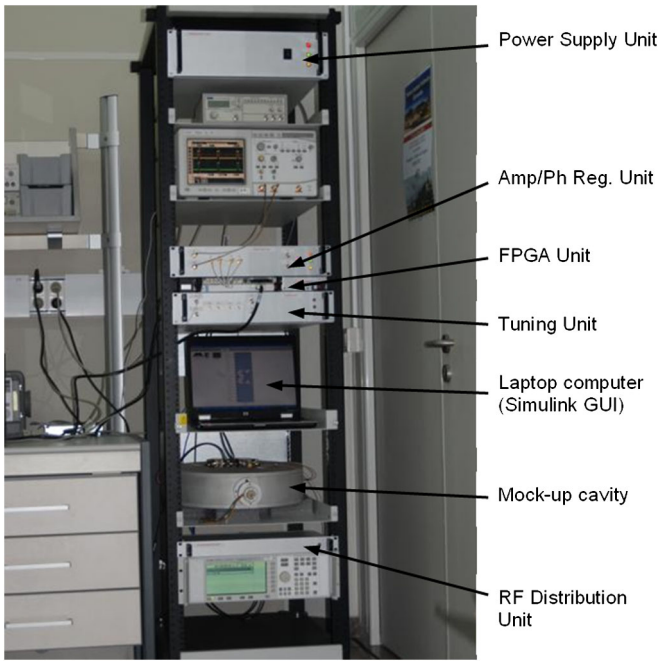

FIG. 13. Picture of the LLRF system being tested with the mock-up cavity at the rf laboratory of the UPV/EHU University.

the cavity field about their set values in percent and degree, respectively. It should be noted that the stability of the cavity field can be degraded by several effects, some of which are out of the framework of the LLRF. Therefore, a more profound way to determine the rf stability would be to consider all these effects one by one. The high voltage power supply (HVPS) of the rf amplifier, for example, can generate a significant amount of ripples on its output and that consequently can degrade the short-term stability of the cavity field. The regulation loops incorporated in the LLRF system will only be able to compensate these ripples if they have a large enough bandwidth to accommodate the ripple frequency. Also, the noise present on the distributed master oscillator (MO) signal can degrade the rf stability without being compensated by the LLRF system.

In the rf stability measurements, both short-term and long-term effects should be considered. Short-term stability is the unwanted variations of a signal due to fast disturbances (for example: noise or ripple) measured during short time periods (for example, 1 ms or less) while long-term stability is the slow signal deviations from their set values due to temperature changes, DC offset variations, aging, etc. during long periods (8 hours or longer).

Figure 14 shows the phase noise of the cavity voltage in dBc/Hz measured with a bandwidth of 3 Hz–300 kHz in cw mode with the cavity bandwidth being 200 kHz approximately. As this is almost equal to the phase noise of the signal generator (rf reference), one can conclude that the cavity phase noise could be further improved beyond the measured 0.1° by replacing the rf generator with a better one.

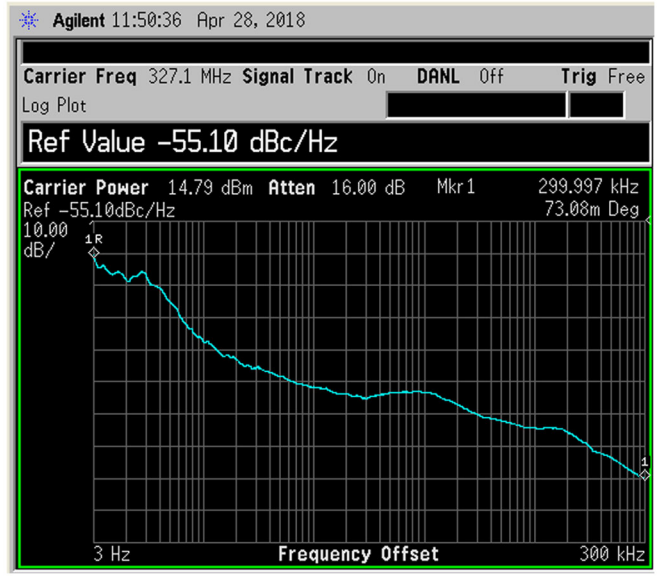

FIG. 14. Measured phase noise of the cavity field in closed-loop mode; the integrated phase noise in the cavity single sideband is less than 0.1°.

Figure 15 compares the power spectrum of the signal generator to that of the cavity pickup signal in pulse mode. As there is a close resemblance between the two waveforms at the rf frequency, this graph also confirms that the measured phase noise was mainly due to the signal generator.

In order to check the long-term performance of the LLRF, the system was put into operation with 65% of its maximum output voltage during a period of 100 hours continuously in an unregulated temperature environment. The cavity probe signal was measured with a rf power

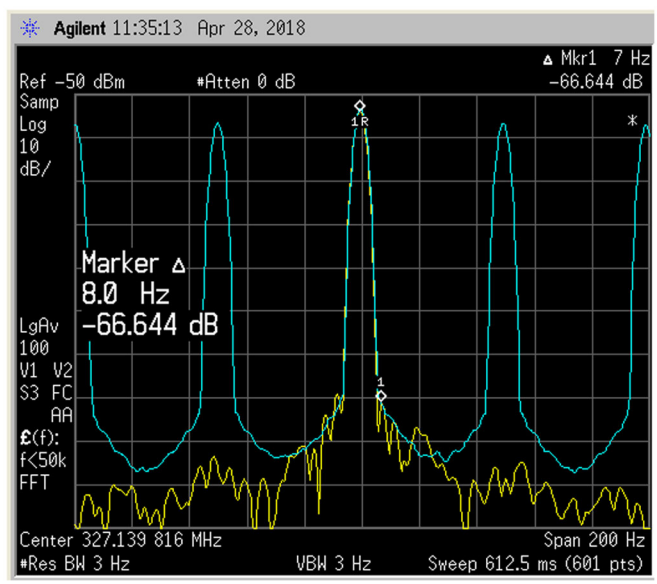

FIG. 15. Measured power spectral density of the rf signal generator and the cavity field in pulsed mode.

meter and the temperature by a PT-100 sensor using the LABVIEW program in both cases. The results obtained from these tests are shown in Figs. 16(a)–16(e).

From these graphs a few effects degrading the long-term stability can be identified. For example, the cooling system of the rf laboratory was switched on at $t = 43$ h and switched off at $t = 48$ h. The effect of these temperature variations on the long-term stability of the cavity field can be seen in Fig. 16(b), where the $\pm 0.5\%$ stability requirements and the power meter accuracy have also been shown for comparison. Also, it was observed that all the signals were much more stable during nights and weekends as the temperature variations and vibrations caused by the laboratory staff resulted in some stability degradations. This can be clearly seen during $t = 75$–100 h which corresponds to a weekend. For the final installation, it is planned to minimize these unwanted effects by regulating the temperature and installing the rf transmitter and the cavity in a vibration-free place.

During these tests, the cavity reflected voltage was always below 10% (i.e., 1% of reflected power) as it can be seen in Fig. 16(e). The reflected voltage can be further reduced by choosing a narrower phase error window at the expense of moving the tuner more frequently. If the window is too narrow, the tuner will vibrate at its position due to the noise on the measured phases. In the LLRF tests, tuner vibrations were observed with $(+\mathrm{ph}_{\mathrm{thresh}}, -\mathrm{ph}_{\mathrm{thresh}}) = (+0.2°, -0.2°)$.

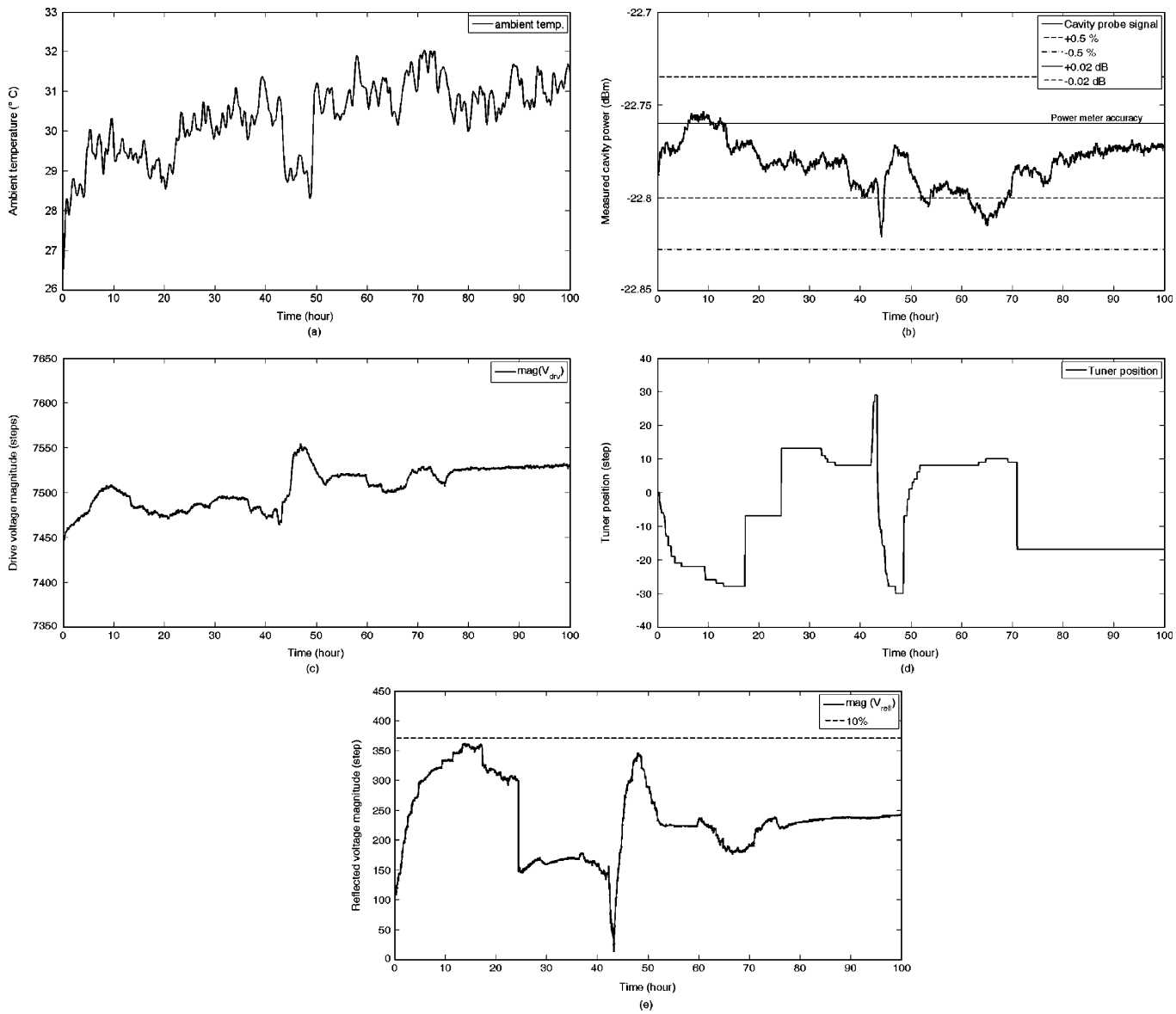

FIG. 16. 100-hour long-term stability measurements. From top to bottom: (a) ambient temperature, (b) measured cavity power, (c) cavity drive voltage (LLRF output), (d) tuner position, and (e) reflected voltage. The *steps* in cases (c) and (e) correspond to the DAC/ADC counts. In (d), the *steps* correspond to the pulses sent to the stepper motor.

For normal operation, the error window was set to $(+\mathrm{ph}_{\mathrm{thresh}}, -\mathrm{ph}_{\mathrm{thresh}}) = (+0.4°, -0.4°)$.

2. Linearity

Linearity becomes an important issue when the rf field is changing such as in ramping or pulsed rf applications. System nonlinearities cause actual amplitude/phase of the cavity to deviate at some point from its set value degrading the system accuracy. Also, strong nonlinearities push feedback loops towards becoming unstable. The main contribution to the overall system nonlinearity is usually due to the LLRF or the rf amplifier depending on its type. Klystron amplifiers, for example, are known to have significant nonlinearities at their peak power level. These nonlinearities will therefore be seen in open-loop operation. In closed loop, however, the nonlinearity of the rf amplifier will be automatically compensated by the integrator part of the regulator (for example, if a PI regulator has been utilized for the feedback loop) provided that no signal becomes saturated. The nonlinearity of the signal path from the cavity pickup loop to the PI regulator will then determine the overall system nonlinearity. This implies that the input stage of the LLRF system, which usually converts the probe voltage to baseband, should be as linear as possible while the linearity of the output stage is of less importance. Figure 17 presents the linearity of the regulation loop showing a very good response up to the saturation level of the DACs generating the drive voltage for the IQ modulator. The signal levels are therefore configured so that the maximum amplifier power can be achieved before the DAC becomes saturated.

3. Transient response

Transient response deals with issues related to the evolution of the cavity field with time upon a change in the reference level [18]. Also, the response of the regulation loops to the disturbance caused by the beam is studied under this topic. The cavity transient response, in general, needs to be as fast as possible but should not undergo any overshoot or oscillation. This requirement implies that the LLRF bandwidth should be larger than the cavity bandwidth by a factor of 5–10 and the delay of the electronics be short. Then, the time constant of the feedback loop can be reduced through the adjustment of the regulator gains to be almost equal to the natural time constant of the cavity. Also, the response of the loop to the beam, which acts as disturbance, will be similar to the one of the reference change because the loop dynamics is the same in both cases. Figures 18 and 19 show the pulsed cavity voltage in closed-loop mode and an expanded view of the pulse at the rising edge. The measured settling time is 1.9 μs which is almost the same as the one due to the natural step

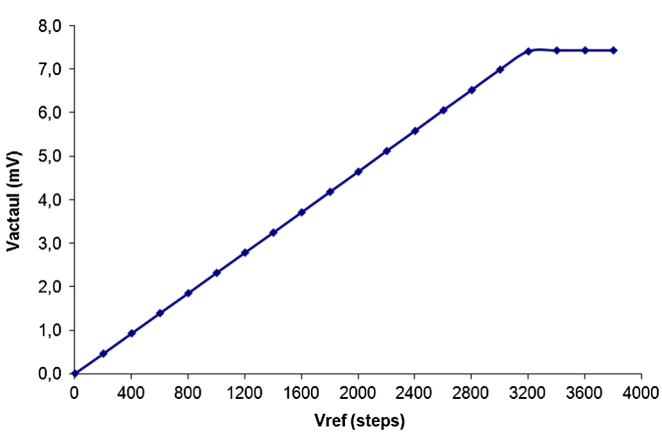

FIG. 17. Linearity response of the LLRF system in closed-loop mode. The horizontal axis is the reference value of the cavity voltage and the vertical one is the actual cavity voltage measured by a spectrum analyzer configured directly in mV unit.

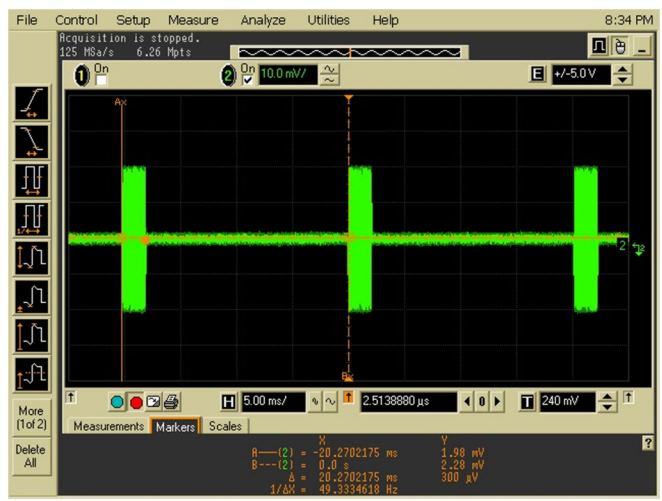

FIG. 18. Measured cavity voltage in pulsed mode with a pulse rate of 50 Hz and pulse width of 2 ms.

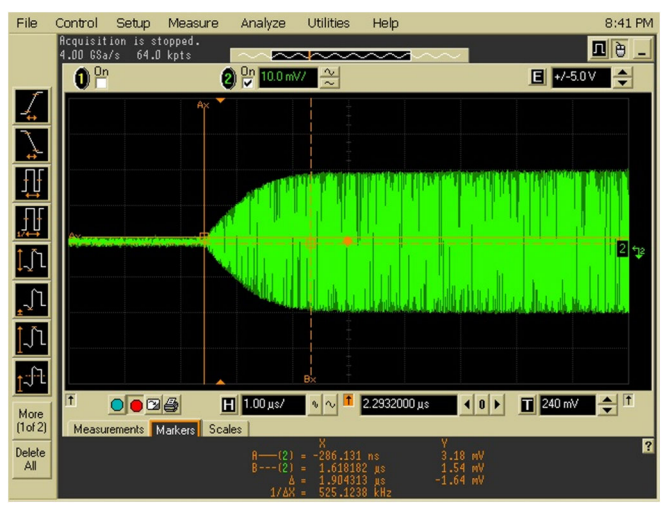

FIG. 19. A zoomed view of the cavity pulse at the rising edge with a settling time of 1.9 μs.

response of the mock-up cavity. The pulse rise time can be further reduced by injecting more power into the cavity at the rising edge using the feed-forward inputs shown in Fig. 7 with the hard limit being the maximum available power from the rf amplifier.

The total loop delay was measured at 800 ns approximately. From that amount, 500 ns was due to the ADCs and DACs, 200 ns was the delay of the baseband low-pass filters in the FPGA, and about 100 ns due to the control program and the cable lengths. It is important to note that large loop delays can make the loop response oscillatory or even unstable; therefore care should be taken to reduce the loop delay as much as possible by utilizing fast electronics and short signal paths.

4. Loop stability

A feedback loop in some circumstances becomes unstable. That can happen, for example, if the loop gain is too high, or the loop has severe nonlinearities or long delays. As the loop gets closer to the instability point, larger oscillations become visible on the signals and the amplitude of the oscillations grows until the signals saturate or the interlock system eventually intervenes and stops the plant.

The phase margin of the system was measured simply by changing the amount of the phase shift introduced by the phase shifters shown in Fig. 7 and loop instability was observed at $\pm 55°$ about the optimum phase. Although this is smaller than the simulated phase margin with the mock-up cavity (i.e. $\pm 73°$ with 800 ns of loop delay), it still provides a very large margin to ensure the loop stability. The difference between the simulated and the measured phase margins is believed to be due to the errors and dynamics which were ignored in the simulations such as the amplifier nonlinearity and the filter dynamics.

B. Tests with the RFQ cold model

The design/manufacturing of the RFQ cold model is the same as the one intended for the future Rutherford Appleton Laboratory–front end test stand (RAL-FETS) except the length which is 40 cm instead of the desired length of 1 m for each RFQ section. Because of this and due to the effect of the flat end plates, the resonance frequency and the unloaded quality factor of the cold model are different from the final ones (319 MHz and 7773 instead of 324 MHz and 9000) [22]. The preliminary results obtained from these tests are similar to the ones from the mock-up cavity except the settling time which is significantly longer due to the increase of the quality factor (see Fig. 20). Looking at the rising edge of the pulse, two time constants can be distinguished. The shorter one ($\tau \approx 6\ \mu$s) which happens first is due to the RFQ and amplifier dynamics when the P control has a dominant effect while the longer one is due to the integral part of the PI regulator (it can be reduced through a readjustment of the PI gains).

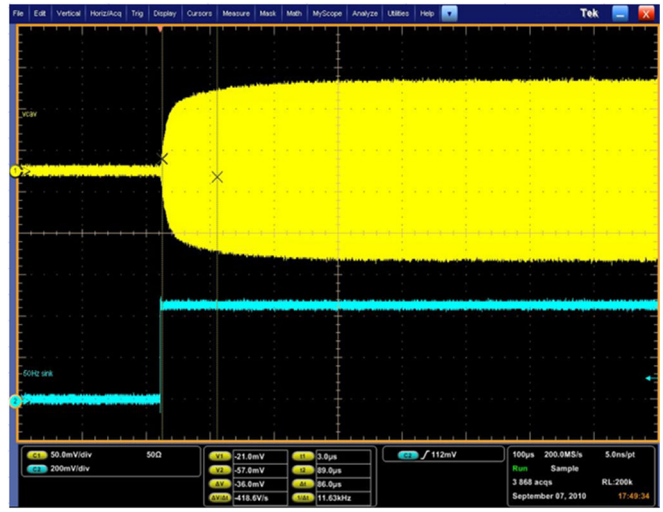

FIG. 20. Measured RFQ voltage in pulsed mode; the settling time (100 μs approximately) can be further reduced by a readjustment of the PI gains and/or feed-forward control.

Tuning an RFQ is not a trivial task due to its mode spectrum. While in a pill-box cavity it is rather easy to lock on the desired resonance mode, in an RFQ three independent azimuthal modes exist, being one quadrupole and two dipole modes. The quadrupole mode is formed by the magnetic flux from each vane splitting in two halves each flowing around the tip of the vane and returning in the two adjacent quadrants. The dipole modes, on the other hand, are formed by each pair of the opposite vanes [23]. From flux conservation, the azimuthal sum of the fluxes in the four quadrants is equal to zero. When the RFQ is properly tuned, the amplitudes of the fluxes in all four vanes are equal minimizing the amplitude of the dipole modes and resulting in best approximation to a pure quadrupole operating mode. If the RFQ is not well tuned, the amplitudes of the four fluxes are not equal and the cavity mode will be an admixture of the quadrupole mode and the two dipole modes. In the RFQ mode spectrum, it can be seen that the frequency of the dipole modes lies typically a few percent lower than that of the operating quadrupole mode introducing the possibility of accidentally exciting a higher longitudinal mode of the dipole family [23].

The tuning tests with the RFQ cold model were done with one motorized tuner mounted in one RFQ quadrant and three manual tuners on the other three quadrants. It was then observed that at a specific position of the motorized tuner there was a sudden jump in the $\mathrm{ph}(V_{\mathrm{fwd}}) - \mathrm{ph}(V_{\mathrm{cav}})$ due to the excitation of the dipole modes causing tuner vibrations. This usually happened half an hour after the system start-up when the RFQ temperature rose up and the motorized tuner reached that specific point. Because of this reason, it is foreseen to replace the manual tuners with

TABLE II. LLRF performance summary.

Parameter	Specifications	Actual	Unit
Operation mode	Pulsed	cw/pulsed	
Settling time	≤ 100	<100[a]	μs
Loop delay		800 approximately	ns
Phase noise	± 0.5	± 0.1	°
Short-term amplitude stability	± 0.5	$< \pm 0.1$	%
Long-term amplitude stability	± 0.5	$< \pm 0.5$	%
Linearity		100 approximately	%
Dynamic range		>30	dB
Phase margin		± 55	°
Maximum reflected power		<1	%

[a]The settling time with the final RFQ is estimated at 30–50 μs.

motorized ones so that all four tuners move in parallel, thus keeping a good separation between the quadrupole and dipole modes [24].

VIII. SUMMARY AND CONCLUSION

A pulsed digital LLRF system has been designed and developed by the ESS-Bilbao rf group in collaboration with the Electricity and Electronics Department of the University of the Basque Country and the ISIS laboratory to be used for the RFQ systems of RAL-FETS and the future ESS-Bilbao linac. As the LLRF system should control large quantities of pulsed rf power, it needs to have a wide bandwidth and a good transient response so that the rf pulse settles in a short time before the beam pulse enters the cavity. The proposed LLRF design for these accelerating structures is based on direct rf-to-baseband conversion using an analog IQ demodulator, baseband signal processing in a FPGA, and finally up-conversion to rf using an IQ modulator. In order to improve the accuracy of the probe voltage measurement, errors inherent to analog IQ demodulators have been identified and compensated by FPGA algorithms and proper setting of the feedback loop parameters. Computer simulations and practical results obtained from a mock-up cavity and an RFQ cold model verify the ability of the LLRF system to meet all the requirements such as amplitude and phase stability, dynamic range, phase margin, and linearity as shown in Table II. Furthermore, the effect of unwanted resonant modes on the stability of the feedback loop is studied showing that such instabilities are very unlikely due to the LLRF design and the mode spectrum of the accelerating structures.

The current LLRF system can be favorably compared with those used in linacs with similar applications [3,4] and takes us to a next step where the aim will be a focus on the efficient control of the effects of rf phase and amplitude noise on the beam emittance, a territory for which charts have only recently been sketched [25]. Finally, some considerations of the present development, such as expanding the tuning system to control the tuners of each RFQ section independently, is now under study. Also, within the next two years, it is foreseen to develop an industrial version of the LLRF system suitable for being used for the future linac and test it with the RFQ and the klystron amplifier up to the nominal power.

ACKNOWLEDGMENTS

The authors would like to thank the Electricity and Electronics Department of the University of the Basque Country (UPV/EHU) for providing the required equipment and their assistance and support during the LLRF development and tests. We also extend our appreciation to Alan Letchford and David Findlay from ISIS for the technical discussions and Saad Alsari from Imperial College London for the help we received in the tests with the RFQ cold model.

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