Cascade ΣΔ modulator with digital correction for finite amplifier gain effects

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This paper presents a simple and fully digital solution to correct the effect of amplifier finite gain in cascade ΣΔ modulators. The main contribution of this letter is a simple digital method to evaluate the integrator pole errors, which are further taken into account to modify the reconstruction filter. The method is applied to a 2-1 cascade modulator.

Cascade modulator: The operation of cascade ΣΔ modulators is similar to that of a pipeline converter in the sense that the first modulator makes a coarse conversion of the signal and the successive modulators are used to digitize the quantization error of the preceding stage. Signal reconstruction is achieved by mean of the proper digital filter that takes into account the shaping applied to each conversion [1]. Figure 1 shows a 2-1 ΣΔ cascade modulator topology that consists of a 2^{nd} order double-loop modulator with single-bit quantizer as a first stage and a 1^{st} order modulator with single-bit quantizer as a second stage.

The governing equations of such a modulator are,

$$Y_1 = z^{-2}X + (1-z^{-1})^2 E_1$$
$$Y_2 = z^{-1}E_1 + (1-z^{-1})E_2 \quad (1)$$

where E_1 and E_2 are the quantization errors of the first and second stage respectively.

The reconstruction filter needed to obtain a 3rd order noise shaping is described by,

$$Y = z^{-1}Y_1 + (1-z^{-1})^2 Y_2 \quad (2)$$

Amplifier finite gain compensation: In the previous description, the reconstruction filter has been derived assuming ideal integrators. But real integrators present pole errors that are related to amplifier finite gain. These pole errors modify the actual shaping of the quantization error. As a result, the cancellation of the 1st stage noise will not be complete unless the real shaping is taken into account.

Let the first, second and third real integrator z-domain transfer function be

$$\frac{z^{-1}}{1-p_1 z^{-1}}, \quad \frac{z^{-1}}{1-p_2 z^{-1}}, \quad \frac{z^{-1}}{1-p_3 z^{-1}} \quad (3)$$

respectively. Parameters p_1, p_2 and p_3 represent the real integrator poles.

In order to obtain a third order behaviour, the reconstruction filter has to be modified to take into account the real integrator poles. Nevertheless, a Taylor development of the error introduced using the ideal reconstruction filter of (2) shows that the main degradation can be compensated by simply taking,

$$Y = z^{-1}Y_1 + (1-p_1 z^{-1})(1-p_2 z^{-1})Y_2 \quad (4)$$

Pole error evaluation: One of the key points for the efficiency of the digital correction is the evaluation of the corrective parameters (p_1 and p_2 in our case). Most proposals describe adaptive solutions that can follow drifts in the parameter values [2] [3]. However, such solutions are usually costly as they require the introduction of an error signal to be minimized as well as a correlation filter. The former can have an impact on the modulator performance and the latter can represent an important amount of hardware. In [4] a correction mechanism is proposed but an efficient method to determine the correction terms is lacking.

In this letter, a solution is proposed to evaluate integrator pole errors. The principle of operation is illustrated in figure 2. In a first step (see figure 2), the normal input path to the modulator is disabled and a periodic digital sequence is sent to the modulator re-using the feedback DAC during the sampling phase. Notice that the sequence can be stored in a recycling register. In this situation, it has been shown in [5] that the mean value of the output bit-stream deviates from the input sequence mean value in an amount that is proportional to the pole error. Hence, the pole evaluation is carried out by up/down counters and simple logic that perform the sum of the difference between input and output bit-streams over a given number of samples. The counter output for the test of the first integrator pole error (see figure 2) is,

$$counter1 \approx 2NQ(1 - p_1) \tag{5}$$

where Q is the input sequence mean value, and N the number of summed samples

In a second step (see figure 2), the normal input to the second integrator is disabled and a delay is introduced in the digital feedback path. Here again, a periodic digital sequence is sent to the 2nd integrator re-using the feedback DAC during the sampling phase. For an input sequence of the form [1 1 … 1 0] (with a number *L-1* of 1s and one 0, and *L*>5), it has been shown [6] that the counter output is,

$$counter2 \approx \frac{2N(1-p_2)}{\ln\left(\frac{5-3L}{5-L}\right)} \tag{6}$$

For both the first and second integrator pole error evaluation, the impact of an input-referred offset on the counter value can be compensated performing an additional evaluation using in this case the opposite sequences. The result of the second evaluation has just to be subtracted from the result of the first one.

From the two counter outputs, estimators of the pole errors p_1 and p_2 can easily be derived, in particular if the equation parameters (*N*, *L* and *Q*) are chosen such that the required division can be approximated by register shift.

The proposed method has been validated using a realistic MATLAB Simulink model of the cascade 2-1 modulator that takes into account the major shortcomings of ΣΔ modulators [7]: thermal noise, amplifier finite gain, slew-rate and bandwidth, saturation, etc. All the parameters other than the amplifiers gain were set to acceptable values such that the influence of amplifier finite gain could be isolated. A Monte-Carlo simulation of 200 runs was performed, randomly varying the amplifier gains in the range [30;70]dB. For each run, the pole errors were evaluated as explained above for an input

sequence of the form [1 1 1 1 1 0] for both integrators. We thus have Q=2/3, L=6, and N was set to 33000 points. Furthermore, the modulator Signal-to-Noise Ratio (SNR) for an input sine wave of amplitude 70% of full-scale was evaluated for the uncorrected case (equation (2)) and the corrected case (equation (6)). This was done by filtering and decimating the modulator output by 128 and calculating an FFT over 1024 points. Figure 3 represents a histogram of the corrected and uncorrected SNR. The impact of pole errors can be seen as the uncorrected SNR is dispersed over a wide range. The efficiency of the proposed correction method is also demonstrated. Indeed, the corrected SNR is centred near the maximum achievable value and the average improvement over the 200 runs is as high as 2.8 effective bits.

Conclusions: A simple and fully-digital correction scheme has been proposed to take into account the finite amplifier gain effects in cascade $\Sigma\Delta$ modulators. The integrator pole errors are evaluated in foreground. The corrective action is carried out by modifying the reconstruction filter, which has been shown to greatly improve the modulator signal-to-noise ratio.

Moreover, the proposed technique could very well be extended to self-correction, provided that the reconstruction filter be automatically updated using the evaluation counter outputs. This could be realized at power up or periodically when the modulator is idle, with no need of external circuitry or signals.

Acknowledgments:

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List of Captions:

Figure 1

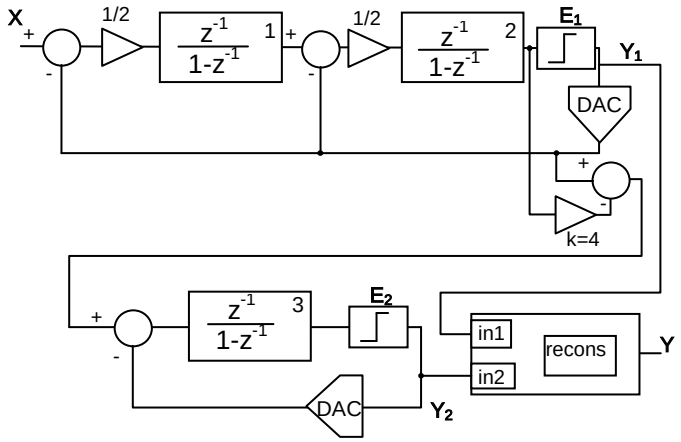

X
+
-
1/2
$\frac{z^{-1}}{1-z^{-1}}$
1
+
-
1/2
$\frac{z^{-1}}{1-z^{-1}}$
2
E_1
Y_1
DAC
+
-
k=4
+
-
$\frac{z^{-1}}{1-z^{-1}}$
3
E_2
in1
in2
recons
Y
DAC
Y_2

Figure 2

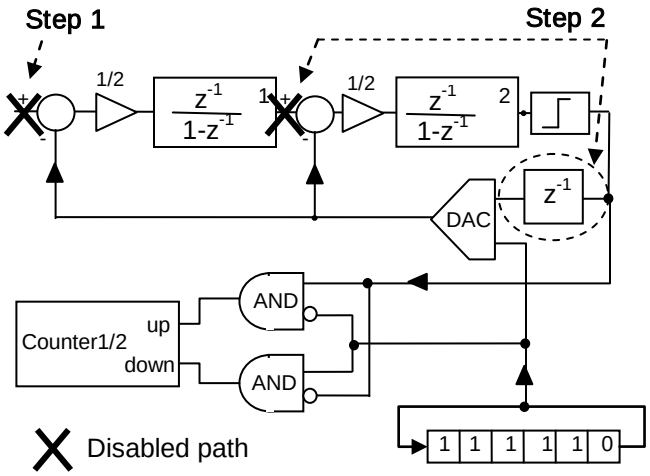
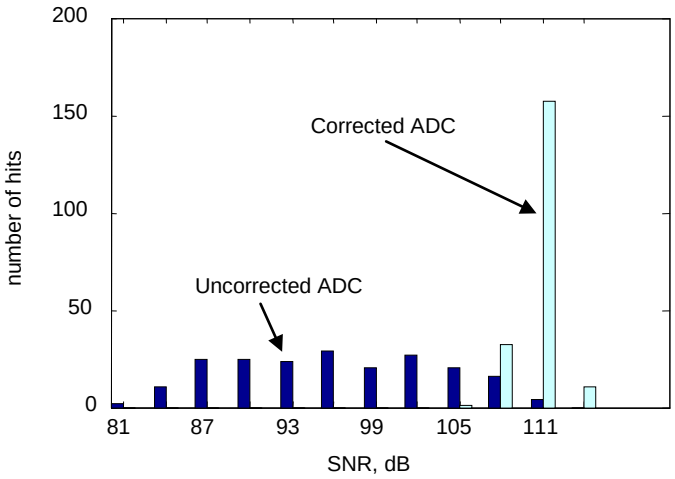

Step 1
Step 2
1/2
1/2
DAC
AND
AND
up
down
Counter1/2
Disabled path
1 1 1 1 1 0

Figure 3


200
150
100
50
0
number of hits
Corrected ADC
Uncorrected ADC
81
87
93
99
105
111
SNR, dB