Low-Cost Digital Detection of Parametric Faults in Cascaded ΣΔ Modulators

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***Abstract*—The test of ΣΔ modulators is cumbersome due to the high performance they reach. Moreover, technology scaling trends raise serious doubts on the intra-die repeatability of devices. Increase of variability will lead to an increase in parametric faults difficult to detect. In this paper, a design-oriented testing approach is proposed to perform simple and low-cost detection of variations in important design variables of cascaded ΣΔ modulators. The digital tests could be integrated in a production test flow to improve fault coverage and bring data for silicon debug. A study is presented to tailor signature generation, with test time minimization in mind, as function of the desired measurement precision. The developments are supported by experimental results that validate the proposal.**

***Index Terms*—ΣΔ modulation, Design for testability, testing, fault diagnosis.**

I. Introduction

In the field of analog to digital conversion, ΣΔ converters manage to push much of the hardware to the digital domain. As a result, this type of converter benefits of technology scaling in a major amount than other architecture. The vast success of ΣΔ converters has motivated extensive research which has driven ΣΔ modulators to their limits.

As technology shrinks to the nanometer scale, the scientific community agrees to state that intra-die variability (i.e. device mismatch) will become a major bottleneck if it is not properly handled [1]. From a test viewpoint, an important increase of parametric faults can thus be expected. For ΣΔ modulators, that have gained much interest because of their low sensitivity to the performance of their analog parts, such an evolution might be critical. Indeed, ADC black-box functional tests may fail to detect parametric deviations that could evolve as reliability issues.

Interesting functional Built-In Self-Test (BIST) techniques can be found in the literature. In [2] is shown how to compute in a simple manner the gain error, offset and 3^{rd} order distortion of the ADC transfer function. On the other hand, [3] implements an on-chip histogram test, and [4] uses digitally encoded sine-waves to perform FFT tests. In the original work, a filter is used to remove the quantization noise. However, several works have proposed to directly use the ΣΔ encoded sine-wave as a test stimulus for ΣΔ modulators. In [5], the authors propose to use a sine-wave encoded at the same order as the modulator under test but to scale down the resulting stimulus with respect to the full-scale. In this way, they ensure that the quantization noise of the test stimulus remains below that of the modulator. In [6] and [7], the authors propose to use a sine-wave encoded at a higher order, so that the portion of the test stimulus quantization noise that lays in the base-band of the test stimulus is lower than that of the modulator under test. These techniques have proven useful to evaluate functional metrics at reasonable cost but with, at best, the same precision as the standard functional test they are based on. In particular, it is shown in [7] that the test accuracy is limited for signals close to full-scale. Similarly a fault simulation in [6] demonstrates that the proposed test underestimates the distortion in some cases. In that sense, they can help reducing the cost of a functional test flow but do not provide added value in terms of fault coverage.

On the other hand, purely defect-oriented approaches usually lack of faithful validation. Indeed, it is not possible to physically model and simulate all the possible defects (including electrical deviations) and to estimate their probability of occurrence. The validation of defect-oriented approach is thus limited to fault coverage [8], where accuracy has to be sacrificed for computability. In switched capacitors circuits, only shorts, opens and deviations in the capacitor ratios are often considered [9], [10].

In previous papers [11] and [12], the authors have proposed a fully digital BIST scheme that allows to measure important design variables of the main building block of ΣΔ modulators: namely, the integrator pole error and its settling error. In this paper, we show how the digital tests could be integrated in a production test flow to improve fault coverage and bring data for silicon debug. Indeed the requirement of hardware simplicity can be relaxed if the target is not a full-BIST scheme, and better test signature can be built.

Relying on experimental results from an integrated prototype, it is shown how the signature generation can be tailored to reach an adequate precision on the measurement of integrators leakage and settling errors. The fully digital nature of the test allows the use of a low-cost digital tester and enables parallel test, while test time remains greatly lower than conventional FFT-based functional test.

The test scheme is a good complement to functional test, as it brings important information on building blocks. In that

This work has been partially funded by the Junta de Andalucía project EXC/2005/TIC-927 and by the Spanish Government project TEC-2007-68072.

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sense, it could be compatible with the functional BIST scheme proposed in [6] that performs an SNDR test using a 1-bit digital stimulus like in [4], leading to noticeable agreement with standard SNDR test for small amplitudes. The injection of this digital stimulus relies on the same principle as for our method. As was said previously, one drawback of the approach in [6] is that it cannot detect small THD induced by near full-scale signals. Our approach would not only improve the defect coverage for this case, due to the good sensitivity to integrator settling error, but also enhance diagnosing capability.

The paper is organized as follows: Section 1 reviews the digital tests and presents the $\Sigma\Delta$ modulator prototype fabricated to prove their feasibility. Section 2 demonstrates how test signature can be effectively generated to provide diagnosis capability in a reduced time. Section 3 addresses the possibility to use the decimation filter for test purpose if the bit-stream is not accessible, and provides interesting comparison with functional test results. Section 4 discusses possible improvements of the method, and Section 5 draws the conclusions of the paper.

II. The digital tests

A. Test concept and prototype

The idea behind the proposed tests is to evaluate the non-idealities of the building blocks that compose a cascaded $\Sigma\Delta$ modulator. Principally, tests have been developed to evaluate the pole error and the settling error in the different integrators, because these design variables are key to the overall performance of $\Sigma\Delta$ modulators. This approach can be applied to any cascaded combination of 1^{st} and 2^{nd} order stages. Work is still necessary to extend the proposal to higher order single-loop architectures. While 1^{st} and 2^{nd} order modulators are inherently stables, higher order modulators can have bounded states only for a limitted range of inputs [13]. The digital stimuli used for test purpose in our proposal induce higher internal states than DC levels [14]. Stability during test mode may thus be a concern for modulators of order higher than 2.

Multibit quantizers are usually used only in the last (and less critical) stage of cascaded modulators. We will thus limit the scope of this paper to single-bit quantizer, but the reader can refer to [11] and [14] for multi-bit tests.

The procedure is common to all the tests, and the generic setup is shown in Fig.1 for a cascaded modulator. Under test mode, the modulator operating conditions are set such that the DC component of the response deviates from the DC component of the test stimulus in an amount that is proportional to the non-ideality under test.

The test stimulus is a digital sequence that can be periodic (with a short period of less than 10 samples) or pseudo-random. The output bit-stream (Y_i) is acquired by the test equipment (i.e. a simple digital ATE) and the signature computed off-chip.

The modifications of the modulator operating conditions affect exclusively control signals of the switches. As a result, a configuration register has to be introduced to control the different test modes. It is important to notice that no additional switch is introduced, so that the signal path remains unaffected

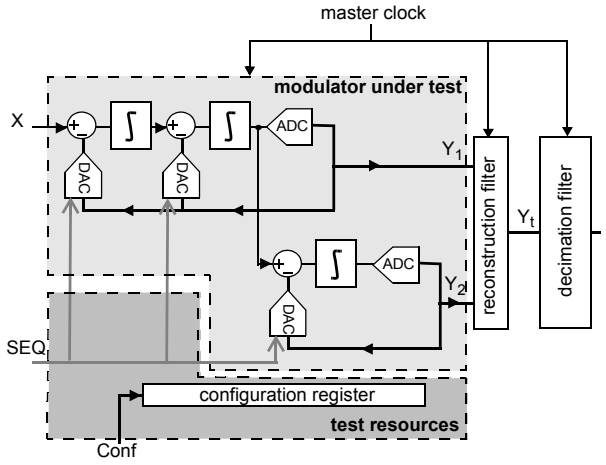

Fig. 1. Generic setup for cascaded $\Sigma\Delta$ modulator digital test with two dedicated test inputs: one for configuration and another for the digital stimulus

by the DfT modifications and no particular optimization is needed for the building blocks. The switch control modifications require some clock gating, in a way similar to what is proposed in [7]. In any case, this is not a critical point from a jitter perspective, because the gated switches are not those that define the sampling instant. More details can be found in [12] and [14] about practical implementation. Among other modifications, each summing node is modified such that the direct input (i.e. the positive input in Fig.1) can be disabled and the feedback DAC can be re-used to send the test sequence. In this way, the different stages of the cascaded modulator can be considered individually.

In order to give experimental support to our approach, a prototype has been integrated in a CMOS 0.35 μm technology. This prototype is the 2-1 cascaded modulator shown in Fig.2. The three integrators are driven by the same sampling and feedback phases (Φ_1 and Φ_2, respectively) at a nominal frequency of 2MHz. On the left side, the z-domain and switched capacitor implementation is presented for nominal operation. It can be noticed that the switches that form the feedback DACs are driven by the stage output. On the right side an example of test configuration has been illustrated. The 2^{nd} and the 3^{rd} integrators are tested in parallel. The switch of the direct path of the integrator under test is maintained open while the feedback DAC is re-used during the sampling phase (Φ_1) to send the test stimulus. It can be appreciated how the test configuration for the 2^{nd} integrator actually reconfigures the stage as a first order for test purpose. In order to test the first integrator, the digital stimulus would be fed through the first DAC, and the nominal input switches dsiconnected. The rest of the modulator could remain unchanged with respect to nominal operation, though the second stage (i.e. the 3^{rd} integrator) could also be disconnected and tested in parallel.

It is known that the performance of a $\Sigma\Delta$ modulator is more sensitive to the first integrator than to those located further in the loop which can be simplified. However, for the sake of design time reduction, the same integrator has been re-used in our prototype. This also brings us the possibility to directly compare the results obtained for the 3 integrators.

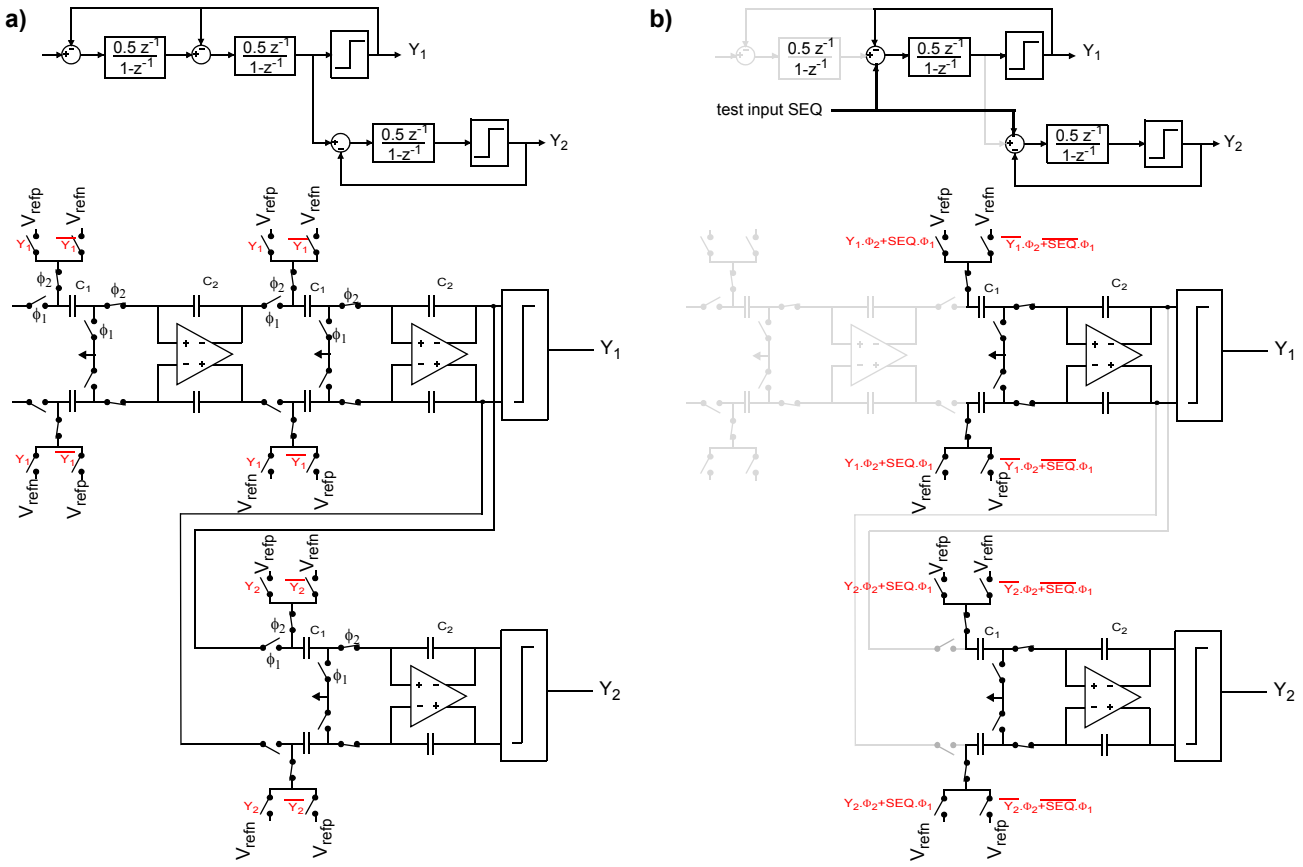

Fig. 2. $\Sigma\Delta$ modulator prototype: a) in nominal configuration; b) in leakage test mode for the 2^{nd} and 3^{rd} integrators, the nominal integrator input switch remains open and the feedback DAC is re-used to input the test sequence during phase Φ_1

The prototype includes all the DfT modifications required to perform the proposed tests: few logic gates and a configuration register to properly control the switches and the feedback DAC. The test sequence and the master clock are generated externally. Similarly, the output bit-streams of the two stages are shifted off-chip, which means that both the reconstruction and decimation filters have to be emulated in software. This option has been preferred in order to get a major flexibility on the post-processing.

Apart from these necessary test-purpose modifications, the prototype also includes a simple mechanism to induce parametric deviations in the behaviour of the integrators. Namely, an external tuning voltage has been considered to control the bias currents of the 3 amplifiers. Though such a mechanism cannot model all the possible parametric defects that may arise in an integrator, a similar effect would be obtained, for instance, from a mismatch in a current mirror. In any case, there is no doubt that varying the bias current modifies the performance parameters of the amplifier. This is illustrated in Fig.3 that displays electrical simulation results of the amplifier DC gain, Slew-rate and Gain-Bandwidth product versus the included tuning voltage [12].

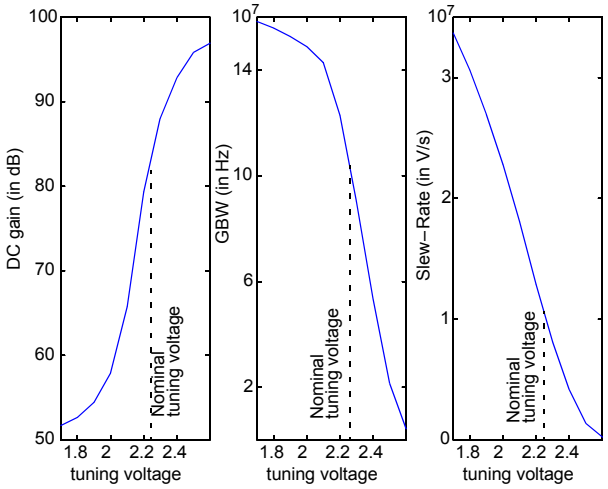

Fig. 3. Amplifier characteristics versus tuning voltage

B. Integrator leakage test

An integrator pole error causes the leakage in the modulator base-band of a portion of the quantization noise shaped at an order lower than the modulator order. As a consequence, the modulator SNR is reduced. This phenomenon is more severe for cascaded modulators than for single-loop modulators, due to improper noise cancellation in the reconstruction filter. We have proposed tests to measure the amplifier DC gain (i.e. the integrator pole error) in 1^{st} and 2^{nd} order modulators [11] and we present here a brief summary.

For the 1^{st} integrator of a 2^{nd} order modulator, the proposed test is very simple. It consists in sending a digital sequence (SEQ) of mean value Q different from 0 to the modulator and checking how the mean value of the output bit-stream (Y) deviates from the input sequence mean value.

To get rid of an eventual input-referred offset, another acquisition (quoted with a star symbol in (1)) has to be performed with an input sequence of mean value $-Q$. A z-domain analysis shows that the obtained signature is equal to,

$$\begin{aligned} s_1 &= \frac{1}{N}\left[\sum_{i=1}^{N} seq_i - y_i\right] - \frac{1}{N}\left[\sum_{i=1}^{N} seq_i - y_i\right]^* \\ &= 4Q\Delta p \pm \frac{4}{N} \end{aligned} \tag{1}$$

where Δp is the integrator pole error and N the number of averaged samples.

The behaviour of a 1^{st} order modulator is strongly driven by non-linear dynamics. This implies that a z-domain analysis using the approximation of a linearized quantizer cannot be performed. It has been shown in [15] that the 1^{st} order modulator output bit-stream follows exactly the input, when that input is a digital sequence. This behaviour is even strengthened by integrator pole error. Hence, a slightly different test was necessary for 1^{st} order modulators. The proposed test consists in adding an extra delay in the feedback loop of the modulator (in the digital part of the loop), and using as a test stimulus a digital periodic sequence formed by a number $M-1$ of 1s and a single -1. The sequence period M has to be strictly higher than 5. For instance, a sequence of period $[1\ 1\ 1\ 1\ 1\ -1]$ could be used. Notice that the extra delay is introduced only during test mode and does not impact the modulator nominal behavior. Under these conditions, it can be shown that the integrator output follows a fixed pattern. An integrator pole error manifests as a slow exponential-like decay of the pattern. It can be shown that such decay causes periodic transitions in the integrator pattern and that such transitions cause a deviation in the mean value of the modulator output. Hence, the test signature is computed in the same way as for the 2^{nd} order modulator, giving in this case,

$$\begin{aligned} s_2 &= \frac{1}{N}\left[\sum_{i=1}^{N} seq_i - y_i\right] - \frac{1}{N}\left[\sum_{i=1}^{N} seq_i - y_i\right]^* \\ &= \frac{4\Delta p}{ln\left(\frac{3M-5}{M-5}\right)} \pm \frac{4}{N} \end{aligned} \tag{2}$$

C. Integrator settling error test

For the proper behavior of a $\Sigma\Delta$ modulator, the dynamics of the amplifiers are also of utmost importance. Indeed, improper settling will cause a noise increase in the base-band and also harmonic distortion. In [16], a test has been proposed to measure such settling errors. However, such test required some slow arithmetic operation to build the signature. A modification was later introduced [12] such that the same signature elaboration as for the leakage test can be used.

A digital sequence, preferably of mean value 0, is sent to the integrator under test. Moreover, the modulator master clock is modified such that the clock period is doubled when a logic 0 is sent and remains nominal when a logic 1 is sent. In this way, it can be shown that the integrator settling error that occurs for a step corresponding to a logic 1 input sample and a logic 0 feedback sample can be referred as a DC level at the modulator input. To get rid of possible offset contributions, another acquisition has to be performed with the same test sequence but inverting the clock period modification (double for a logic 1 and nominal for a logic 0). As demonstrated in [12] the signature can be written as,

$$s_3 = \left(P_2 + P_{-2}^*\right) \times er_2 \pm \frac{4}{N} \tag{3}$$

where er_2 is the settling error under test (normalized to the modulator full-scale) and P_2 and P_{-2}^* are the probability of occurrence of having a 1 input sample and a 0 feedback sample (for the 1^{st} acquisition) or a 0 input sample and a 1 feedback sample (for the 2^{nd} acquisition), respectively. Using a random digital sequence as an input allows to estimate a-priori the term $\left(P_2 + P_{-2}^*\right)$ as being equal to $1/2$. The signature thus simplifies to,

$$s_3 = \frac{1}{2} \times er_2 \pm \left(\frac{4}{N} + 3er_2\sqrt{\frac{N}{2}}\right) \tag{4}$$

The error term in the expression of the signature is increased with respect to (3) by the 3σ contribution of the approximation of the actual value of the term $\left(P_2 + P_{-2}^*\right)$ to $1/2$.

III. Time-precision trade-off

For the digital tests summarized above, the signatures represent a measurement of the DC level deviation of the modulator output bit-stream from the expected value. This measurement can be performed by simple counters for the sake of hardware simplicity in a BIST focus. However, a simple counter is a 1^{st} order filter, which is obviously not optimum to remove the shaped quantization noise of a $\Sigma\Delta$ modulator. Actually, according to (1), (2) and (4), the precision on the different signatures is always in the order of $\pm 4/N$, where N is the number of averaged samples.

As our purpose is to retrieve the DC component of the output bit-stream, we should ideally select the sharpest filter with the lowest cut-off frequency. One drawback is the increased complexity, which may not be a limiting factor if the filter is implemented in an ATE. But a major concern is test time. Indeed, the filter order (and thus sharpness) and cut-off frequency are closely linked to the filter settling time. As a matter of fact, it is usually considered that an order $L+1$ is sufficient to properly filter a modulator of order L [13]. The proposed tests apply to 1^{st} and 2^{nd} order sections, so filters of order greater than 2 and 3 respectively would be more suitable to build the signature than simple counters. For the sake of simplicity, we will limit our study to comb filters, which are widely used to remove quantization noise in $\Sigma\Delta$ modulators [17]. The transfer function of a comb filter of order $L+1$ is,

$$H(z) = \left(\frac{1 - z^{-\frac{f_s}{2f_c}}}{1 - z^{-1}} \right)^{L+1} \tag{5}$$

where f_s is the modulator sampling frequency and f_c is the filter cut-off frequency. The oversampling ratio (OSR) is related to the filter cut-off frequency by,

$$OSR = \frac{f_s}{2f_c} \tag{6}$$

For such a filter, the number of samples required for proper settling is,

$$N_{set} = (L+1) \times \frac{f_s}{2f_c} \tag{7}$$

For an ideal modulator of order L, under the assumption that Bennetts conditions [18] are fulfilled, the transfer function can be written as,

$$Y = z^{-L}X + \left(1 - z^{-1}\right)^L E \tag{8}$$

where Y is the output bit-stream, X the input signal, and E is a random variable that represents the linearized quantizer error. Its variance is,

$$\sigma_E^2 = \frac{\Delta^2}{12} \tag{9}$$

where Δ is the quantizer step ($\Delta = 2$ for one-bit quantizer). For an ideal filtering, the quantization noise in the baseband can be calculated as,

$$\sigma_{noise}^2 = \frac{\pi^{2L}\sigma_E^2}{(2L+1)\left(\frac{f_s}{2f_c}\right)^{2L+1}} \tag{10}$$

Provided that two acquisitions have to be performed to get rid of the offset, the variance of the test signature should be twice that of a single acquisition.

A. The first order ΣΔ case

In what has been exposed previously, it has been assumed that the quantization noise is a random variable, shaped to high frequency. While this is a common assumption to describe ΣΔ modulators under normal operation, its validity range may not extend to the proposed tests. Indeed, the stimuli are not low-frequency continuous waves but digital sequences with short periods.

It is demonstrated in [15] that the response of an ideal 1^{st} order modulator to a digital sequence is the same digital sequence: in other words, there is no noise-shaping. Moreover, it has been shown in [11] that, during the leakage test, the output bit-stream follows a fixed pattern of the same mean value as the test sequence but twice the period. Integrator leakage perturbs this pattern and introduces periodic transitions that modify the overall DC level. Fig.4 shows the integrator output for a simulation of a leakage test for a 1^{st} order ΣΔ modulator with a pole error $\Delta p = 5.10^{-3}$. Notice that the modulator output bit-stream is actually the quantized version of the integrator output (i.e. its sign), but the effect of leakage

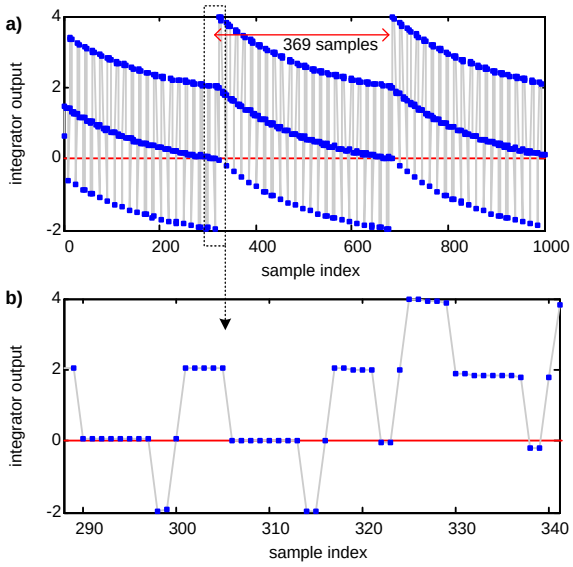

Fig. 4. Integrator output during a leakage test: a) over 1000 samples, the exponential decay of the envelope can be appreciated; b) the zoom on a transition shows how the repeating pattern is broken when the central level crosses 0

is best appreciated at the integrator output. The exponential decay of the envelope that can be seen in Fig.4-a) is due to leakage. When the central markers cross 0 a sharp transitions occurs. It can be seen in Fig.4-b) how the integrator output pattern is locally modified for a transition. The number of samples between two transitions has been shown to be,

$$N_s = \frac{ln\left(\frac{3M-5}{M-5}\right)}{\Delta p} \tag{11}$$

where M is the period length of the test sequence and Δp is the integrator pole error. In our case, for M=8 and $\Delta p = 5.10^{-3}$, we obtain $N_s = 369$, which is verified by the simulation. The filter has to sense more than one transition to retrieve the information of interest.

In order to illustrate this with experimental results, we performed a leakage test for the second stage of the prototype (which is a 1^{st} order modulator), with a test sequence of period $[1\ 1\ 1\ 1\ 1\ 0]$ and mean value $2/3$ (taking into account that the logic 0 is converted to an analog -1, normalized to the Full-Scale). A total number of 40000 samples were acquired for this sequence and its opposite. Then the output bit-streams have been post-processed using Matlab to study the use of several filters.

Fig.5 shows the evolution in time of the signatures obtained with a 2^{nd} order filter for 3 different values of the cut-off frequency: $f_s/288$, $f_s/720$ and $f_s/3240$. For the highest cut-off frequency, the filtering is not sufficient to average several transitions. Periodic peaks can be appreciated that correspond to the train of transitions (which is approximately a train of Dirac pulses) convoluted by the filter impulse response. For a cut-off frequency of $f_s/720$, the impulse response of the filter is of a length similar to the transition period and for the smallest cut-off frequency, the filtering is sufficient to

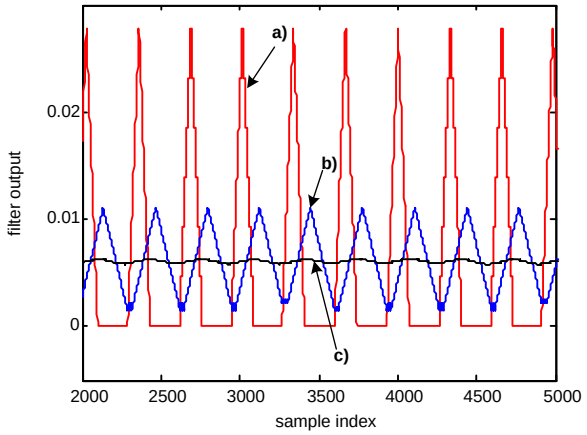

Fig. 5. Filter output for a 1^{st} order modulator leakage test at 3 different cut-off frequencies: a)$f_c = f_s/288$; b)$f_c = f_s/720$; c) $f_c = f_s/3240$.

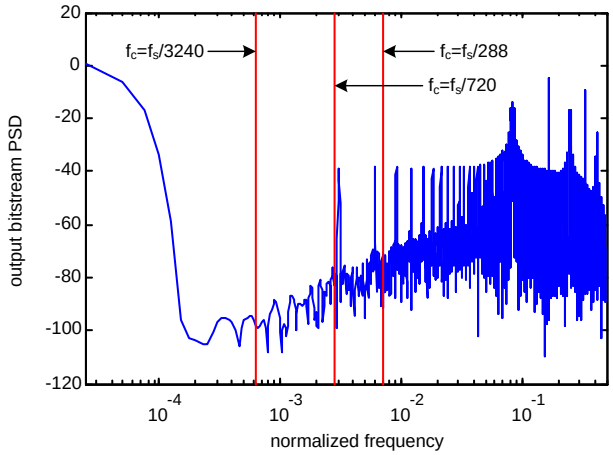

Fig. 6. Output bit-stream spectrum of a 1^{st} order modulator during leakage test. The filter cut-off frequency must be sufficient to remove the tonal components.

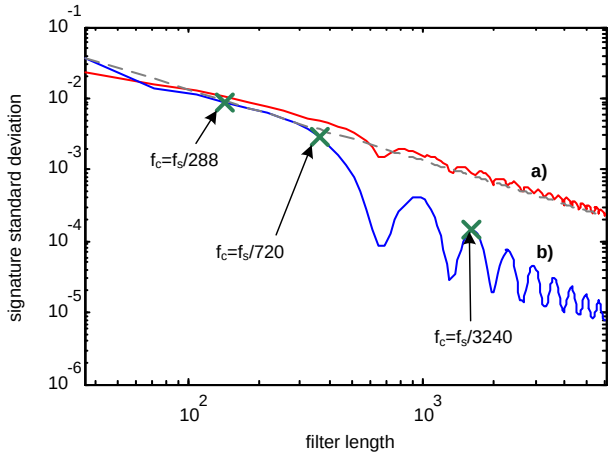

Fig. 7. Standard deviation of 1^{st} order modulator leakage test signature versus filter length: a) for a simple counter; b) for a 2^{nd} order filter

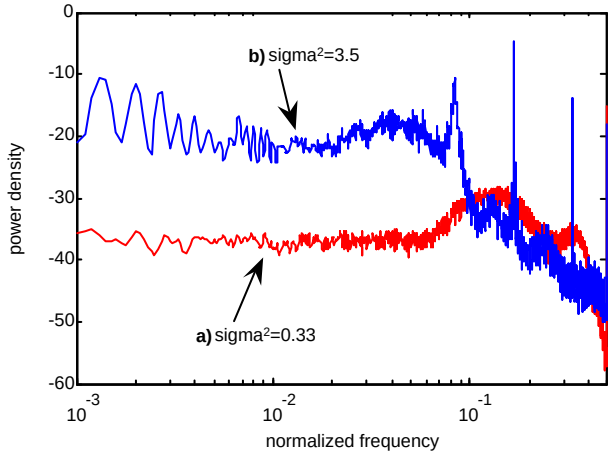

Fig. 8. Spectrum of the quantizer error E in a 2^{nd} order modulator: a) for a small DC input; b) for a digital sequence of mean value $Q = 2/3$

effectively remove the tonal contribution and isolate the DC component (i.e. the pole error information).

Fig.6 also illustrates the above effects, showing the normalized bit-stream spectrum together with the 3 filter cut-off frequencies. First of all, it can be verified from it that the base quantization noise is shaped, but is well under the tonal contribution that is due to the leakage-induced periodic transitions. Secondly, it can be verified that for $f_c = f_s/288$, some tones fall in the pass-band. The cut-off frequency $f_c = f_s/720$ is located close to the fundamental tone of the transitions and for $f_c = f_s/3240$, all the tones are filtered out. This is coherent with the time-domain observations commented above.

Finally, Fig.7 shows the signature standard deviation versus the filter impulse response length, for both a simple counter (case a) and a second order filter (case b). The 3 cases mentioned above are quoted on the figure with cross markers. It can be seen that for low filtering, the results of the simple counter and the 2^{nd} order filter are similar. Notice that the dashed line corresponds to the expected $4/N$ scaling for the simple counter. The standard deviation scaling significantly improves for the 2^{nd} order filter if the cut-off frequency of the filter is smaller than the transition frequency. As a conclusion of the above study, it can be said that, in order to design an efficient filter for the test signature, the procedure should be the following: i) estimate the minimum pole error that must be detected, ii) use (11) to evaluate the transition periodicity, iii) select a filter OSR higher than the transition period (for instance, the double).

B. The second-order ΣΔ case

In principle, the higher the modulator order, the more decorrelated is the quantization error from its input, which implies that the validity conditions for the linearization of the quantizer are fulfilled. Hence, it can be expected that the test signature improvement due to better filtering be noticeable for a 2^{nd} order modulator. In order to verify this assumption, we performed two high level simulations in Matlab: the first one for a 2^{nd} order modulator with a small DC input and the second one with a digital sequence input.

Fig.8 shows the spectrum of the quantizer error in the two cases. The linear model assumes that this error is a white noise of variance expressed as (9). It can be seen that the spectrum

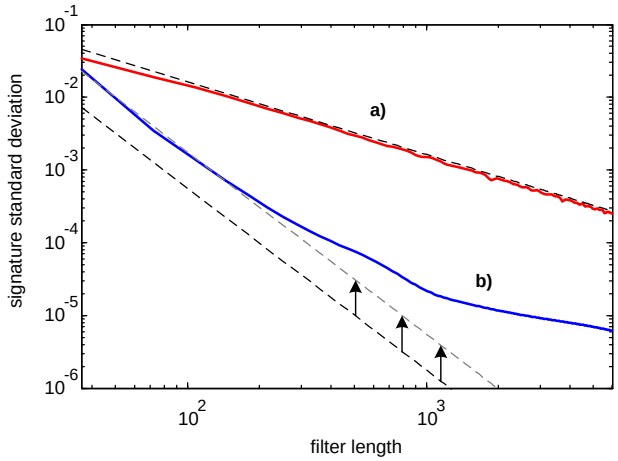

Fig. 9. Standard deviation of 2^{nd} order modulator leakage test signature versus filter length: a) for a simple counter; b) for a 3^{rd} order filter

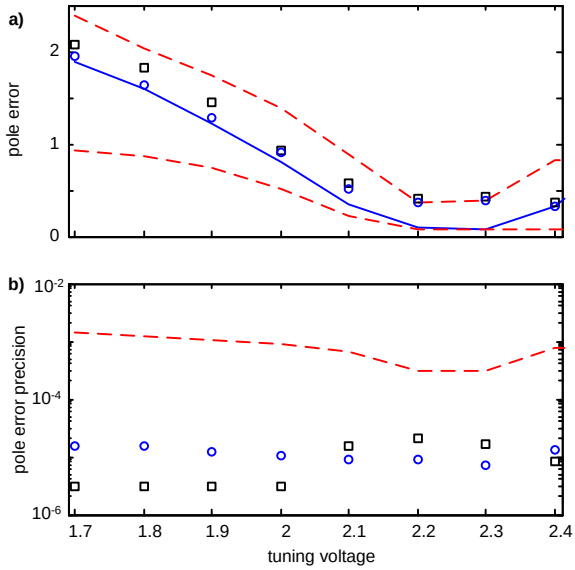

Fig. 10. a) Pole error versus amplifier tuning voltage; b) measurement 3σ dispersion and process corner variability

is truly white in none of the two cases but is reasonably random. What is more important is the value of the variance. For a small DC input, the simulation gives a variance of 0.33, which is very close to the expected value, while for the digital sequence, the quantizer is clearly overloading and the variance increases by an order of magnitude. As a result, this increased error should be taken into account in the linearized model during test and we should write it as,

$$\sigma_E^2 \approx 10\frac{\Delta^2}{12} \tag{12}$$

Fig.9 shows experimental results obtained for a leakage test of a second order modulator. Two acquisitions were performed over 40000 samples, with an test sequence of period $[1\ 1\ 1\ 1\ 1\ 0]$ and mean value $Q = 2/3$ (taking into account that the logic 0 is converted to an analog -1, normalized to the Full-Scale). On these two acquisitions, we varied the filtering options. First, we considered a simple counter (case a) and we varied the number of averaged samples. Next we applied a 3^{rd} order filter (case b) and varied the cut-off frequency (i.e. the OSR) and thus the impulse response of the filter. In both cases, the signature standard deviation can be derived once the filter has properly settled. The graph represents the obtained standard deviation versus the filter length (i.e. the settling time). The dashed lines correspond to the expected value. For a simple counter, the agreement is almost perfect. For the 3^{rd} order filter, the trend is the expected. The lowest dashed line corresponds to limit given by the ideal expression with (9), while the upper one corresponds to the increased variance due to quantizer overloading derived by simulation (12).

Finally, for filters of high length (i.e. low cut-off frequency), it can be seen in Fig.9 that the rate of the signature standard deviation scaling with filter length is lower than expected. Indeed, at some point that depends on the actual performance of the modulator under test, white thermal noise dominates over quantization noise. In any case, it can be seen how the signature standard deviation for a 3^{rd} order filter is significantly lower than that of the signature with a simple counter of same length.

C. Diagnosis capability

The proposed tests allow to digitally measure important design variables of all the integrators in a 2^{nd} order and a 1^{st} order modulator, or any cascaded combination of such stages. Moreover, adequate filtering leads to a signature precision that enables the localization of the modulator in the design space, which can be very valuable for diagnosis and silicon-debug, and thus for yield learning.

This subsection tries to demonstrate it with our prototype. We vary the tuning voltage of the amplifiers in order to induce parametric deviations and perform the proposed tests on the three integrators. In order to validate the measurements against a reference, we also performed electrical simulations of the integrator to determine the expected leakage and settling error as function of the tuning voltage. Furthermore, we repeat these simulations for the different process corners.

Fig.10-a) shows the evolution of the integrator pole error as a function of the tuning voltage. The solid line corresponds to the electrical simulation of the typical mean corner, while the dashed lines represent the maximum and minimum values reached by the different process corners. The round markers stand for the pole error measured for the 1^{st} integrator (in a 2^{nd} order modulator configuration), while the square markers stand for the pole error measured for the 2^{nd} and the 3^{rd} integrators. Indeed, these integrators are identical and are both measured in a 1^{st} order modulator configuration and hence produce the same results.

The dashed line on Fig.10 b) represents the process variability (i.e. it corresponds to the difference between the two dashed lines in Fig.10 a). The markers show the measurements 3σ precision. The square markers are obtained for the 2^{nd} and the 3^{rd} integrators with a 2^{nd} order filter of cut-off frequency $f_s/9000$. The round markers are obtained for the 1^{st} integrator

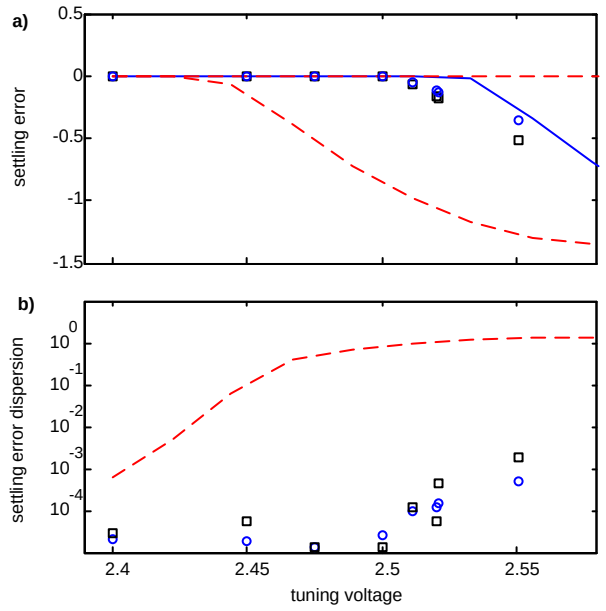

Fig. 11. a) Settling error versus amplifier tuning voltage; b) measurement 3σ dispersion and process corner variability

with a 3^{rd} order filter of cut-off frequency $f_s/2000$. It can be seen how in both cases the measurement 3σ dispersion is between 1 and 2 orders of magnitude below the process variability, even in the worst case (i.e. for the smallest pole error).

Fig.11 shows the same graphs obtained for the settling error. The cut-off frequencies are the same as for the leakage tests. Here again, it can be seen how the settling error tests reach a precision that is close to 2 orders of magnitude below process variability, even for the small settling error obtained for a tuning voltage of 2.4V.

Let us study how much test time is necessary to obtain this diagnosis capability. Four acquisitions are necessary for each integrator (two for leakage test and two for settling test). However, we can consider that the test of the 2^{nd} and the 3^{rd} integrators can be performed in parallel because they involve different $\Sigma\Delta$ stages (see Fig.2). Taking into account that the filter settling time is related to the cut-off frequency though (7), the total number of samples required to perform the proposed tests on the 3 integrators is thus,

$$N_{samples} = 4 \times 3 \times 2000 + 4 \times 2 \times 9000 = 96000 \quad (13)$$

Notice that the filtering is performed in real-time and there is thus no more post-processing than the subtraction of the two acquisitions results for each test. The time needed to load the modulator configuration filter can be neglected with respect to the acquisition time. Moreover, as the test stimulus is purely digital, no additional settling time has to be considered. The acquisition time is thus a good approximation of the total test time by,

$$T_{test} = \frac{N_{samples}}{f_s} \quad (14)$$

where f_s is the modulator sampling frequency. This is quite competitive with respect to functional tests that do not offer the same diagnosis capability. Indeed, for an OSR of 100, a single FFT over 1024 samples would require the acquisition of roughly 102400 samples. This number is comparable to our result but FFT requires important post-processing and non-negligible setup time. Indeed, as shown in [19], the test time for FFT-based tests is not dominated by acquisition time but by other factors like setup time, data transfer time and FFT-processing time. In this reference, the actual test time is 93ms. Our prototype uses a quite slow sampling frequency of 2MHz. The test time for 96000 samples would be of the order of 50ms, which is still lower than the 93ms of an FFT test. For the same modulator working at 20MHz, the test time would scale down to 5ms. Finally the digital nature of the proposal also enables massive parallel testing, which further reduces the effective test-time.

IV. DECIMATION FILTER RE-USE

In some cases, $\Sigma\Delta$ modulators are sold as stand-alone parts and the output bit-stream is directly accessible for test purpose. An optimum filter can thus be designed for each test, as explained in previous section. In some others, the $\Sigma\Delta$ modulator is integrated together with a decimation filter, and the output bit-stream is not directly accessible. This is not necessarily impairment, as this decimation filter can be used to build the test signatures if two conditions are met:

i) The settling error test requires that the modulator master clock be modified as function of the test sequence. This modified master clock must be used to drive the decimation filter.

ii) For cascaded modulator, the reconstruction filter must be configurable such that it can by-pass the output of the different stages directly to the decimation filter.

In what follows, we will study the possibility to build the test signatures with only one valid sample of the decimation filter for each acquisition. In such case, the test time would be determined by the settling time of the decimation filter, and in any case would be order(s) of magnitude below functional (FFT-based) test time.

In order to determine whether the decimation filter provides sufficient filtering, we will consider a functional criterion: the tests must be able to unambiguously detect the given parameter (pole error or settling error) even if the deviation does not imply performance degradation. In other words, the sensitivity of the proposed test to the targeted defect must be greater than that of a functional test.

It is well known that the performance of a $\Sigma\Delta$ modulator is much more sensitive to the performance of the 1^{st} integrator than to the integrators located further in the loop. The worst case for our study is thus to consider deviations in the 1^{st} integrator.

A. Leakage test versus functional test

Let us consider the case of a simple 2^{nd} order modulator. The leakage test signature for a second order modulator is given by (1). In order to be detectable at the output of

the decimation filter, the variation of the DC component (i.e. $4Q\Delta p_1$) must be greater than the signature precision. Moreover, the variance of the signature is twice the variance for a single acquisition, which is given by (10). The minimum detectable pole error can thus be determined as,

$$\Delta p_{min} = \frac{3\sqrt{2\sigma^2_{noise}}}{4Q} \tag{15}$$

Introducing (10) and (12) (with $\Delta = 2$) in (15), and taking into account that the decimation filter cut-off frequency is related to the OSR through (6), it comes,

$$\Delta p_{min} = \frac{3}{2Q}\sqrt{\frac{\pi^4}{3OSR^5}} \tag{16}$$

Furthermore, the amount of quantization noise that leaks into the baseband for a given pole error Δp can be calculated as,

$$P_{noise}(dB) = 10log\left(1 + \Delta p^2 \times \frac{OSR^2}{\pi^2} \times \frac{10}{3}\right) \tag{17}$$

Substituting Δp by Δp_{min} in (17), the minimum detectable leakage corresponds to a noise degradation of,

$$P_{min}(dB) = 10log\left(1 + \frac{5}{2} \times \frac{\pi^2}{Q^2 OSR^3}\right) \tag{18}$$

At the pole error detection limit, the noise degradation is higher for lower values of the OSR. However, even for a low OSR for instance 16, the decimation filter should be sufficient to detect a leakage that would cause a 0.06dB SNR loss with an input sequence of mean value $Q = 2/3$. This means that for a stand-alone second-order modulator, the decimation filter is sufficient to build an adequate signature with only one valid sample for each acquisition. The leakage test time reduces to twice the settling time of the decimation filter. For a cascaded modulator of order L, with a 2^{nd} order modulator as first stage, the quantization noise leaking into the baseband due to a pole error in the first integrator can be calculated as,

$$P_{noise}(dB) = \cdots \tag{19}$$
$$10log\left(\frac{\Delta_1}{\Delta_n}\left(1 + \frac{2\Delta p^2}{\pi^{2L-2}} \times \frac{OSR^{2L-2}}{d^2} \times \frac{2L+1}{3}\right)\right)$$

where Δ_1 and Δ_n are the quantizer step of the first and last stage, respectively; and d is a factor greater than unity that depends on the branch coefficients of particular cascaded architecture [20]. Substituting Δp by Δp_{min} in (19), the SNR loss associated to the minimum detectable pole error is,

$$P_{min}(dB) = \cdots \tag{20}$$
$$10log\left(\frac{\Delta_1}{\Delta_n}\left(1 + \frac{2L+1}{20d^2Q^2} \times OSR^{2L-7} \times \pi^{6-2L}\right)\right)$$

Here, things are different than for a 2^{nd} order modulator alone. Indeed (20) shows that the SNR loss associated to the minimum detectable pole error will increase with the OSR if the order of the cascaded modulator is higher than 3. For instance, taking $d = 2$, $Q = 0.5$ and $\Delta_1 = \Delta_n = 2$, it comes that the SNR loss associated to the minimum pole error detectable with the decimation filter at $OSR = 64$ would be 0.02dB for a 3^{rd} order modulator, 6dB for a 4^{th} order and 32dB for a 5^{th} order. Hence, it can be concluded that the detection of pole errors that have a significant impact on performance in cascaded modulator of order higher than 4 would require more filtering than the one provided by the decimation filter.

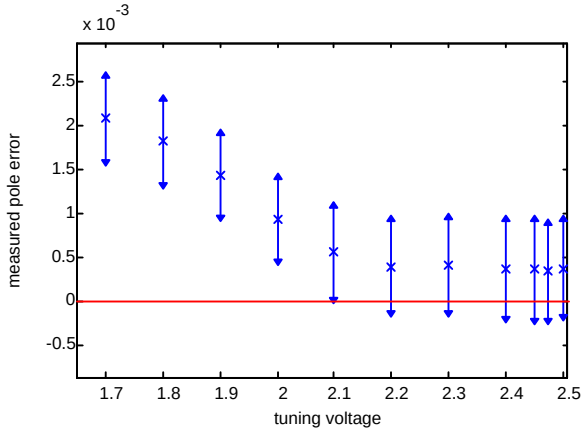

Fig. 12. Measured pole error versus amplifier tuning voltage, with the confidence interval corresponding to the 3σ dispersion of the signature taking a single sample of the decimation filter.

These results can be verified, at least partially, with our prototype. For that purpose we considered a 4^{th} order decimation filter, with an OSR of 50. The first valid sample is thus obtained after 200 modulator samples according to (7), which in our case corresponds to 0.1ms. Then, we have varied the tuning voltage of the amplifiers to induce parametric deviations. For each tuning voltage, we performed a leakage test with an input sequence of mean value $2/3$, and also a functional test. This functional test consists in sending a low-frequency sine-wave (1.6kHz) with an amplitude of 70% of the modulator Full-Scale and performing an FFT on the output of the decimation filter. Actually, the reconstruction and filtering is emulated in software, so we can perform the functional test on the complete 3^{rd} order modulator but also on the 1^{st} stage only, which is a 2^{nd} order modulator.

Fig.12 shows the pole error, evaluated with only one valid sample, for the different tuning voltages. The experimental 3σ confidence interval of the measurement is also displayed and is around 6×10^{-4}. It can be seen that for tuning voltages below 2.1V, the pole error is detected (because 0 is not contained in the confidence interval).

Fig.13 shows the modulator SNR as a function of the 1^{st} integrator pole error for a 2^{nd} order modulator (case a) and for a 3^{rd} order modulator (case b). The markers correspond to experimental result, that is to say the measured SNR versus the measured pole error. The curves correspond to high level Matlab simulations. The dashed line corresponds to a simulation without thermal noise, while the solid lines correspond to simulations with an additive Gaussian noise source of variance 8.3×10^{-6} at the modulator input, that we

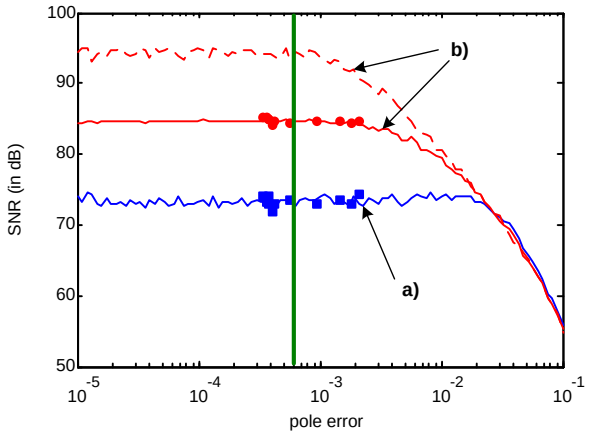

Fig. 13. Modulator SNR versus 1^{st} integrator pole error: a) for a 2^{nd} order modulator; b) for a 3^{rd} order modulator.

introduced to emulate the unexpectedly high level of white noise in the baseband (which may be due to quantization noise coupling to the references). Finally, the vertical line corresponds to the 3σ detection limit of 6×10^{-4} (the same as in Fig.12), which marks the unambiguous detection limit (called Δp_{min} in (15)). Accordingly to the dashed line, the maximum pole error that can be induced by the tuning voltage (of the order of 2.5×10^{-3}) should have been sufficient to see a 10dB degradation of the 3^{rd} order modulator SNR. Unfortunately, the presence of thermal noise in our setup lowers the nominal SNR and masks the expected degradation. Despite of this, it can be seen that the vertical line that marks the Δp_{min} limit intersect the curves on the plateau region before degradation. This means that, with only one valid sample (for each acquisition) of the decimation filter, our digital test is able to detect unambiguously the pole error better than a functional test. For a cascaded modulator of order higher than 3, additional filtering would probably be required, as the degradation limit would be pushed toward lower pole errors.

B. Settling error test versus functional test

The settling error of the first integrator can be referred to the modulator input and translates into a distortion term. For a DC input v, the first integrator is submitted to two levels as function of the feedback sample: level $v-1$ which is associated to a probability of $(1+v)/2$ and level $v+1$ which is associated to a probability of $(1-v)/2$. The expression of the deviation with respect to a straight transfer function as function of the DC input v is thus,

$$d(v) = \frac{1+v}{2} er(v-1) + \frac{1-v}{2} er(v+1) \qquad (21)$$

where $er(x)$ is the integrator settling error for a given input x. This expression can thus be seen as the contribution of the integrator settling error to the modulator INL. It could be thought that the maximum distortion should be obtained for the maximum integrator settling error but this is not the case. The settling error for an integrator input of 2 (obtained for an input sample of value 1 and a feedback sample of value -1) is the highest one, but the probability of occurrence of a level 2 at the integrator input tends to zero. Actually, experience says that the INL curve of $\Sigma\Delta$ modulators is usually close to a 3^{rd} order polynomial. The location of its maximum and minimum depends on the modulator but a value of 2/3 of the full-scale is a good example. In this case, the maximum INL could be evaluated as,

$$\begin{aligned} INL_{max} &= d\left(\frac{2}{3}\right) \\ &= \frac{5}{6} er\left(\frac{-1}{3}\right) + \frac{1}{6} er\left(\frac{5}{3}\right) \\ &\approx \frac{1}{6} er\left(\frac{5}{3}\right) \end{aligned} \qquad (22)$$

In a first approximation it can be considered that the integrator settling error associated to a -1/3 integrator input level is order(s) of magnitude smaller than the settling error associated to a 5/3 input level.

For a settling error test performed with a random input sequence, it has been seen that the DC component in the signature was of the form,

$$s = \frac{1}{2} er\,(2) \qquad (23)$$

The higher the integrator input, the higher the settling error. Hence, using (22) we can write,

$$\left(er(2) > er\left(\frac{5}{3}\right)\right) \Leftrightarrow (s > 3INL_{max}) \qquad (24)$$

For the signature to unambiguously detect a settling error it must be greater than 2 effective LSB (Least Significant Bit) — one for each acquisition. Similarly, if the INL is high enough to impact the ADC it implies that the maximum INL be greater than 1LSB effective. Hence we can write,

$$s > 3INL_{max} > 3LSB \qquad (25)$$

For a single loop modulator, the LSB during the test is the same as the LSB of the overall modulator, and taking only one valid sample of decimation filter would thus be sufficient to build the settling error test signature. Once again, the results are different for a cascaded modulator, as the effective LSB obtained for the first stage alone is not the same as the overall modulator LSB. Even though, an adequate filtering can be calculated such that the 3σ uncertainty is smaller than one LSB of the overall modulator.

In the same way as for the leakage test, Fig.14 shows experimental results of the measured settling error of the first integrator, versus the tuning voltage. Here again, the signature is computed using only one valid sample of the 4^{th} order decimation filter (of $OSR = 50$). A zoom inset has been added to make visible the measurement uncertainty range on an adequate scale. It can be seen that for voltages above 2.5V, the settling error is unambiguously detected since the 0 line does not fall within the uncertainty range. The 3σ uncertainty is around 2×10^{-3}.

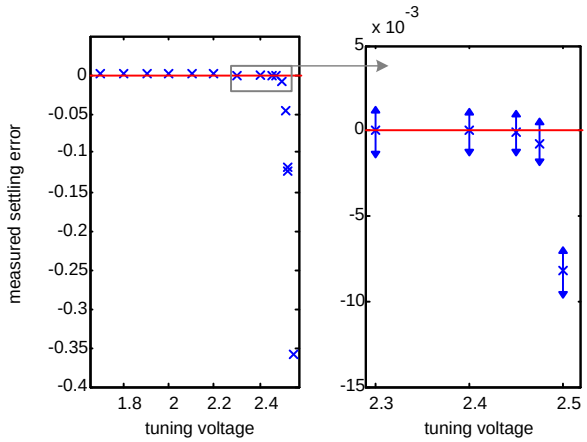

Fig. 14. Measured settling error versus amplifier tuning voltage, with a confidence interval corresponding to the signature 3σ dispersion taking a single sample of the decimation filter

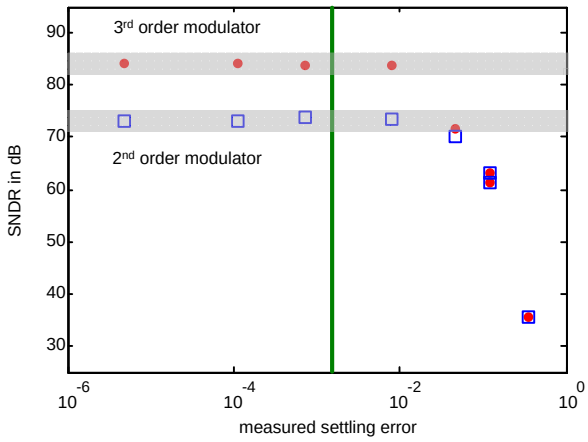

Fig. 15. Modulator SNDR versus 1^{st} integrator settling error, for both the complete 3^{rd} order modulator and the 1^{st} stage alone.

Fig.15 shows the measured Signal to Noise and Distortion Ratio (SNDR) for the first stage (a 2^{nd} order modulator) and for the complete 3^{rd} order cascaded modulator, versus the measured settling error.

For the SNDR measurement, an FFT was performed on 40000 samples of the output bit-stream, which corresponds to 800 samples in the baseband for an OSR of 50. A type-2 Rife-Vincent window was used to avoid spectral leakage. The gray rectangles indicate the $\pm 3\sigma$ dispersion of the SNDR measurement.

The vertical line corresponds to the 3σ detection limit obtained for a signature taking only one sample of the decimation filter. Hence, all the settling error on the right side of the line would be unambiguously detected.

It can be seen how, for both cases, the proposed test can detect a settling error in the 1^{st} amplifier even at values that do not affect the performance, since there is a data point that falls within the gray rectangle of the fault-free SNDR uncertainty range but on the right side of the settling error detection limit.

So it can be concluded that for single loop-modulators, one sample of the decimation filter should be sufficient to build the test signature and retrieve information of any deviation

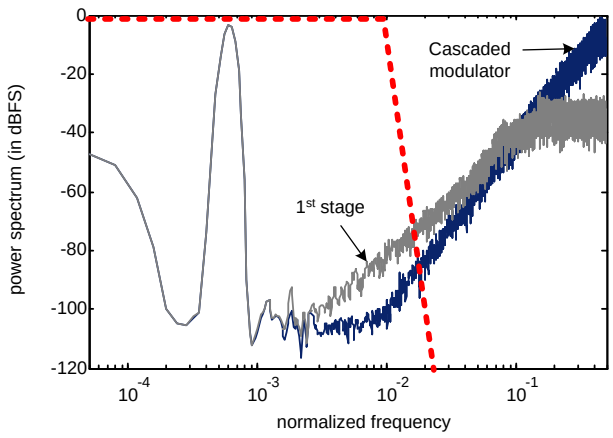

Fig. 16. Power spectrum of the cascaded modulator and its first stage

that could affect performance, while for cascaded modulators, further filtering may be required (specially for modulator orders higher than 3).

A modulator of order L contains L integrators. Considering that each integrator is tested for leakage and settling, that each test requires two acquisitions and that the decimation filter is of order $L+1$, the complete acquisition time can be evaluated as,

$$T_{acq} = \frac{4OSR}{f_s} \times L \times (L+1) \tag{26}$$

In our case, the test of the three integrators would thus require 60 decimation filter samples (i.e. 3000 modulator samples) for a test time of 1.5ms, which is negligible with respect to a functional test time of close to 100ms.

V. Discussion

The filtering provided by the decimation filter is not programmable in the majority of cases. This means that the signatures derived from only one valid sample will have a given precision that may or may not be sufficient.

For single loop modulators, the decimation filter is designed to reach a given precision and usually removes most of the quantization noise. We have seen in previous section that this filter should be adequate for test purpose with a functional test criterion in mind. However, a higher precision may be desired to improve diagnosis capability and to provide more accurate information for silicon debug or yield learning.

High-order cascaded modulators can reach a high precision even with a low OSR. As a consequence, it is possible that the decimation filter designed for the complete cascaded modulator could not be adequate to filter the quantization noise of a single stage in test mode. The filter order (i.e. sharpness) will be higher than strictly necessary and this is not an issue, but the cut-off frequency is possibly too high. This is sketched in Fig.16, which represents the power spectrums of the 1^{st} stage and of the cascaded modulator for our prototype for an input sine-wave. The dashed line shows how a filter designed to remove most of the quantization noise for the cascaded modulator can let some quantization noise unfiltered when applied to a single stage.

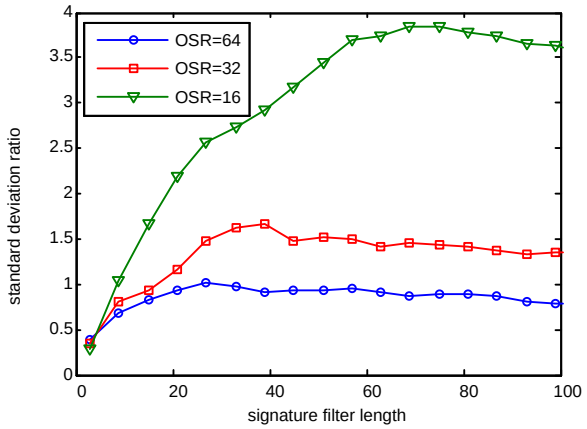

Fig. 17. Counter to 3^{rd} order filter signature precision ratio (σ_1/σ_3), as a function of the filter length

If a higher signature precision is desired, the decimation filter output has to be filtered further. The next question is how. Is it sufficient to simply average some samples? Or on the contrary is it worth implementing a higher order filter? We can postulate that if the shaped quantization noise is not significant with respect to other sources like thermal noise, averaging several samples (i.e. a 1^{st} order filter) will be more adequate than a higher order filter, because for a given number of samples a lower cut-off frequency can be obtained. On the other hand, if the shaped quantization noise is the dominating factor in the signature precision, a filter of higher order is likely to provide better results.

In order to illustrate this fact, Fig.17 presents experimental results obtained for the leakage test of the first stage of our prototype. A number of 40000 samples of the output bit-stream is acquired. Provided that the complete modulator is a 3^{rd} order, we then emulate in Matlab a decimation filter of order 4, for various $OSRs$. On the decimation filter output, we then perform additional filtering: in one case we simply average N samples (obtaining a signature standard deviation quoted σ_1) and in the other we use a 3^{rd} order comb filter of length N (obtaining a signature standard deviation quoted σ_3). The figure represents the ratio σ_1/σ_3 as a function of the additional filter length. It can be appreciated how for low OSR (both 16 and 32) there is still a large amount of shaped quantization noise in the decimation filter output. For that reason, a 3^{rd} order filter is more efficient than a counter and the ratio is well above 1. On the contrary, for a larger OSR of 64, the thermal noise is dominating and a simple counter outperforms a 3^{rd} order filter.

VI. Conclusion

It has been shown in this paper how simple digital tests can be integrated in a production test flow for cascaded $\Sigma\Delta$ modulators. These digital tests measure important design parameters, namely the pole and settling error of all the integrators, bringing an interesting complement to functional test. Indeed, they can be very valuable for low-cost wafer-level screening test, including at-speed and burn-in tests.

It has been shown how to tailor signature generation, which relies on the measurement of a DC component in the stages output bit-streams, in order to reach a given precision.

Hence, the proposed tests can provide valuable data for silicon debug, locating the DUT in the block-level design space with a precision greater than corner variability. This is a valuable feature for the future design paradigm where device variability is seen to be prevalent.

Moreover, the signature precision study has been carried out with test time minimization in mind. The experimental results show that test time is almost reduced to data acquisition time and is much lower than traditional FFT-based functional tests. The test cost is further reduced by the digital nature of the proposed tests that opens the door to parallel testing on low-cost digital testers.

Acknowledgment

The authors would like to thank the reviewers for their careful revision and their very constructive comments.

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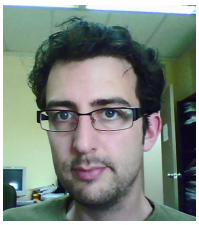

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