# OBT for settling error test of sampled-data systems using signal-dependent clocking

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***Abstract*—This work presents a modification of traditional Oscillation-Based Test schemes for sampled-data systems. This new test scheme is based on doubling the sampling frequency when the oscillation changes its sign. This way, the DC level of the output oscillation signal becomes a simple signature sensitive to the settling errors in the device under test and to its oscillation features. The proposed technique is illustrated on a switched-capacitor second-order lowpass filter. This case study is used to show the sensitivity of the proposed signature to the linearity of the DUT. Electrical simulation results are provided to validate the proposal.**

## I. Introduction

Nowadays, commercial trends of IC industry have forced the integration of complex SoCs consisting of tightly integrated analog, mixed-signal, and digital circuitry onto a single IC substrate. This high integration level provides a significant reduction in production cost, but there is a simultaneous increase in the cost of testing and diagnosing these devices [1], [2].

Testing non-digital cores embedded in a SoC represents a challenging task. A direct test of a non-digital block is based on the application of precise test patterns to the DUT and the analysis of its response. This usually requires the use of expensive external test equipment and the provision of an adequate test access to internal nodes of the SoC. However, the increase in integration capabilities turns these requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals from the chip to the external tester.

Moving some of the test resources inside the chip may be a way to overcome these issues. This is why BIST (Built-in Self-Test) approaches should be so interesting if made feasible. Manipulations would remain internal, transport problems would be eliminated, test interface would be simplified, and the need of expensive external test equipment would be reduced. A potential shortcoming of BIST strategies is that they have to be provided at a low overhead with respect to the original DUT. Otherwise they would not be advantageous.

In this framework, OBT (Oscillation-Based Test) has been proposed as a low-overhead technique suitable for the on-chip test of diverse analog and mixed-signal cores [3]–[7]. Oscillation-based test relies in forcing oscillators either in a circuit or in a full system. The DUT is reconfigured by any means into an oscillator, and the resulting oscillation is characterized. Correct operation of the DUT can be inferred from the characteristics of its oscillation.

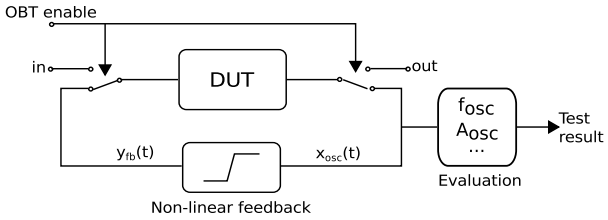


Fig. 1. Block diagram of traditional OBT

This work proposes a low-cost modification of traditional OBT for sampled-data systems by using signal-dependent timing during the oscillating mode. The idea of using signal-dependent timing is adapted from previous work by the authors for testing the dynamic performance of $\Sigma\Delta$ A/D converters [8]. This variable timing is implemented by changing the sampling frequency when the oscillating signal changes its sign. The goal of this paper is to demonstrate that the DC level of the resulting asymmetric oscillation becomes a simple signature for testing sampled-data systems, sensitive to settling errors in the DUT, and that can replace the traditional amplitude-frequency pair of measurements for evaluating oscillation-based tests with a lower test overhead.

This paper is organized as follows. Firstly, Section II reviews previous OBT strategies. Then, Section III discusses the theoretical basis of our proposal. Section IV presents an example of implementation using a fully-differential second-order lowpass SC filter as DUT. Section V provides some relevant experimental results to validate the proposal. Finally Section VI summarizes the main contributions of this work.

## II. Brief review of traditional OBT strategies

Traditional Oscillation-Based Test is based on converting the DUT into a sinusoidal oscillator during test mode by providing an appropriate feedback path. Fig. 1 illustrates a typical example of OBT application. The DUT in Fig. 1 is detached from the signal path during test mode and set to oscillate by adding a saturating gain block in feedback. OBT was initially proposed as a structural testing framework [3]. The key premise in this structural framework is that any fault

in the DUT changes its oscillation features in comparison to the fault-free circuit. Oscillation features that can be monitored for fault detection include frequency, amplitude, dc level, distortion, and so on. It has been demonstrated that monitoring multiple oscillation characteristics increases fault coverage [7], but it also increases the overhead. Hence, many OBT proposals are limited to the observation of the oscillation frequency and, in some cases, its amplitude.

This is the main potential issue of OBT. Relying in the monitoring of a single observable (or a very reduced set of observables) compromises fault coverage, and furthermore, makes nearly impossible the location of the faults.

Another potential issue is common to other structural approaches for non-digital circuits: circuit integrity does not guarantee the fulfillment of the specifications. Predictive OBT (POBT) has been proposed as a solution to bring the advantages of OBT to a functional test framework [9]–[13]. POBT makes use of statistical post-processing tools to predict functional specifications of the DUT from its oscillation features in test mode. POBT offers a promising solution, but it has some serious drawbacks that have to be addressed. The information contained in the oscillation, as commented before, is very limited. Hence, mapping this limited information into a wide set of specifications may be difficult. Furthermore, the oscillation features are fixed by the sinusoidal oscillation regime itself and cannot be controlled. In essence, this can be seen as a DUT tested using only one test pattern, which in the end also limits the information that can be extracted.

Many practical POBT strategies address this issue by adding other set of observables to complete the information contained in the oscillation. Thus, the work in [9] adds supply current monitoring to the measurement of oscillation characteristics, while the work in [10] adds the measurement of oscillation features at different internal nodes of the DUT. The proposal of Complex OBT (COBT) in [12], [13] also follows this trend by the exploitation of chaotic oscillation regimes, which is roughly equivalent to exciting the DUT with spectral-rich test patterns.

This work explores a low-overhead modification of traditional OBT for sampled-data systems that can be used to improve fault coverage and mapping models. We propose a simple modification of the sampling clock during the oscillating test mode. The sampling clock frequency is made signal dependent and changes when the oscillation changes sign. As it will be shown, this simple modification will lead us to the definition of a signature sensitive to the settling error of the DUT and to its oscillation features.

## III. Theoretical basis

### A. Settling error in sampled-data systems

Before presenting the proposed OBT modification, it is convenient to review the concept of settling error in sampled-data systems. In order to simplify the discussion, it will be illustrated using the switched-capacitor integrator in Fig. 2. The selected SC integrator is a basic building-block for many switched-capacitor circuits, and the obtained results can

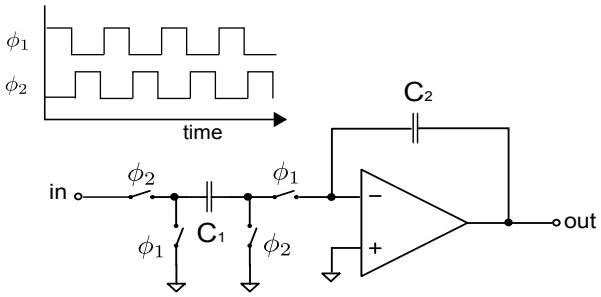


Fig. 2. Switched-Capacitor integrator

be extended to other more complex systems. Ideally, this integrator performs a cumulative sum: its output at instant $n$ is the sum of the output and the input at instant $n-1$. Settling error can be defined as the deviation from this ideal behavior due to non-ideal dynamic performance of the integrator.

A commonly used approximation to study the dynamic behavior of an integrator with a non-ideal settling is the one-pole approximation, together with a maximum current limitation for the amplifier. In that model, the settling of the amplifier is determined by two parameters: its Gain-Bandwidth product, $GBW$, and its Slew-Rate, $SR$. For the sake of readability, time and frequency are normalized to a sampling frequency of 1, that is,

$$\begin{aligned} T_s &= 1 \\ \widehat{SR} &= SR \times f_s \\ \widehat{GBW} &= GBW \times f_s \end{aligned} \tag{1}$$

where $\widehat{SR}$ and $\widehat{GBW}$ are the conventional slew-rate and gain-bandwidth product, $f_s$ is the sampling frequency. Parameters $SR$ and $GBW$ are time-normalized versions of the slew-rate and gain-bandwidth product, respectively. Let us consider the integrator in Fig. 2. Let $V_i$ be the voltage stored on capacitor $C_1$ at time 0, and $V_o$ the integrator output at the end of the integrating phase, that is, at time $T_s/2$. Three regions of operation can be considered, depending on parameter $t_0$ defined as:

$$t_0 = \frac{b|V_i|}{SR} - \frac{1}{2\pi GBW} \tag{2}$$

where $b = C_1/C_2$ is the integrator gain. Phenomenologically, $t_0$ indicates the time at which the amplifier stops slewing.

- In the first region, with $t_0 < 0$, the input voltage is sufficiently small such that the amplifier does not slew. The settling is then determined only by the GBW and is exponentially shaped. It can be described as,

$$V_o = V_{o,n-1} + bV_i(1 - e^{-\pi GBW}) \tag{3}$$

  It is easily seen that the settling error is proportional to the input voltage, and increases with the sampling frequency.
- In the second region, where $t_0 > 1/2$, the input voltage is so high that the amplifier slews over the whole integrating phase. The output voltage can be written as,

$$V_o = V_{o,n-1} + \frac{SR\,\mathrm{sign}(V_i)}{2} \tag{4}$$

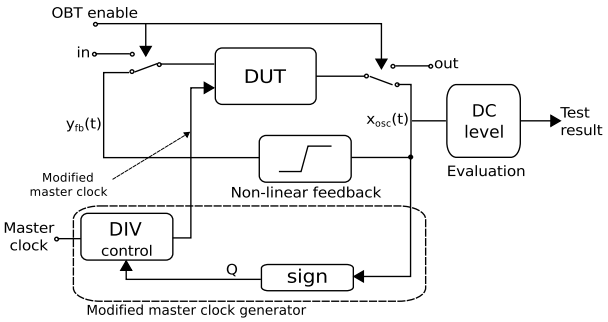


Fig. 3. Block diagram OBT mod

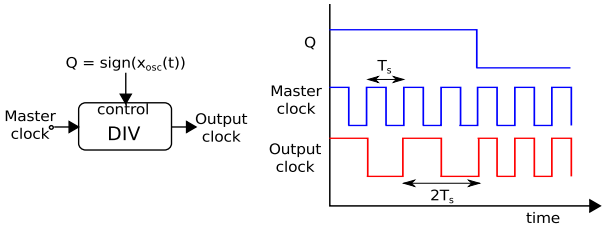


Fig. 4. Modification of the DUT clocking

Such a settling error is clearly non-linear, as the integrator output does not depend on the exact value of the input voltage.

- The last region is the intermediate zone between the previously described ones, with $t_0 \in [0, 1/2]$. The amplifier begins to slew but manages to return to the exponential settling at some point. In this case, $V_o$ can be described as

$$V_o = V_{o,n-1} + SR\,\text{sign}(V_i)\,t_0 + (bV_i - SR\,\text{sign}(V_i)\,t_0)\left(1 - e^{-2\pi GBW(1/2-t_0)}\right) \quad (5)$$

Here the settling error is non-linear but the output voltage still depends on the input.

Equations (2)–(5) model the settling behavior of the integrator. A more realistic approach should consider also the amplifier finite DC gain and output impedance, as well as parasitic and load capacitances, charge injection phenomena, etc. However this analysis gives sufficient insight to describe the operation principle of the proposed test.

### B. Modified OBT for settling error test

Based on the previous discussion, it is straightforward to conclude that the settling error increases with the sampling frequency. The proposed OBT modification consists in varying the sampling frequency as a function of the oscillating signal to produce a DC component in the oscillation sensitive to this settling error. The main motivation is that it is simpler to acquire a DC component than analyzing spectral content.

Fig. 3 shows a simplified block diagram of the proposed OBT modification. The system master clock is fed to a programmable frequency divider, labelled DIV in Fig. 3. This block has a control input driven by the sign of the oscillating output $x_{osc}(t)$. The implementation of this block will be detailed in the next section. This digital block modifies the clocking of the DUT such that when the sign of the oscillation is positive (or conversely negative), the clock phases last $k$ times as much as when the sign of the oscillation is negative (or conversely positive). Notice that only the master clock is actually modified: the generation of non-overlapping phases remains unaltered. Fig. 4 shows an example of the clock modification for $k = 2$.

Switched-capacitor circuits are governed by the charge packets that flow through the capacitors at each switching event. They are thus event-based circuits. The described operation does not modify the oscillation regime because, to a first-order, it does not depend on the duration of the signal samples. This affirmation is, however, difficult to prove analytically given that the oscillation regime depends on the dynamic of each particular system. Empirical observation over particular SC filters suggests that this statement is true for low values of $k$, while the oscillation may become unstable for large values of $k$ ($k \gg 10$).

Alternating a "fast" clock and a "slow" clock when the oscillation changes its sign, different settling behaviors can be observed within one oscillation period. Furthermore, the DC component of the oscillation can be used as a simple test signature. The proposed signature, $S$, is defined as

$$S = \frac{1}{M\,T_{osc}} \int_0^{M\,T_{osc}} x_{osc}(t)\,dt \quad (6)$$

where $M$ is an integer number of oscillation periods, $T_{osc}$ is the oscillation period, and $x_{osc}(t)$ is the output oscillating signal. Fig. 5 shows two examples to illustrate the sensitivity of $S$ to the settling error. Fig. 5a shows a complete settling scenario, while Fig. 5b shows the resulting oscillation when non-complete settling occurs while the faster clock is active (in the example, when the sign of $x_{osc}(t)$ is negative). The non-ideal settling produces an increase of the DC level $S$ that can be detected.

### C. Analytical approach

As seen in Fig. 5, the most visible effect of the settling error is a signal attenuation. In order to get an idea of what can be expected by the proposed signature, let us make the approximation that the settling error translates into a gain error $\alpha$. This would be the case if the integrator operated always in the region defined in (3), with $\alpha = (1 - e^{-\pi GBW})$. It would be more correct to consider a different $\alpha$ for each sample, since we have seen that the settling error is non-linear. However, we will use a constant gain error for the sake of simplicity, in order to obtain a meaningful result.

Let $x_i$, with $i \in [1, N]$, be the samples of the oscillation waveform over one period. Let us consider that the positive and negative lobes are identical, with only a sign difference. Without modifying the clock, the continuous-time integral of a perfectly settled oscillation waveform over the positive lobe,

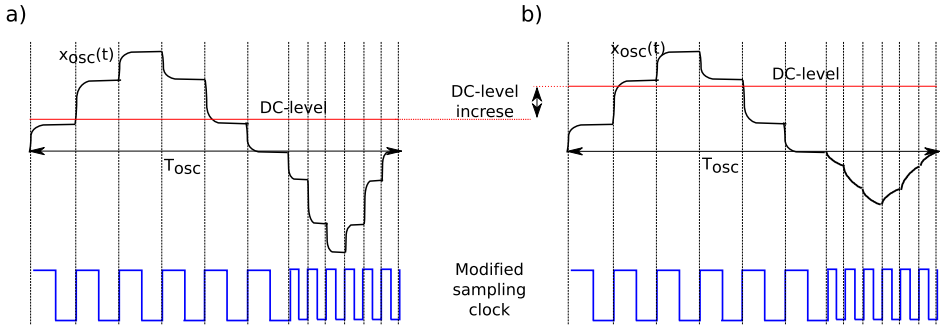


Fig. 5. Oscillating output signal under modified clocks for settling error OBT: a) Complete settling scenario; b) Incomplete settling while the faster clock is active produces a DC level increase

$A$, can be written as follows,

$$A = \frac{2}{T_{osc}} \int_0^{T_{osc}/2} x_{osc}(t)\, dt \qquad (7)$$
$$= \frac{2}{NT_s} \sum_{i=0}^{N/2} x_i T_s = \frac{2}{N} \sum_{i=0}^{N/2} x_i$$

where $T_s$ is the nominal sampling period. As expected, we obtain that $A$ is the discrete average of the samples. It is equal to the DC level of the rectified oscillating waveform and thus directly related to its amplitude.

If the clock period is doubled over the positive lobe we can consider that we have a perfect settling, while for the negative lobe we apply the above mentioned assumption of an equivalent gain error. We thus can develop (6), as

$$S = \frac{2}{3NT_s} \left( \sum_{i=0}^{N/2} x_i 2T_s + \sum_{i=N/2+1}^{N} \alpha x_i T_s \right) \qquad (8)$$
$$= \frac{2-\alpha}{3} A$$

Notice that the $2/3$ factor comes from the asymmetry in the duration of the positive and negative lobes of $x(t)$. If the settling of the integrator is accurate, $\alpha$ is very close to one and the signature close to one third of $A$. With higher settling errors, $\alpha$ is expected to decrease and the signature to increase. Also the value $A$ is sensitive to the oscillation amplitude and frequency. Hence, the proposed signature $S$ not only senses settling errors, but it can be also advantageously used to replace the usual amplitude-frequency measurements in traditional OBT by a single low-cost measurement at DC.

## IV. Implementation Example

The proposed test technique has been implemented using a SC fully-differential second-order lowpass filter as DUT. Fig. 6 shows a schematic view of the DUT and added test circuitry. The system works with two non-overlapped clock phases $\phi_1$ and $\phi_2$. A non-linear feedback loop has been added to force the oscillation during the test mode. This feedback loop comprises a comparator followed by a single-bit D/A converter. The comparator is also reused to track the sign of the output oscillating signal and feed it to the modified phase generator. The outputs of the comparator are then employed to trigger the clock modification for the settling error test mode. The complete system has been designed in a 0.35$\mu$m CMOS technology.

Fig. 6 also shows the implementation of the clock phase generator as a Finite-State-Machine. A digital multiplexer allows to select three operation modes. For the normal OBT mode and normal operation of the DUT, a zero is sent to the FSM control input and phases $\phi_1$ and $\phi_2$ are independent of the comparator output. For the other two modified OBT modes, the phases duration is doubled when the comparator output is a logic "1", or a logic "0", respectively. This way the presented FSM acts as a frequency divider controlled by the sign of the oscillating output signal. As it can be seen, the overhead due to this modification is very small.

Furthermore, given that the test information contained in the oscillation is moved to its DC component, the required signature extractor can be implemented at a very low-cost either on-chip or off-chip using a simple passive lowpass filter to filter out the signature $S$ from the oscillation.

## V. Validation and Discussion

This section intends to validate the sensitivity of the proposed signature to the settling errors in the DUT, and to show an example of catastrophic fault detection.

Firstly, we are going to consider the effects due to settling errors in the selected DUT performance. The SC filter under test is composed of two SC integrators in a feedback configuration. Then, the results in (2)–(5) can be directly extrapolated to the integrators composing the filter. According to this analysis, in the more general case, settling errors will increase with the sampling frequency. In order to illustrate this effect, Fig. 7 shows the large signal transfer function of the DUT for different sampling frequencies, obtained by electrical simulation of the DUT. These curves were measured by exciting the DUT with a single tone signal at the filter corner frequency. As expected, there is an effective non-linear decrease in the gain of the filter due to the incomplete settling when the sampling frequency increases. Our assumption of a gain error is thus reasonable, though it obviously also introduces nonlinearity.

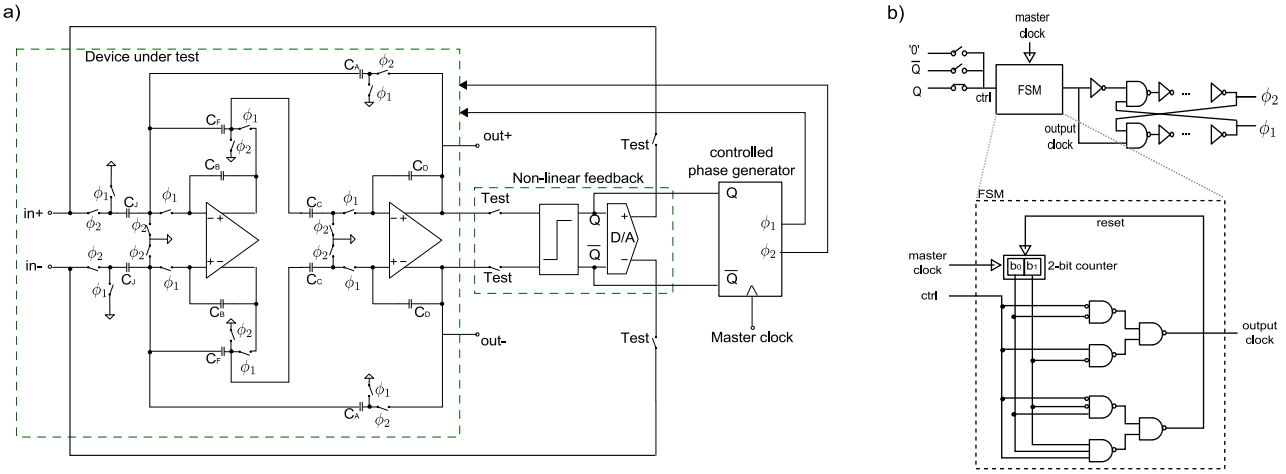


Fig. 6. a) Schematic of the SC filter under test and added test resources; b)Implementation of the modified clock phase generator

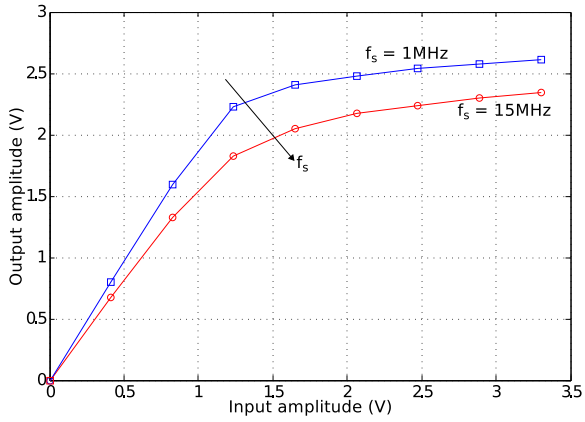


Fig. 7. Large signal transfer characteristic for a sinusoidal input at the filter corner frequency

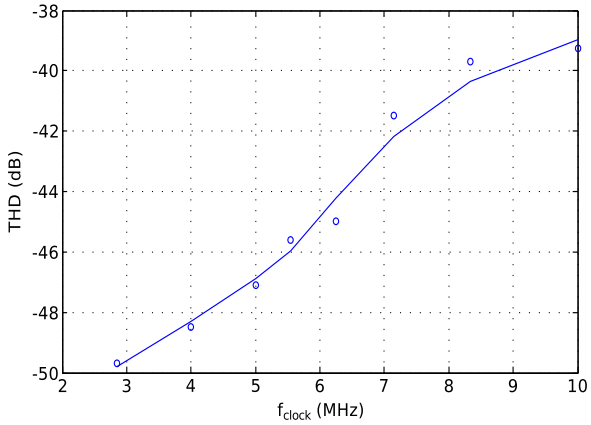


Fig. 8. THD of the filter under test versus clock frequency

Incomplete settling have an important impact in the linearity of the filter. Thus, Fig. 8 shows the evolution of the THD of the DUT when varying the sampling frequency. Measures were obtained also from electrical simulation of the system in Fig. 6 exciting the DUT with a single tone at corner frequency. As expected, increasing the clock frequency also increases the settling error, hence degrading the linearity of the filter. It is important to notice that the frequency region considered in this simulation corresponds to an incomplete settling scenario for the filter under study.

In order to verify the sensitivity of the proposed signature to the settling errors in the DUT, the system in Fig. 6 has been simulated at electrical level to perform the proposed modified OBT for settling error test. The experiment was repeated at different sampling frequencies, and testing was performed both doubling the clock period when the sign of the oscillation is positive and, conversely, doubling the clock period when the sign of the oscillation is negative. Fig. 9 show the evolution of the signatures for both cases, where $S_1$ (solid line) denotes the signature obtained when doubling the clock period when the sign of the oscillation is positive, and $S_0$ (dashed line) denotes the signature obtained doubling the clock period when the oscillation is negative. It is clear to see the correlation to the evolution of the THD. Both $|S|$ and THD increase when increasing the clock frequency.

It is also particularly interesting that, due to the fully-differential architecture of the filter under test, doubling the period of the clock when the oscillation is negative or positive only changes the sign of the signature. This opens an interesting path to further studies for detecting asymmetries in the DUT. This concept of asymmetry detection is used in the following example aimed to show the fault detection capabilities of the proposed signature. Signatures $S_1$ and $S_0$ were extracted when injecting open and short faults in switches and capacitors, as well as permanent stuck-at ON faults for switches. The sampling frequency was set to its nominal value $f_{clock} = 1$MHz.

The obtained results are shown in Fig. 10. In order to assess the test yield in this application example, 300 instances of the

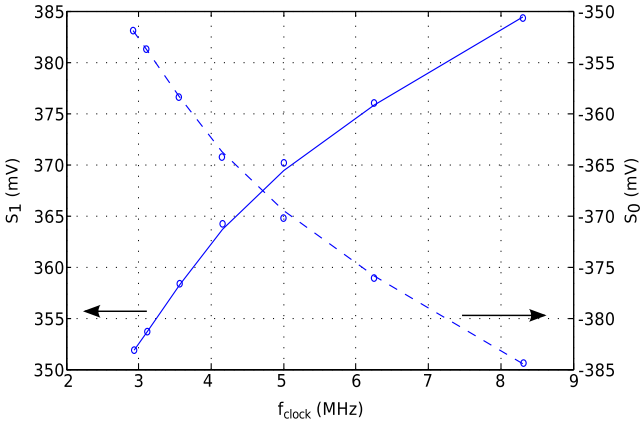


Fig. 9. DC level of the oscillating output signal, $S$, versus master clock frequency.

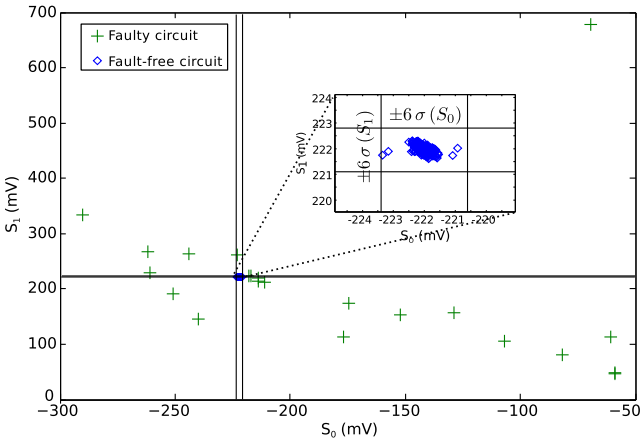


Fig. 10. Detection of catastrophic faults

fault-free circuit where generated by Monte Carlo simulation and signatures $S_1$ and $S_0$ were extracted. Diamonds markers in Fig. 10 stand for fault-free circuits, while cross markers stand for faulty ones. Using a simple $\pm 6\sigma$ criterion for fault detectability, all the considered faults translate to detectable deviations in the signatures. This result is particularly interesting due to the fact that the detection of this set of faults using traditional OBT would usually require the evaluation of the oscillation frequency and amplitude [7], while the proposed OBT modification allows its detection simply by filtering the oscillation to use its DC component as test signature.

## VI. Conclusions

Oscillation-based test is undoubtedly an interesting path to mitigate the ever increasing cost of testing non-digital blocks. It has been demonstrated in a wide variety of circuits, and the inherent low-overhead of its required test resources makes it a good candidate for fully BIST implementations. However, it has an important drawback: fault coverage and/or specification prediction may be compromised due to the limited information that can be extracted from the oscillation.

In this paper, we have presented a simple modification for OBT of sampled-data systems to enhance these test techniques. It is based on varying the frequency of the sampling clock when the oscillation changes its sign. It has been demonstrated that the DC level of the resulting asymmetrical oscillation becomes a signature sensitive to the settling errors in the DUT.

In order to verify the feasibility of the technique, the proposed OBT strategy has been implemented using a switched-capacitor analog filter. The design of the complete system has been described and the low-overhead of the proposed technique has been verified. Electrical simulation results have been provided to show the correlation of the proposed signature to the linearity of the DUT and its fault detection capabilities.

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