The Front-End Concentrator card for the RD51 Scalable Readout System

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ABSTRACT: Conventional readout systems exist in many variants since the usual approach is to build readout electronics for one given type of detector. The Scalable Readout System (SRS) developed within the RD51 collaboration relaxes this situation considerably by providing a choice of frontends which are connected over a customizable interface to a common SRS DAQ architecture. This allows sharing development and production costs among a large base of users as well as support from a wide base of developers.

The Front-end Concentrator card (FEC), a RD51 common project between CERN and the NEXT Collaboration, is a reconfigurable interface between the SRS online system and a wide range of frontends. This is accomplished by using application-specific adapter cards between the FEC and the frontends. The ensemble (FEC and adapter card are edge mounted) forms a 6U x 220 mm Eurocard combo that fits on a 19" subchassis. Adapter cards exist already for the first applications and more are in development.

KEYWORDS: Data Acquisition Circuits; Data Acquisition Concepts; Digital Electronic Circuits

Contents

1. Introduction: The Scalable Readout System (SRS)

Mandated to establish a "Portable Multichannel Readout system for Multi Pattern Gas Detectors", the Scalable Readout System (SRS) was developed within the RD51 collaboration [1] as a complete readout system for gas detectors like GEMs or MicroMegas and not excluding other types of detectors. Conventional readout systems exist in many variants since the usual approach is to build readout electronics for one given type of detector.

SRS relaxes this situation considerably by providing a choice of ASICs, hybrids or discrete frontends, either with analog, binary or digital readout, which are connected over a customizable interface to the DAQ system. This interface is implemented via generic adapter cards to a common module for all aplications, the Front-End Concentrator (FEC) and application-specific adapter cards. The FEC and the adapter card are edge mounted to form a 6U x 200 mm Eurocard. The FEC architecture is built around a configurable FPGA with event buffer, Gigabit Ethernet, I/O for Trigger and clocks and I/O for the adapter cards. The adapter card must include all the necessary resources (like signal connectors, amplifiers, ADCs, buffers, logic, etc.) to readout and control the custom front-end.

Upstream from the adapter cards, SRS defines common components for all DAQ systems. For small systems, the FECs are directly connected via gigabit Ethernet cables to the SRS default online system for RD51 users, DATE [2] which runs on 32 and 64 bit architectures and can be connected via UDP Ethernet. DATE runs on top of Scientific Linux and is supported during the lifetime of the LHC. Large systems require the Scalable Readout Unit (SRU) for aggregating up to 40 FECs to 10-Gbit Ethernet network ports of an online PC or farm. A more detailed introduction to the RD51 SRS can be found in [3].

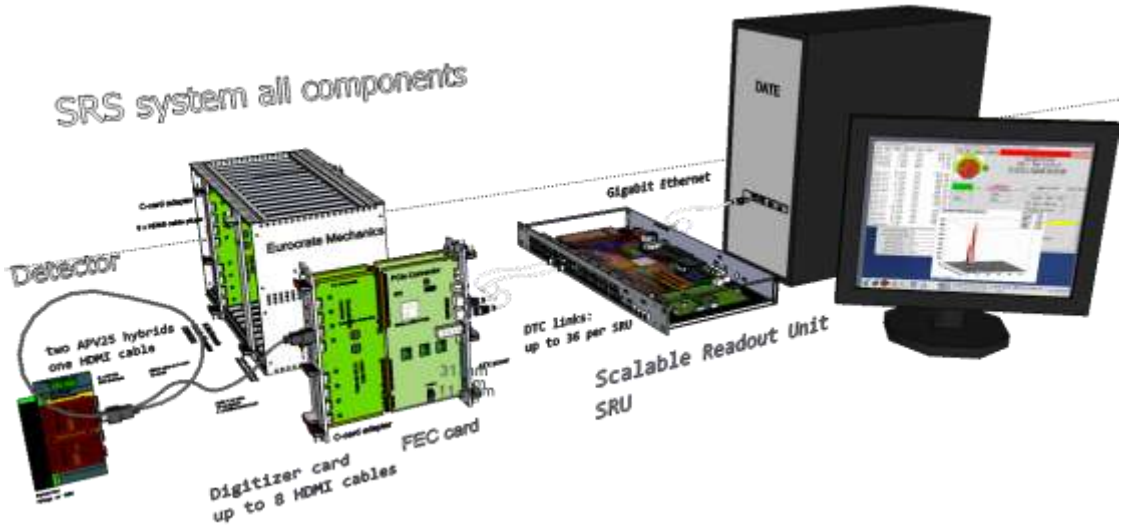

Figure 1. The SRS architecture

The SRS has been adopted or is being evaluated for a number of applications including (as of September 2011):

- Readout of PMT and SiPM sensors in the NEXT Collaboration [4]-[5]
- Muon tomography for the detection of high-z materials in cargo, a homeland security application by the Florida Institute of Technology [6]
- MicroMegas based reference tracker station for NA-62
- THGEM readout station at UNAM, Mexico
- Characterization of GEM foils at the Helsinki Institute of Physics
- Readout of resistive strip MicroMegas as upgrade to ATLAS detector
- GEM Chamber project (Jefferson Lab) and GEM readout via SRS (BNL)

2. The Front-End Concentrator card in the field

The FEC and the adapter card are edge mounted combos which form a standard 6U x 220 mm Eurocard (figure 2). Standard 19-inch Eurocard chassis without backplane allow both front panels (FEC's and adpter card's) to be accessible for I/O. Standard SRS crate come in several variants, the 3U Minicrate, the half-power and full power 6U Eurocrates. The power is generated by commercial ATX power supplies with SRS-specific ATX power adapters which use the ATX voltages (+5V, +12V, -12V and -5V), produces regulated +3.3V and +1.8V power and limits the maximum current with on-board fuses.

The half-power Eurocrate allows for up to 4 FEC combos and frontend hybrids with a maximum of 120W combined on +5V and +3.3V. The full power Eurocrate can house up to 8 combos and one clock and trigger fanout module. Despite the noisy nature of the ATX sources, on-board filters and regulators on the ATX power adapters reduce it to acceptable low levels. Existing applications using a 12-bit ADC adapter card (see Section 5.2) report very low induced noise.

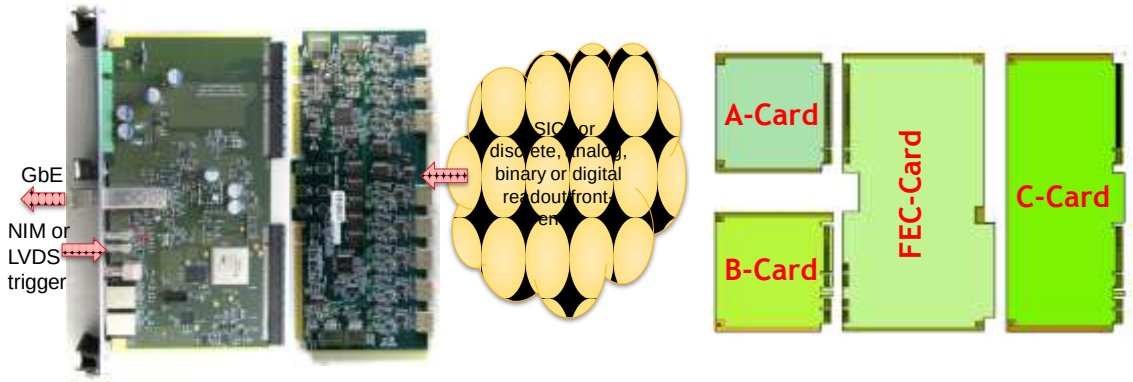

Figure 2. The FEC and the adapter card are edge mounted to form a standard 6Ux220mm Eurocard (left). On the right, the A, B and C form factors for the adapter cards.

Besides the 19" Eurocard chassis mechanics shown in figure 3 left, an evaluation system exists in a more compact form factor named "SRS minicrate" (figure 3, right).

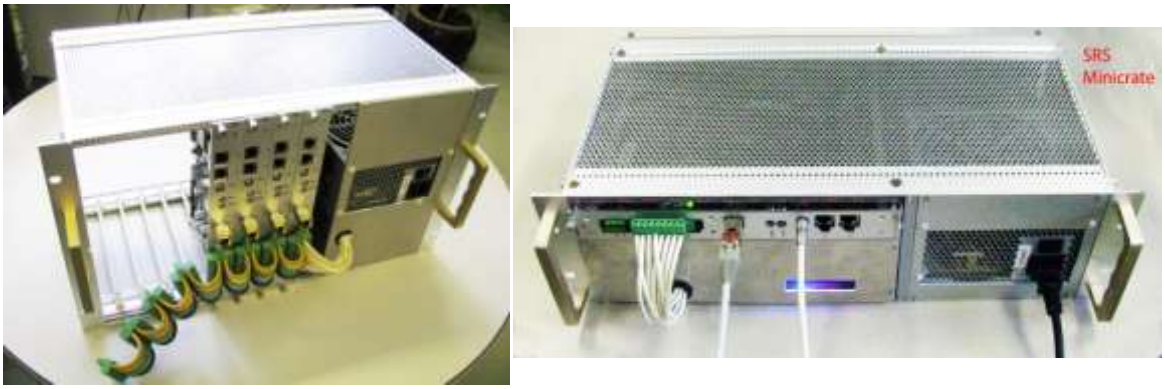

Figure 3. FEC cards, ATX power supply and ATX box unit in a 19" chassis (left). The SRS minicrate (right).

3. The FEC hardware

The heart of the module is a Xilinx Virtex-5 LX50T FPGA as all I/Os in the front panel and in the edge connectors are connected to this device.

A 256-MByte DDR2 buffer is placed very close to the FPGA. It allows 16-bit read/write transactions at a 400 MHz data rate. An SFP socket allows plugging either copper or optical transceivers. Usually, a 1.25 Gbps copper gigabit Ethernet is used to interface the online PCs. The UDP protocol is implemented in the FPGA firmware to send data frames of any size up to 9 KBytes (Jumbo frames), which is the recommended value as it has been found that the larger the frame, the higher the link throughput.

The clocking and trigger scheme is very flexible thanks to the additional I/Os in the front panel and to the firmware reconfigurability. NIM input and output via LEMO 00 connectors as well as an LVDS input on a LEMO 0B can be used as alternative trigger input/output or clock input. Additionally, two RJ45 sockets, each with two LVDS input and two LVDS output pairs, provide further flexibility for trigger, clock, slow controls and data transmission.

Figure 4. A picture of the FEC card version 3.

4. Data, timing and control (DTC) link

SRS systems with a larger number of FEC cards require an SRU as data concentrator between the FEC layer and the online system. For this purpose the DTC link of the SRU is interfaced via RJ45 connectors. Each RJ45 socket provides four LVDS pairs (two inputs, to outputs) to implement a full-duplex link over standard CAT-6 network cable. Inputs are defined as clock and command (including eventually trigger) lines. Outputs carry event data.

A first implementation by the NEXT Collaboration defines a simple 16-bit-word frame format. Each data frame is composed of a start of frame header, an identifier and frame length word, a variable number of data words and an end of frame trailer. A CRC word before the trailer is optional. A similar frame format has been defined for the command line and is currently used in the NEXT application for acquisition on/off, timestamp synchronization and trigger commands. Each data line is operated at 200 Mb/s. The input clock line, generated by the destination, is a 100 MHz free running clock.

The described link (with no CRC word and with a 352 Mb/s rate) was validated in a point-to-point test setup with a 15-meter CAT-6 network cable. No error in the link occurred during three days of operation at the nominal 352 Mb/s load with PRBS data. The estimated BER is lower than 1e-13 with a 99.99% confidence level. This result confirms the goodness of the link implementation.

5. Adapter cards

Three form factors (A, B and C) have been defined as shown in figure 2, with mechanical specifications and design rules freely available to the SRS developer community. All adapter cards so far are C-sized, though those applications that need but a limited board area and I/O

connectivity can opt for a more cost-effective A or B size. C-card form factor is approx. 233 mm x 97 mm.

5.1 Interface to the adapter card

The FEC module uses up to three connectors to interface the adapter cards, as shown in figure 4, top. From right to left: a PCI Express x16 (named A-Card connector), a PCI Express x8 (B-Card connector) and a PCI Express x1 (Power connector). PCI Express is not used as protocol or electrical interface but as an off-the-shelf high-speed physical connector. Pinout, signal functions and signaling interfaces have been redefined. Adapter cards are free to use either the A, B or both signal connectors, but must use at least one of them. The Power connector can be user or not. The A-Card connector provides the following I/O resources:

- A 32-bit bus with selectable signaling levels. These signals can be used as 32 single-ended lines, as 16 differential pairs or as a mix of single-ended and differential pairs.
- Twenty high-speed LVDS differential pairs, though these can be also used as 40 single-ended signals or a mix of these two functions.
- JTAG bus, I2C bus, presence and power good lines and a few power pins.
- One full-duplex multi-gigabit transceiver, allowing up to 2.5 Gbps data dates.

The B-Card connector provides a 16-bit data bus, JTAG, I2C, presence and power good lines, a few power pins and a multi-gigabit transceiver. The Power connector supplies additional +3.3V, 5V, +12V, -12V, -5V for the adapter card electronics and bias voltage for sensors like APDs or SiPMs.

5.2 The CERN ADC card

The most popular adapter card (figure 5, left) was originally designed to interface the RD51 APV25 ASIC hybrid [7] and will soon interface also the RD51 Beetle ASIC hybrid. Among other features, the card includes dual 8-channel 12-bit 40-to-50 MHz ADCs. As a result, this card can be used as a generic 16-ch digitizer. This is the case of the PMT plane readout in the NEXT-1 experiment prototype [5] or the GEM readout in a muon tomography station prototype at the Florida Institute of Technology [6].

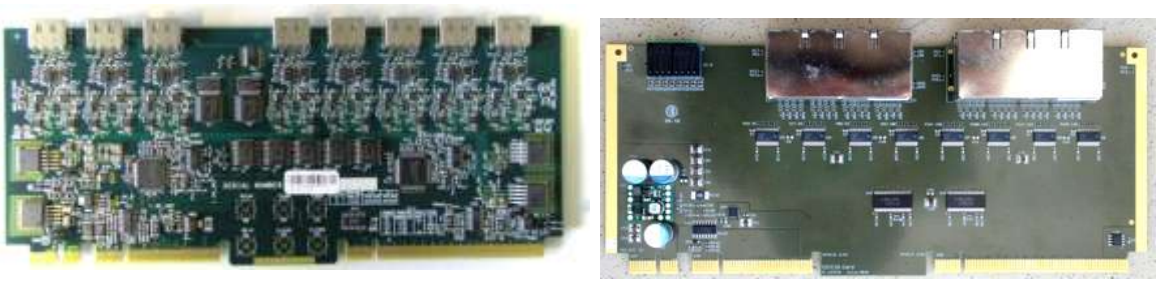

Figure 5. The CERN ADC adapter card (left) and the NEXT LVDS card (right).

5.3 The NEXT LVDS card

This card is a 16-fold DTC interface as described in section 4. It includes two octal RJ45 sockets, LVDS buffers and 16 LEDs controlled from an I2C bus. Designed by the NEXT Collaboration, it has a dual purpose: (1) readout of the digital front-end for the SiPM plane array in the NEXT-1 experiment [4] and (2) together with a mating FEC, to form the trigger module for the NEXT-1 experiment, distributing common clock and commands (including time stamped triggers) to all DAQ FECs and receiving trigger candidates from them.

5.4 Adapter cards projected and under design

There is a new C-sized card under design to read out the new VMM1 ASIC at BNL. There is a C-card under design to interface the (also called) FEC module based on the AFTER ASIC from the T2K electronics. In the horizon, there is an interest to develop a CERN GBT receiver card to interface the next generation of digital readout ASICs.

6. FPGA firmware

RD51 aims at providing new and existing users with firmware code for the common functional blocks and examples for application-specific code. In order to ease code reuse and user application development, the FEC firmware is modular with simple I/O interfaces. Firmware is mainly composed of seven functional blocks (figure 6). Some of them are available and ready to use (like the DDR2, GbE and DTC interfaces) while others must be developed for each application (Adapter Card Interface and Process Unit blocks). An additional block, the Control Unit, provides a set of basic commands and configuration/status registers which can easily be modified for each specific application. An auxiliary unit synchronizes the data flow between the functional blocks using FIFO-like interfaces: the Configurable Interconnect Unit.

As an example, in the case of the PMT plane readout in the NEXT-1 experiment prototype, the Adapter Card Interface has been programmed to implement the CERN ADC Card interface. Data are formatted and stored in the DDR2 buffer. Data are also processed (Process Unit) to send trigger candidates through the DTC Interface to a Trigger Card (another FEC). The same interface is used to receive a valid trigger that forces data to be sent to the DAQ PC through the GbE interface. The Configurable Interconnect Unit is programmed to define the appropriate data flow.

7. Future work

A new FEC version is being designed in order to increase processing power and data throughput. The Virtex-5 FPGA will be replaced by a more powerful Virtex-6 device with enhanced SEU immunity. The DDR2 buffer will be replaced by a four times larger and faster DDR3 memory. A second SFP+ socket will be added to allow for a second gigabit interface or slow controls via Ethernet. Additionally, more I/Os, especially multi-gigabit capable lines, will be added to the edge connectors while maintaining backwards compatibility.

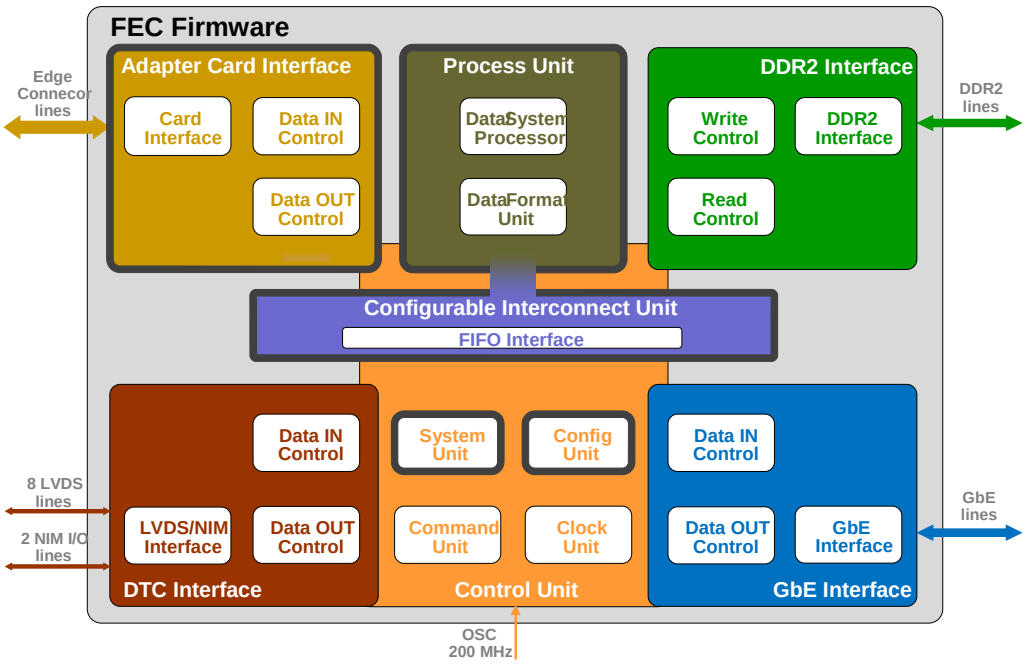

Figure 6. Functional blocks in the FEC firmware.

Acknowledgments

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