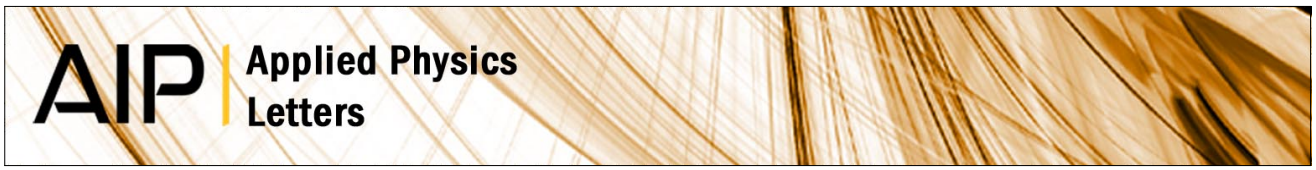

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Quantum well heterostructures grown by molecular beam epitaxy on silicon-on-gallium arsenide substrates

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Silicon-on-gallium arsenide (SonG) wafers have recently been proposed as optimal substrates for monolithic integration of GaAs-based optoelectronic devices with silicon electronics. In this letter it is demonstrated that high quality quantum well heterostructures can be grown on SonG substrates under conditions consistent with the survival of pre-existing electronics. Photoluminescence and cathodoluminescence measurements confirm that these layers are sufficiently high quality to allow integration of light emitting and laser diodes on SonG substrates. © *1999 American Institute of Physics.* [S0003-6951(99)03648-7]

The monolithic integration of silicon VLSI electronics with gallium arsenide (GaAs) optoelectronic devices presents significant challenges. The reasons lie in the substantial differences between these two semiconductors in several key material properties, specifically the lattice constants, which differ by 3.5% (5.43 Å for silicon vs 5.63 Å for GaAs), and the thermal expansion coefficients, which differ by a factor of more than 2.5 ($2.6\times10^{-6}\,^{\circ}\mathrm{C}^{-1}$ for silicon vs $6.86\times10^{-6}\,^{\circ}\mathrm{C}^{-1}$ for GaAs). A solution which has recently been proposed to overcome these material roadblocks is the use of silicon-on-gallium arsenide (SonG) wafers.[1] In this technique separation by implantation of oxygen (SIMOX) silicon wafers are hydrophilically bonded to GaAs wafers. The bulk of the SIMOX wafer is then removed leaving a thin layer of silicon (several hundred angstroms thick) bonded to a GaAs wafer through several dielectric layers. A TEM cross-section view of the bonded layers on the top of a SonG wafer is shown in Fig. 1. These wafers can then be used in an SOI process to produce silicon electronics on GaAs optoelectronics-friendly substrates; alternatively, the same bonding techniques might be used to bond and transfer completely processed SOI CMOS to GaAs wafers to achieve the same goal.

The attractiveness of this structure for monolithic optoelectronic integration derives from several device and materials observations. First, it is well known that thin layers can tolerate much higher stress than thick layers. The level of stress experienced by the thin silicon layer in a SonG wafer is similar to that experienced by the silicon in silicon-on-sapphire wafers because the thermal expansion coefficient of sapphire is very similar to that of GaAs. Thus we anticipate that a thin layer of silicon bonded to GaAs can tolerate subsequent high temperature processing. In fact SonG wafers have successfully been exposed to temperatures of 700 °C, and should tolerate far higher temperatures with suitable encapsulation of the back surface of the GaAs wafer.[1] Second, optoelectronic devices require thicknesses on the order of microns, but MOS devices only require a silicon thickness of a few hundred angstroms. The thin Si in a SonG wafer is thus perfectly suited for fabricating VLSI Si electronic circuits, and the GaAs substrate provides the optimal foundation for optoelectronic devices. Finally, the lattice mismatch between the materials can be circumvented by bonding oxide-coated single-crystalline wafers.

A first step in realizing a monolithic integration of Si and GaAs devices using the SonG structure is to demonstrate that an optical device heterostructure can be integrated with the silicon film on a SonG wafer using epitaxial growth on the GaAs substrate.[2,3] It is this step which is addressed in this letter.

Samples approximately 1 cm by 1 cm square were cut from a SonG wafer.[1] Photoresist was spun over the upper sample surface. Using conventional contact optical lithography, an array of 50 μm squares was created through the photoresist exposing the underlying buried oxide (BOX) layer. Reactive ion etching (RIE) was used to penetrate through the BOX layer and the Si layer. The RIE process conditions were 50 sccm of CF_4 and 5 sccm of O_2 with a pressure of 30 mT, 400 W of power, and a dc bias of 487 V.

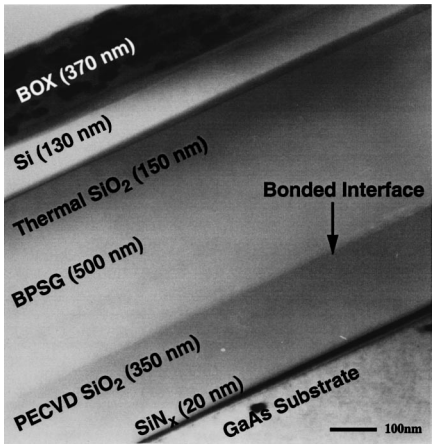

FIG. 1. A TEM cross-section micrograph of the upper portion of a SonG wafer showing, beginning at the top, the BOX layer, the silicon layer, the various oxide layers in the bonding region, and a part of the gallium arsenide substrate. Additional views of SonG wafers can be found in Ref. 1.

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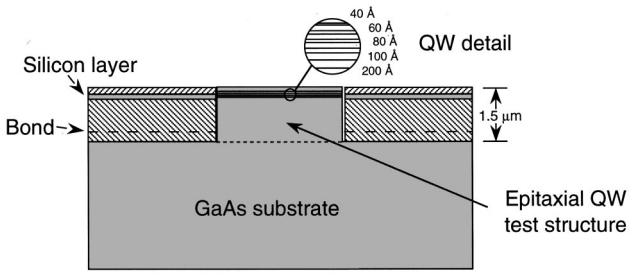

FIG. 2. An artist's schematic cross section of a multiple quantum well heterostructure grown in a dielectric growth window on a SonG wafer. The polycrystalline deposition which occurs outside of the growth window is not shown in this cartoon.

The remaining dielectric layers were removed with buffered oxide etch until the underlying GaAs substrate was exposed. The photoresist was then stripped with acetone. The oxide bonding layers in the region of the wafer from which the sample was cut were thinner than shown in Fig. 1, so the growth windows were just under 1 μm deep.

Molecular beam epitaxy (MBE) was used to grow a GaAs buffer layer and a $In_{0.2}Ga_{0.8}As$/GaAs quantum well structure on the SonG sample, and, simultaneously, on a piece of an epiready GaAs wafer; the latter will be referred to in the following as the control sample. Five $In_{0.2}Ga_{0.8}As$ quantum wells were grown with nominal thicknesses of 4, 6, 8, 10, and 20 nm, respectively. The GaAs spacers between the wells were nominally 20 nm, the GaAs cap layer was 100 nm thick, and the initial GaAs buffer layer was approximately 1.2 μm thick. A cross-sectional schematic of the target structure, albeit with a deeper growth window, is shown in Fig. 2.

Prior to beginning epitaxy, any native oxide on the gallium arsenide surfaces was removed using atomic hydrogen at 450 °C, rather than thermal desorption; the MBE growth was performed at 475 °C.[4] Reduced temperature techniques were used because it is known from earlier work[5] that processed electronics must be kept below 500 °C in order to avoid any degradation of their performance.

Wherever the GaAs substrate was exposed, the grown material was single crystalline. Over the BOX layer, the grown material was polycrystalline. This can be easily distinguished in Fig. 3, which shows a photomicrograph of a focused ion beam etch (FIBE) cross section through the growth in one window and the area adjacent to it. The original GaAs substrate, the thin Si layer, and the oxide bonding layers, and the single crystal growth and the polycrystalline deposit are all clearly visible. One also notes that the wet etching of the growth window resulted in some lateral etching of the oxide layers above and below the silicon layer; this can be corrected in future work.

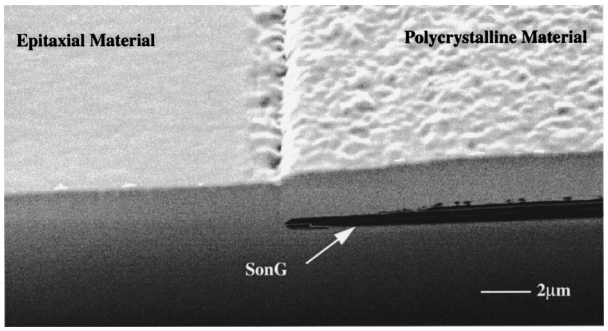

FIG. 3. A SEM photomicrograph of a FIBE cross section of the growth on the SonG sample positioned to overlap the edge of a growth window and show the epitaxial heterostructure, the original SonG layers, and the polycrystalline deposit over the top of the latter.

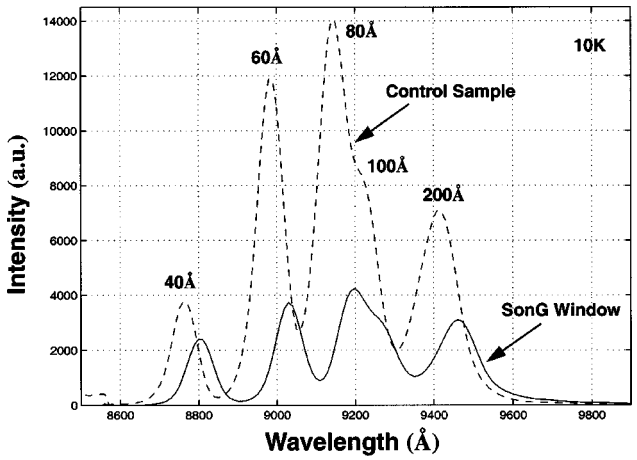

FIG. 4. Photoluminescence spectra taken at 10 K on the control sample and on the SonG sample after epitaxy. The vertical scales are uncalibrated but the relative intensities have been corrected for the smaller area of single-crystal growth in the windows on the SonG sample.

The quality and uniformity of the growth were assessed using photoluminescence (PL) and cathodoluminescence. PL data were collected on the structures grown on the control sample and in the windows on the SonG substrate; this data is shown in Fig. 4. The measurements were taken using argon ion laser excitation at a temperature of 10 K. The luminescence peak due to each quantum well can be distinguished independently, although the 8 and 10 nm quantum well peaks overlap somewhat. The intensity of the data from the growth on the SonG wafer is about a third of that from the control wafer, even after accounting for the reduced area of light emission from the SonG windows. This may be because the epiready sample is of higher quality than the semi-insulating substrate of the SonG wafer, but this point needs further study. The quality of the SonG growth is suitable for device fabrication, but can be improved further, perhaps through the incorporation of thicker and more complex buffering layers.

The other feature which is different between the two photoluminescence spectra shown in Fig. 4 is a wavelength shift. An analysis of this shift indicates that the x value of the $In_xGa_{1-x}As$ in the quantum wells is larger by 0.01 for the SonG sample than for the control sample. This can be explained by noting that although the samples were grown simultaneously, they were at different locations on the mounting block in the MBE chamber and thus experienced different growth parameters. Another possible explanation is that there was a temperature difference in the SonG windows due to the silicon and/or oxide coverings.

The sharpness of the photoluminescence peaks on both samples indicates that the growth was uniform over the approximately 1 cm^2 area of each sample, even if it varied between the two samples. In the case of the SonG wafer, this sharpness is also an indication that the well composition did not vary appreciably near the edges of the growth windows.

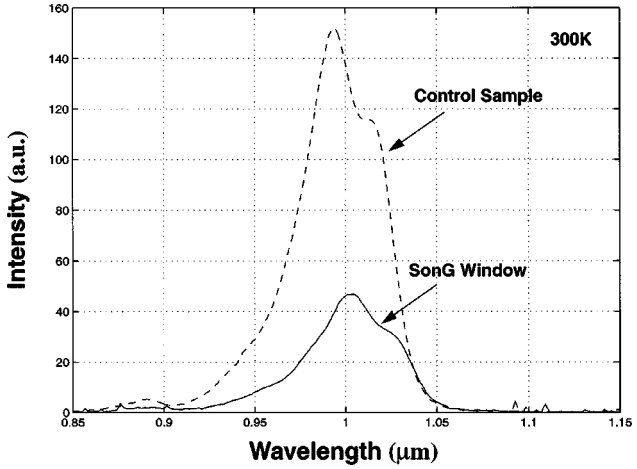

FIG. 5. Cathodoluminescence spectra taken at room temperature on the control sample and on the SonG sample after epitaxy. The vertical scale is uncalibrated but is the same for both samples.

Cathodoluminescence (CL) data were collected at room temperature on the bulk GaAs substrate as well as the SonG sample; these spectra are shown in Fig. 5. A 10 keV electron beam source was used. Because this measurement was made at room temperature, the intensity of the CL was less than that of the PL and also it is not possible to distinguish the individual quantum well peaks in the spectrum. Once again the intensity from the SonG windows was approximately three times smaller than from the control sample. (Note that because the electron beam excites a small area that could be localized within a growth window on the SonG sample, no correction was made of the intensity of the CL spectrum from this sample.) Also, the SonG window data are again shifted with respect to the bulk data, consistent with the PL data. (The CL spectra are, of course, shifted with respect to the PL data because of the band gap change with temperature.) It will be of interest in the future to do more detailed profiling of the CL intensity and spectrum from edge-to-edge in a growth window to confirm the uniformity indicated from the PL spectra and to see if there is any reduction in intensity near the edges of the well.

High quality $In_{0.2}Ga_{0.8}As/GaAs$ quantum well heterostructures have been grown on a silicon-on-gallium arsenide substrate. PL and CL measurements confirm that the films are sufficiently high quality to allow integration of light emitting diodes (LEDs) and/or laser diodes on SonG wafers. With the successful demonstration of high quality quantum well heterostructures on SonG wafers, the next goal is to demonstrate that such structures can be grown on SonG wafers with functioning electronic devices in the silicon, and to then integrate, for example, laser diodes with silicon circuitry in this manner. To this end future work will include bonding fully processed SOI CMOS wafers to GaAs, rather than SOI wafers containing no electronics.

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[1] J. M. London, A. H. Loomis, J. F. Ahadian, and C. G. Fonstad, Jr., IEEE Photonics Technol. Lett. **11**, 958 (1999).
[2] J. F. Ahadian, P. T. Vaidyananthan, S. G. Patterson, Y. Royter, D. Mull, G. S. Petrich, W. D. Goodhue, S. Prasad, L. A. Kolodziejski, and C. G. Fonstad, Jr., IEEE J. Quantum Electron. **34**, 1117 (1998).
[3] J. F. Ahadian and C. G. Fonstad, Jr., Opt. Eng. (Bellingham) **37**, 3161 (1999).
[4] P. A. Postigo, G. Lullo, K. H. Choy, and C. G. Fonstad, Jr., J. Vac. Sci. Technol. B **17**, 1281 (1999).
[5] E. K. Braun, K. V. Shenoy, C. G. Fonstad, Jr., and J. M. Mikkelson, IEEE Electron Device Lett. **17**, 37 (1996).