BIST Method for Die-Level Process Parameter Variation Monitoring in Analog/Mixed-Signal Integrated Circuits

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Abstract *- This paper reports a new built-in self-test scheme for analog and mixed-signal devices based on die-level process monitoring. The objective of this test is not to replace traditional specification-based tests, but to provide a reliable method for early identification of excessive process parameter variations in production tests that allows quickly discarding of the faulty circuits. Additionally, the possibility of on-chip process deviation monitoring provides valuable information, which is used to guide the test and to allow the estimation of selected performance figures. The information obtained through guiding and monitoring process variations is re-used and supplement the circuit calibration.*

I. Introduction

With the increased complexity of VLSI circuits and the reduced access to internal nodes, the task of properly testing these devices is becoming a major bottleneck. The large number of parameters required to fully specify the performance of mixed-signal circuits and the presence of both analog and digital signals in these circuits make the testing expensive and time consuming task. Design for Testability (DfT) and Built in Self Test (BIST) techniques are aimed at increasing observability and controllability for reducing test cost and improving test quality. We propose die-level process monitoring (DLPM) structural BIST testing, where extra circuitry is used to perform an operational test, which is targeted to detect circuit malfunctioning and to assure, up to some extend, that specifications are fulfilled without actually measuring functional parameters. This test approach is less costly and of great importance for easy and fast testing of analog circuits malfunctions, and for increasing observability and controllability of the device under test (DUT). The proposed DLPM method is evaluated on an analog to digital converter (ADC) as the appropriate representative. Although several attempts [1-8] have been made to alleviate increasing test difficulties of ADC testing, none of these methods provides the possibilities for early identification of excessive process parameter variations. In [1], the on-chip delta-sigma DAC for sine wave generation and DSP techniques for data analysis are utilized. However, the technique requires, both, intensive computation and on-chip ADC and DAC. In [1], a sine-wave generator and processing core circuits are incorporated into a VXI bus-based system, which performs both static and dynamic tests. A similar system with external instruments is developed in [2]. A large amount of sampled data must be collected to support both methods. The approach reported in [4] relies on analog circuitry and reference voltages for measurements and allows testing of only DAC-based ADCs. In the oscillation-test method proposed in [5], the impact of the control logic delay and the imperfect analog BIST circuitry on the test accuracy is not assessed. In [6] the linearity of the ADCs is tested by monitoring the LSB externally. The work in [7] proposes an efficient polynomial-fitting algorithm for DAC and ADC BIST. The drawback is again the need of both on-chip ADC and DAC. The viability of a histogram-based BIST approach in case of a sinewave input test signal is investigated in [8]. Applying the sequential decomposition of the test procedure, although reducing the additional circuitry, implies that a high number of input test patterns are required to complete the test.

II. Proposed Method

Measurement of transistor parameters fluctuations is paramount for stable control of transistor properties and statistical monitoring. The evaluation of these effects enables the efficient development of test patterns and test methods, as well as ensures good yields. To facilitate the measurement of these fluctuations, we propose test strategy as depicted in Figure 1. A family of built-in process variation sensing circuits is placed (at least) at each corner of the device under test. This location maximizes the sensing capability of process variations due to process gradients. Depending on the size of the DUT, extra sensors can be placed in and around the DUT to form the additional statistical mass. The built-in process variation sensor (Figure 2) consists of a die level process monitor circuits (DLPM's) extracted from the DUT itself, an amplifier, which isolates the test circuit from the DLPM and a programmable data decision circuit to detect the excessive process parameter variations.

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The analog decision is converted into pass/fail (digital) signals through the latter circuit. The interface circuitry allows the external controllability of the test, and feeds the digital decision to a scan chain. Test control block (TCB) selects through the test multiplexer (TMX) the individual DLPM measurement.

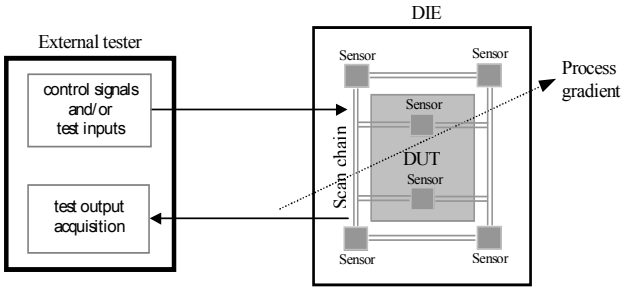

Figure 1: Proposed test strategy

Select, reference and calibration signals are offered to the detector through the interface circuitry. Digital control logic can be inserted on the chip or done externally.

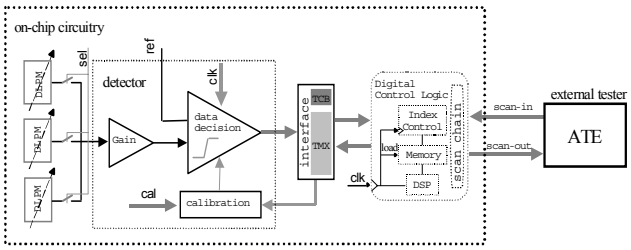

Figure 2: Built-in sensors block scheme

Figure 3 shows the complete test scheme including the DLPM circuits, detector, reference ladder, the switch matrix to select the reference levels for the decision window, the interface to the external world, control blocks to sequence events during test, the scan chain to transport the pass/fail decision and the external tester. To test against a tolerance window it is necessary to test against a "high" and a "low" level. Due to the differential nature of the measurements, two runs with interchanged detector references are needed in each test to assure a proper pass/fail decision. This double-measurement protocol allows the definition of a pass/fail window, instead of a single pass/fail level. Since the result of each run is a digital 1-bit signal, the computation of the test result can be done either on-chip adding some simple logic to the detector, or off-chip using resources located in the tester itself. To test against a tolerance window, two runs $m_{t1}(i)$ and $m_{t2}(i)$ are needed with interchanged data decision circuit references, consists of two thresholds $m_{t1,21}(i)$ and $m_{t1,2r}(i)$. If a test is successful, the measurement point plus uncertainty due to noise, $m_{t1,2}(i)+\varsigma$, will lie within the range given by $(m_{t1,2l}(i), m_{t1,2r}(i))$, where ς is the uncertainty due to noise. As a result, the following inequalities hold,

$$\begin{aligned} m_{t1,2l}(i) &\le m_{t1,2(i)} + \varsigma \le m_{t1,2r}(i) \\ m_{t1,2l}(i) - \max(\varsigma) &\le m_{t1,2(i)} \le m_{t1,2r}(i) - \min(\varsigma) \end{aligned} \quad (1)$$

Assuming that noise ς falls in the range of $(-\Delta,\Delta)$, $m_{t1,2}(i)$ satisfies the following inequality detection thresholds in the presence of measurement noise is

$$m_{t1,2l}(i) - \Delta \le m_{t1,2(i)} \le m_{t1,2r}(i) + \Delta \quad (2)$$

The reference voltages defining the decision windows are related to the DUT specifications and performance figures under study.

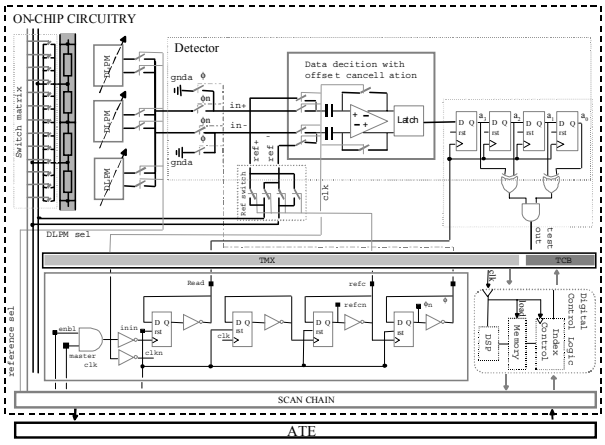

Figure 3: Test scheme block diagram

By sweeping the reference voltage until a change in the decision occurs, information about the process variations can be extracted. The robustness against process variations in the detector itself is provided by an auto-zeroing scheme. If a higher resolution is required, the efficiency of this auto-zeroing can be improved, at the expenses of area overhead, by increasing the value of the input capacitors and/or the preamplifier gain. However, the auto-zeroing scheme does not assure the functionality of the comparator. For instance, a stuck-at fault affecting the output memory element will not be corrected and it will result in a faulty detector. By this reason, an initial test stage to auto-test the detector functionality has to be added to the test protocol. The test protocol is as follows. While the *Enable* signal is high, the system enters in test mode. Inside the test mode, two main phases can be distinguished depending upon the state of signal ϕ. If ϕ is high, the inputs of the detector are shorted to analog ground to perform a test of the detector itself, whereas if ϕ is low the particular DLPM is connected to the detector and tested. Each of these phases takes four *Master clock* periods, two with the reference signal set to the upper limit of the comparison window and the other two with the reference set to the lower limit. During the detector test, the change of the reference should cause the output to change state, since the input is set to zero. The detection of this change is a quick and easy proof of the

functionality of the detector. During the DLPM test, the output of the DLPM is sequentially compared with the references to determine whether the measurement is inside the expected window or not. In both cases, a simple shift register triggered by the signal labeled *Read* acquires the detector output. The rising edges of this signal are located at the 'hold' state of the detector. The test output will be a 4-bit signal, labeled $a_0a_1a_2a_3$, which codifies the four different states. This test result can be computed either on-chip in DSP unit, as depicted in Figure 3, or off-chip. Once the result is available (either the test result itself or the 4-bit number $a_0a_1a_2a_3$ without processing) it can be fed to a scan chain scheme for its later extraction. In addition, it is important to remark that the system features an additional test mode to test all the flip-flops used in the test scheme. When this test mode is activated, the flip-flops are isolated from the rest of the circuitry and connected together as a shift register. Additional test input/output for this purpose are also available.

III. Multi-Step ADC

In multi-step ADC, high linearity is obtained by extensive usage of correction and calibration procedures. Providing structural DfT and BIST capabilities to this kind of ADCs is difficult since the effects of correction mechanism must be taken into account. Overlap between the conversion ranges of two stages has to be considered, otherwise, there may exist conflicting operational situations that can either mask faults or give an incorrect fault interpretation. The primary error sources present in a multi-step ADC are decision stage offset voltage errors, stage gain errors and errors in the internal reference voltages. For all primary error sources, we derive separate DLPM. The offset errors include offset caused by component mismatch, self-heating effects, comparator hysteresis or noise. The gain error group includes all the errors in the amplifying circuit, including technology variations and finite gain and offset of the operational amplifier. The reference voltage errors are caused by resistor ladder variations and noise, as well as to errors in the switch matrix, which are mainly due to charge injection in the transmission gate. By monitoring on-chip process parameters deviation, valuable information, which can be used to guide the test and allow the estimation of selected performance figures, is provided. Figure 4 depicts the proposed test strategy block diagram. The data detector compares the output of the die level process monitor against a comparison reference window, whose voltage values (corresponding to the required LSB values) are selected from the reference ladder or set externally. The total area overhead is limited to the 10 %, while parallelism insures that the data detector settling time is only boundary on the total test time.

A. Multi-Step ADC error modeling

The input-referred error e_{in}, that is equivalent to the contributions of all the individual error sources is

$$e_{in} = e_1 + \sum_{i=1}^{k-1} \frac{e_{i+1}}{G^i} \qquad \text{with} \qquad e_i \le \frac{V_{FS}}{2^{N+1}} G^{i-1} \tag{3}$$

which is the limit of the ADC error arising from each error source to less than ½LSB, where k is the number of the stages i, V_{FS} is full scale input signal and G is the gain of the stage. Decision stage offset of the coarse and fine ADC moves the coarse and fine ADC decision levels. If the correction range is not exceeded by the combination of all errors that shift the coarse ADC decision levels, the effect of the coarse ADC decision stage offset is eliminated by the digital correction. The non-compensated remaining offset at the input of each ADC comparator due to the decision stage offset is given by

$$V_{off|NC}^{D} = \frac{V_{off}^{D}}{G^{i-1}} \tag{4}$$

where $V_{off|NC}^{D}$ is the input referred non-compensated offset, and V_{off}^{D} is the decision stage offset. Imposing a ±½LSB maximum deviation leads to the definition of the comparison window:

$$-\frac{V_{FS}}{2^{N+1}} G^{i-1} \le \Delta V \le \frac{V_{FS}}{2^{N+1}} G^{i-1} \tag{5}$$

The gain error in the S/H and residue amplifier can be combined into one equivalent error that is very critical to linearity. A gain error in the residue amplifier scales the total range of residue signal (signal as a result of the subtraction of the input signal and the DAC signal) and causes an error in the analog input to the next stage when applied to any nonzero residue, which will result in a residue signal not fitting in the fine ADC range. To elevate this problem, two residue amplifiers [9] have been employed. According to coarse quantization decision, a first and a second residue amplifier pass the difference between the analog signal and the closest and the second closest quantization level, respectively. By passing both residues to subsequent stages, information is propagated about the exact size of the quantization step. The absolute gain of the two residue amplifiers is therefore not important, providing that both residue amplifiers match and have sufficient signal amplitude to overcome finite comparator resolution. If the correction range is not exceeded by the combination of all errors that shift the coarse ADC decision levels, the effect of the DAC gain error in series with the coarse ADC is eliminated by the digital correction.

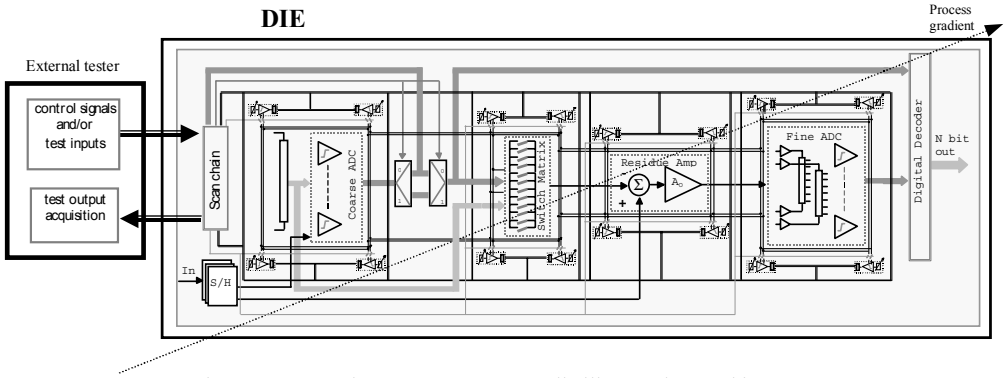

Figure 4: Proposed test strategy conceptually illustrated on Multi-step ADC

Linearity errors in the coarse ADC, DAC and fine ADC can be modeled by decision stage offset voltage errors, stage gain errors and errors in the internal reference voltages. The effect of coarse ADC nonlinearity is studied by examining plots of the ideal residue versus the input. In Figure 5*(a)*, both the coarse ADC and the DAC are assumed to be ideal. When the input is between the decision levels determined by the coarse ADC, the coarse ADC and DAC outputs are constant; therefore, the residue rises with the input.

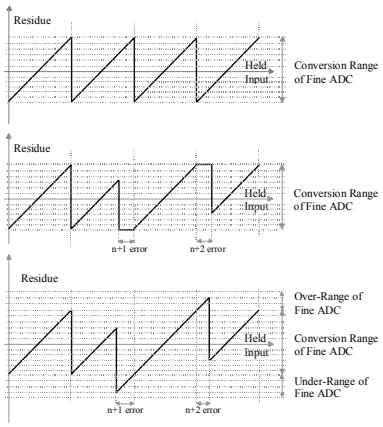

Figure 5a) Ideal residue versus input, b) Residue versus input with coarse ADC nonlinearity, c) Residue versus input with coarse ADC nonlinearity errors when over-range is applied

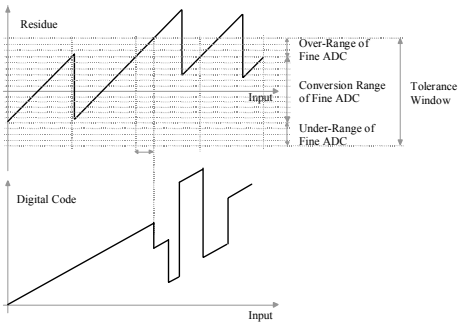

Figure 6: a) Coarse ADC and DAC transfer characteristics in the presence of fault, b) Faulty digitally corrected ADC transfer characteristic

When the coarse ADC has some nonlinearity, with the DAC still ideal, as shown in Figure 5*(b)* for a similar example, two of the coarse ADC decision levels are shifted. When the input crosses a shifted decision level, the residue decreases by the digital value of the fine ADC conversion range. If the conversion range of the second stage is increased to handle the larger residues, they can be encoded and the errors corrected (Figure 5*c*). DAC transfer characteristic in the presence of fault is illustrated in Figure 6*a)*; note that the fault provokes over-range and level shifting errors. Processing these data with the rest of the ADC, including the correction logic is shown in Figure 6*b)*. Digital correction does not mask all errors produced by the fault, and hence the circuit is faulty: on the other hand, since the window comparator threshold has been exceeded the fault is also a "detected fault". The references of the DAC and the subtraction of the input signal and the DAC output determine the achievable accuracy of the total ADC. The residue signal R is incorrect exactly by the amount of the DAC nonlinearity

$$R = GV_{in} - DAC_{out} - \delta_l \tag{6}$$

where DAC_{out} is the ideal output of the DAC, G is the gain and δ_l is DAC nonlinearity error. To limit the resulting nonlinearity to less than ½ LSB

$$\left|\delta_l\right|_{\min} \le \frac{V_{FS}}{2^{N+1}} \tag{7}$$

The linearity of the fine ADC determines the overall achievable linearity of the ADC. However, since the residue amplifier provides gain, the linearity requirements are reduced by this gain factor. The comparison window for the internal reference voltages is given by:

$$\left.\begin{aligned} \Delta V_{|\max} &= V_{FS}\frac{\Delta R}{\sum_{j=1}^{N} R_j} \\ \Delta V &= I_{ref}\Delta R \end{aligned}\right\} \Rightarrow -\frac{I_{ref}\sum_{j=1}^{N} R_j}{2^{N+1}} \le \Delta V \le \frac{I_{ref}\sum_{j=1}^{N} R_j}{2^{N+1}} \tag{8}$$

where I_{ref} is the reference current in the resistor ladder DLPM, V_{FS} is the full scale of the converter, R_j is the value of each resistor in the resistor ladder, and N is the total number of resistor in the ladder,

B. DLPM Selection

From the previous analysis one can conclude that the gain, decision and ladder stages of the ADC are crucial to the ADC's proper behavior. To mimic the DUT behavior, the gain-based DLPM and decision stage-based DLPM are extracted (replicated) from the circuits (amplifiers, comparators) of that particular part of the DUT, which they are meant to observe. The DLPM measurements are directly related to asymmetries between the branches composing the circuit, giving an estimation of the offset when both DLPM inputs are grounded. The gain-based monitor consists of the circuitry replicated from the observed ADC gain stage, which is in most cases a differential input pair with active or resistive loading. The test strategy for the proposed decision stage monitor circuit, which is the replica of the observed comparator decision stage, is based on breaking the regeneration feedback in the latch and sensing process mismatches through the measurement of output offset. In addition to these two, internal reference voltages monitoring, the circuit senses the mismatch between two of the unit resistors used in the actual resistor ladder design. The current that flows through the resistors (whose values are extracted from the ladder itself) is fixed using a current mirror. The voltage drop over the resistors is a measurement of the mismatch. By extracting the DLPM circuit from the DUT itself, the DLPM circuit accomplish some desirable properties: *i)* maximize the sensitivity of the circuit to the target parameter to be measured, *ii)* matches the physical layout of the extracted device under test, *iii)* it is small and stand alone, and consumes no power while in off state, and *iv)* the design of DLPM is flexible enough to be applied in several ways depending on the system-on-chip to which it is added.

C. Test Results

To evaluate the test scheme illustrated in Figure 3 consider the test results shown in Figure 7. A 'pass' DLPM test event denotes the measurement inside the comparison window, while a 'fail' DLPM test event is obtained with a slightly narrower comparison window. At the end of the evaluation time the test output is a go/no-go digital signal, which combines the result of the detector test and the DLPM test. Note that the implementation of the clock generation circuitry needs a control signal to set the initial conditions in the D-flip-flops to a known value. This signal is triggered by the rising edge of the *enable* signal. By sweeping the reference voltage until a change in the decision occurs, information about the process variation effects can be extracted as shown in Figure 8. To employ the test method to evaluate the DUT, a discrimination window for various DLPMs has been defined according to the rules of the multi-step ADC error model. A total of 125 DLPMs have been placed in and around the partitioned DUT. As shown in Figure 9, parameter variation effects of 105 DLPMs fall inside the discrimination window, while 20 results are characterized as faulty ones. Let us take three random "pass" DLPMs and a failing one. Without loss of generality, let us assume that these are the four measurements of one set of DLPMs. In practice, repetitive single-DLPM measurements are performed to minimize noise errors; the number of measurements depends upon the test time budget.

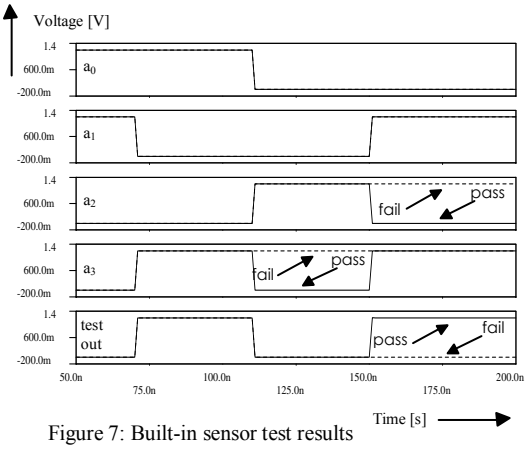

Figure 7: Built-in sensor test results

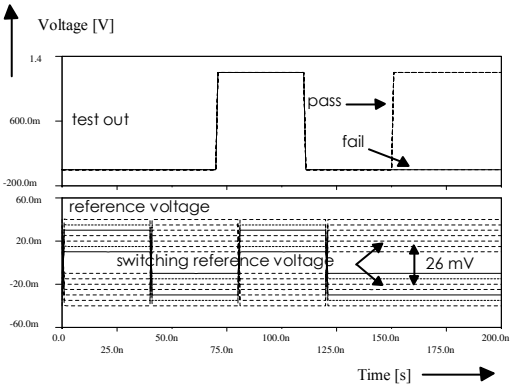

Figure 8: Sweeping the reference voltages to extract the DLPMs offset voltage values, illustrated on the decision DLPM

Each measurement is weighted depending upon the DLPM spatial position and its corresponding matching structure in the circuit under test. In general, it holds that measurements of DLPMs spatially closer to their matching structures have a greater weight than measurements of other non matching DLPMs. In other words, the farther the structure from its matching DLPM is, the lower the assigned weight is. We evaluate the chances that the devices are faulty from the summation of the weighted variances σ_w of these measurements with respect to the expected mean value as

$$-\frac{V_{FS}}{2^{N+1}}G^{i-1} \le \sigma^2_{w\_total} = \frac{1}{N_m}\sum_{n_m=1}^{N_m}\frac{\sigma^2_{w_{n_m}}}{w_{n_m}} \le \frac{V_{FS}}{2^{N+1}}G^{i-1} \qquad (9)$$

for N_m number of measurements and N bit resolution.

Figure 10 illustrates the above-mentioned approach. Namely, we see mean value extracted from Figure 9, the weighted sigmas of each measurement and their relative position to the actual test limits. We regard the device as probably faulty if it falls outside the limits given by equation (9). Typical circuit design is based on worst-case process variability conditions to ensure circuit functionality in various process corners.

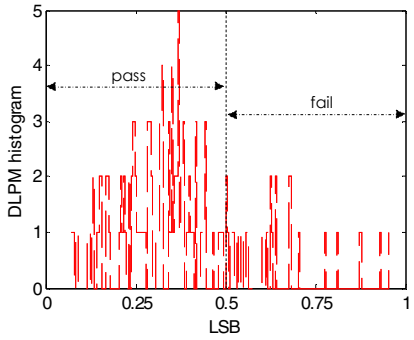

Figure 9: DLPM histogram

This has as drawback that the circuit is bigger, is power hungry and it is much more difficult to reach the desired specs. Thus, it would be better to choose simply a more "relaxed" design condition.

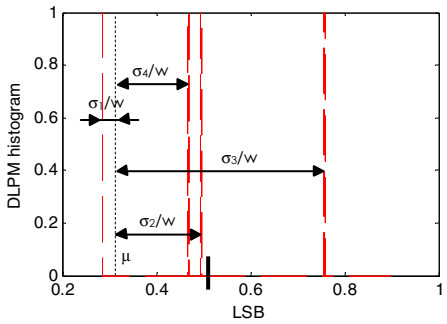

Figure 10: Four measurements of one set of DLPMs

Statistical data extracted through the DLPM measurements allows us to characterize current process variability conditions (process corners) of certain parameters of interest, enabling the optimized design environment.

Similarly, as shown in Figure 9, for the current process and current design there is a yield fall off caused by shifting of the process related LSB window. This process related information allows design re-centering based upon the most failing DLPMs.

On the fly test limit setting is also possible from statistical DLPM data. For instance, if an actually measured parameter distribution is known, the high and low limit values can be updated in the corresponding functional test specs of the device under test leading to the increased yield.

IV. Conclusions

With the use of built-in process monitors, which exploit knowledge of the circuit structure and the specific defect mechanisms, we facilitate early and fast identification of excessive process parameter variation effects in production tests at the cost of at maximum 10% area overhead. The device is characterized as a probably faulty if the average sum of the weighted DLPM measurements is not within the discrimination limits extracted from the DUT architecture restrictions and linearity specifications. Beside the economic considerations, other advantages of providing die-level process variation observability include increased fault coverage and improved process control, diagnostic capabilities, reduced IC performance characterization time-cycle, simplified test program development and easier system-level diagnostics.

Acknowledgements

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