Practical Implementation of a Network Analyzer for Analog BIST Applications

Manuel J. Barragán, Diego Vázquez, and Adoración Rueda
Instituto de Microelectrónica de Sevilla/Centro Nacional de Microelectrónica/Consejo Superior de Investigaciones Científicas (IMSE-CNM-CSIC)/Universidad de Sevilla
Ed. CICA-CNM, Av. Reina Mercedes s/n, 41012 Sevilla, Spain.
e-mail: {manuelj, dgarcia, rueda}@imse.cnm.es

Abstract

This paper presents a practical implementation of a network analyzer for analog BIST applications. The network analyzer consists of a sinewave generator and a sinewave evaluator based on switch-capacitor techniques. Both the generator and the evaluator have been integrated in a 0.35 μm CMOS technology. The functionality of the system has been proved in the lab. For this purpose, a demonstrator board has been developed including the proposed network analyzer and a filter as DUT. Measurements in the lab demonstrate a dynamic range of 70dB in the frequency range up to 20kHz.

I. Introduction

Nowadays, complex mixed-signal electronic systems are extensively developed. Consequently, the increasing cost associated with testing these complex systems have motivated research efforts to explore more efficient testing methodologies. This issue is identified in the SIA Roadmap for Semiconductors [3] as one of the key problems for current and future mixed-signal SoCs.

Usually the test of the analog parts represents the main bottleneck in this line. Traditional test methods for analog circuits rely in functional tests, demanding high quality input stimuli, and high data volume acquisition and processing capability. Moreover, the sensitivity of analog cores to the test conditions and process variations make their test a difficult task which requires expensive ATEs (Automatic Test Equipment).

BIST (Built-In Self-Test) schemes are a well accepted technique to overcome some of the problems cited above. These schemes consist of moving part of the required test resources from the ATE to the chip [3]. BIST applications demand the attributes of low speed digital interface needs with ATE, programming capability, robustness against environmental noise and process variations, and low design effort and area overhead.

Frequency response characterization is a key task in the test of analog cores. The main specifications of many analog building blocks are related to their frequency response, but this test procedure is one of the most expensive due to the required equipment.

Many interesting works have paid attention to this issue. Thus, the works in [4], [5] use DSP techniques to estimate the frequency response of a DUT, while the use of analog multipliers is discussed in [6] and [7]. The work in [8] presents a BIST scheme for the frequency response and harmonic distortion characterization of a DUT based on a switched-capacitor (SC) sinewave generator to provide the test stimuli, and a programmable bandpass filter plus an amplitude measurement block which evaluate the test output. This approach, although simple and cost-effective, is limited to applications demanding a dynamic range below 40dB up to 10kHz, and the frequency response extraction only deals with the magnitude characterization. The work in [9] presents a BIST approach for frequency response testing based on ΣΔ modulation techniques for both test stimuli generation and evaluation. However, that work is signature-based, performing only a structural test of the DUT and not a functional frequency response characterization.

This work presents an on-chip network analyzer suitable for BIST architectures that can cope with the frequency response, both magnitude and phase, and the harmonic distortion of a DUT, providing a dynamic range greater than 70dB up to 20kHz.

This paper is organized as follows: Section II describes the proposed BIST scheme, while the design of its building blocks is discussed in Section III. Section IV presents experimental results obtained from integrated prototypes fabricated in a standard CMOS 0.35 μm technology. Finally Section V summarizes the conclusions.

II. System description

The block diagram of the proposed network analyzer is shown in Fig.1. It consists of a sinewave generator based on a modified 2nd-order filter structure [1], a signature extractor based on a ΣΔ modulation [2], a DSP for signature processing, and some digital control and clocking circuitry.

The system operates based on an external master clock, at frequency f_{eva}. A 1:6 frequency divider generates the

978-3-9810801-3-1/DATE08 © 2008 EDAA

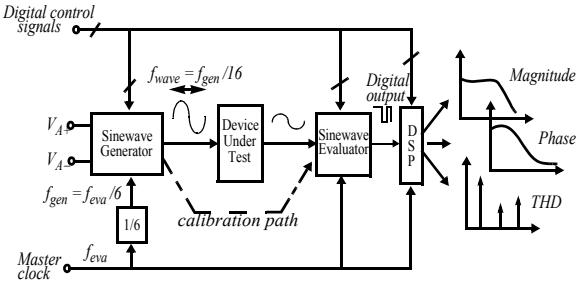

Fig. 1: Network analyzer block diagram

appropriate clock frequency, $f_{gen}=f_{eva}/6$, for the generator block from the master clock. As it will be explained later, the sinewave generator, based on time-variant filtering techniques, delivers a sinewave signal with a frequency $f_{wave}=f_{gen}/16= f_{eva}/96$. The amplitude of the generated signal can be programmed through the DC voltages V_{A+} and V_{A-}. The response of the DUT to the generated stimulus is fed to the evaluator block. This block performs a double modulation of the DUT output signal, square-wave and ΣΔ, and then delivers the output bitstreams to a DSP to extract the frequency response parameters. Since the ΣΔ modulation is controlled by the master clock, f_{eva}, the oversampling ratio in the modulation, $N=f_{eva}/f_{wave}$, is set, by construction, to $N=96$.

This inherent synchronization is an important feature in the proposed scheme: both the generated stimulus frequency and the ΣΔ modulation in the evaluator are accurately controlled by the master clock. That is, the oversampling ratio keeps constant when sweeping the master clock frequency.

The calibration path illustrated with a dashed-line arrow has a double function. On the one hand it allows the verification of the BIST circuitry functionality by bypassing the generated test stimulus to the sinewave evaluator. On the other hand, it allows the characterization of the DUT test input. The information of the test input is essential for the functionality of the network analyzer to relate the DUT input and output signals.

III. Building block design

A. Sinewave Generator

There are several works on the generation of sinewave signals, [8]-[12]. A classical solution is the analog oscillator composed by a filtering stage and a non-linear feedback mechanism [10]. In this case, the quality of the generated signal depends strongly on the shape of the non-linear mechanism and the filter selectivity.

Other approaches adapt digital techniques. For example, the works in [9] and [11] exploits the use of ΣΔ encoded bit-streams that can be stored on a memory or a register while the shape of the filter is matched with the noise shaping characteristic of the bit-stream to remove the undesired noise. This solution requires however a large selective filter (at least one order larger than the order of the ΣΔ encoding scheme) and large bit streams, which may means a large area overhead.

A common element of all theses approaches is the front-end filtering stage to remove the unwanted frequency components. In the case of sinewave generators, such filtering is unavoidable to reduce the level of the harmonic components in order to obtain a high quality signal.

In [1] the authors extended and improved the works in [8] and [12] to present a high performance solution very suitable for BIST applications as the required circuitry is mainly reduced to the unavoidable filter and a very simple digital control circuitry.

Fig.2 shows the generator schematic. Table I lists the values of the design parameters, and Fig.3 shows the

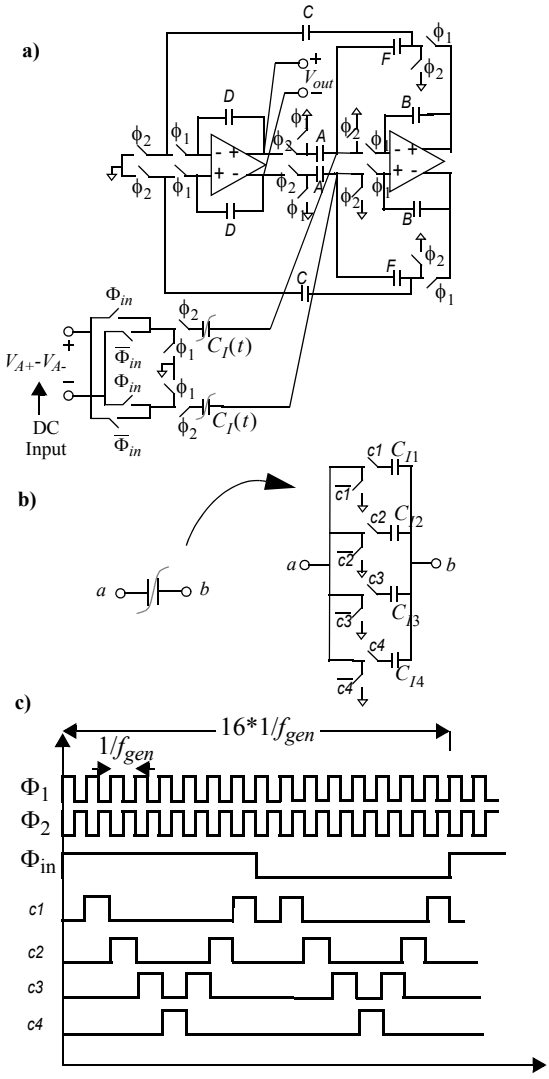

Fig. 2: a) Block diagram of the signal generator. b) Time variant capacitor implementation. c) Time diagram

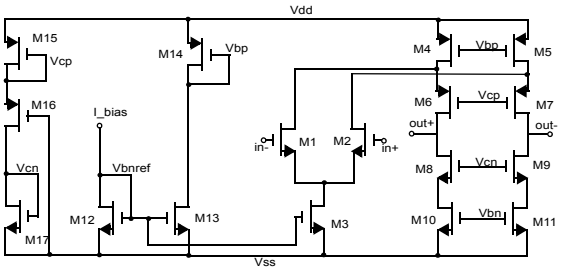

Fig. 3: Fully differential folded-Cascode amplifier.

transistor level schematic of the folded-cascode fully-differential amplifier used in the implementation. The common mode feedback is provided by a dynamic circuit, not shown for simplicity.

A	5.194	**D**	2.574
B	12.749	**F**	1.014
C	1	C_{in}	$C_I(t)$

Table I:Normalized capacitors values

The sinewave generator consists of a fully-differential biquad whose input capacitors have been replaced by an array of four capacitors (C_{I1} to C_{I4}) as depicted in Fig.2b, which are connected in parallel and to the signal path sequentially, according to the time scheme shown in Fig.2c. This time-variant input scheme generates the required steps of a positive half sinewave, while the input switching scheme controlled by signal Φ_{in} (in Fig.2c) sets the weight (positive of negative) of the step. That is, the input capacitor can be described as

$$C_I(t) = \left\{ \Phi_{in}(t) - \overline{\Phi}_{in}(t) \right\} \sum_{k=0}^{4} c_k(t) C_{Ik} \qquad (1)$$

where

$$C_{Ik} = 2\sin\frac{k\pi}{8} \qquad k = 0, 1, \ldots 4 \qquad (2)$$

As it was demonstrated in [1] the output of this system is a filtered version of the quantized sinewave described in (2). Both output amplitude and frequency can be controlled: the amplitude of the generated signal by the input DC level V_{A+}–V_{A-}, and the output frequency, f_{wave}, can be controlled by the clock frequency, $f_{wave} = f_{gen}/16$.

B. Sinewave Evaluator

The use of ΣΔ encoding schemes has been proved to be very efficient for on-chip signal evaluation [9],[13],[14].

The proposed sinewave evaluator is similar to the signature extractor proposed in [9], but its functionality is improved and extended to cope with high precision functional characterizations.

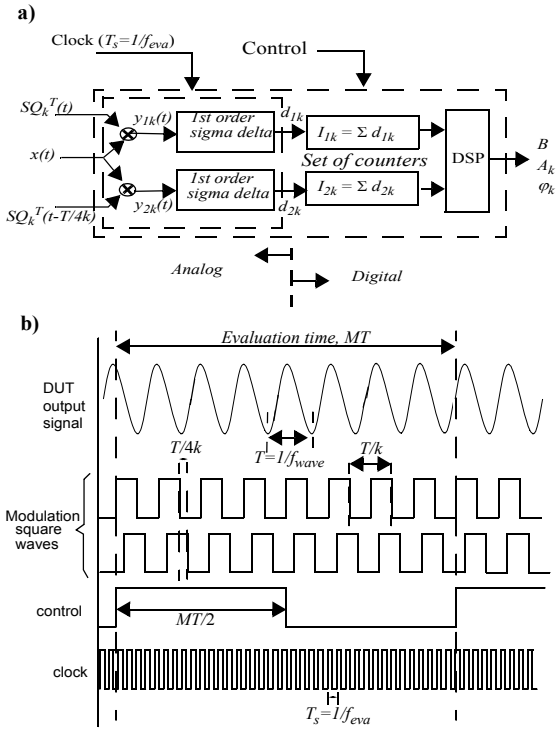

Fig. 4: a) Block diagram of the sinewave evaluator. b) Timing diagram.

Fig.4. depicts a block diagram of the evaluator together with an example of the timing diagram. Its functionality can be briefly described as follows. The signal under evaluation $x(t)$ is modulated by two square waves in quadrature, $SQ_k^T(t)$ and $SQ_k^T(t\text{-}T/4k)$, of amplitude 1 and period T/k, where $T=1/f_{wave}$ is the period of $x(t)$ and k is an integer. The resulting signals $y_{1k}(t)$ and $y_{2k}(t)$ are fed to two matched 1st-order ΣΔ modulators. The generated bit-streams d_{1k} and d_{2k} are integrated along an integer number M of periods of the signal under evaluation using a set of counters to obtain the signatures I_{1k} and I_{2k}. These signatures are then processed using basic arithmetic operations in the digital domain (represented by the DSP block in Fig.4a) to cancel the offset contribution of the modulators and to obtain the main parameters of $x(t)$: DC level, amplitude of the harmonic components and their corresponding phase shifts. Namely, if M is even and $N/2^3k$ is an integer number, where N is the oversampling ratio in the modulator defined as $N=T/T_s$ (where $T_s=1/f_{eva}$ is the sampling period), then the DC level, B, the amplitude of the k-th harmonic, A_k, and its phase shift with respect to $SQ_k^T(t)$, φ_k, can be ensured to be confined in bounded intervals given by [13],

$$B \in \frac{1}{MN}[I_{10} - \varepsilon_{10}, I_{10} + \varepsilon_{10}] \;\; or \;\; \frac{1}{MN}[I_{20} - \varepsilon_{20}, I_{20} + \varepsilon_{20}] \qquad (3)$$

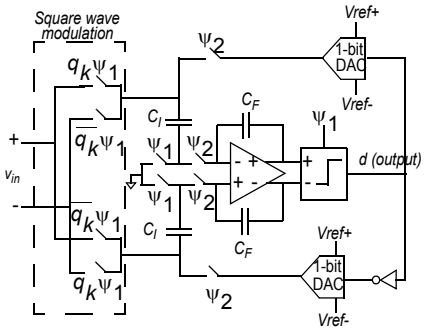

Fig. 5: Sigma-delta modulator with square-wave input modulation

$$(A_k)^2 \in \left(\frac{\pi}{2}\frac{1}{MN}\right)^2 \left[\begin{array}{l} min\left\{(I_{1k}+\varepsilon_{1k})^2+(I_{2k}+\varepsilon_{2k})^2\right\}, \\ max\left\{(I_{1k}+\varepsilon_{1k})^2+(I_{2k}+\varepsilon_{2k})^2\right\} \end{array}\right] \quad (4)$$

$$\tan\varphi_k \in \left[min\left(\frac{I_{1k}+\varepsilon_{1k}}{I_{2k}+\varepsilon_{2k}}\right), max\left(\frac{I_{1k}+\varepsilon_{1k}}{I_{2k}+\varepsilon_{2k}}\right)\right] \quad (5)$$

where $\varepsilon_{1k}, \varepsilon_{2k}$ (k= *0, 1, 2,...*) are unknown error terms (due to the quantization noise in the modulator) but limited to $\varepsilon_{1k}, \varepsilon_{2k} \in [-4, 4]$. So, the relative errors of the measurements can be reduced by increasing the total number of samples (MN).

This analyzer approach has different attributes that make it very interesting for BIST applications. Thus, the required analog circuitry is limited to 1st-order modulators, while its simplicity and robustness is well known. Moreover, most of the signal processing is made in the digital domain. It opens the possibility to integrate it on-chip or to be realized externally with a digital ATE. For this reason, we have decided to integrate only the analog part in a first demonstrator.

Fig.5 shows the schematic of the implemented fully differential first-order ΣΔ-modulator with input square-wave modulation. The ratio C_I/C_F in Fig.5 has been fixed to 0.4 in order to avoid saturations effects in the amplifier while maintain a moderate gain in the integrator. The switching input interface has been properly modified for this application. It operates with two non-overlapping clock phases (ψ_1 and ψ_2) and a digital control signal q_k. It is easy to show that depending on the logic value of q_k (high or low), the weight of the sampled input (*Vin*) is positive or negative. This switching scheme has been used to perform the required square-wave modulation in the ΣΔ modulator itself.

To simplify and reduce the design effort, the amplifier shown in Fig.3 is used in both the sinewave generator and the ΣΔ modulator composing the sinewave evaluator. A simple comparator based on a dynamic latch has been selected for the clocked comparator in Fig.5.

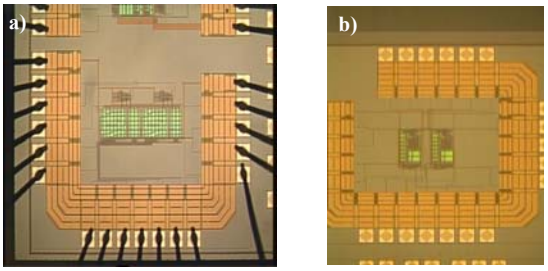

Fig. 6: Microphotographs: a) Sinewave generator, b)Sinewave evaluator

The digital part of the evaluator has not been integrated. Nevertheless, an area overhead estimation can be given. A non-optimized direct synthesis from a VHDL description of the strategy presented in [13] for 16-bit word lengths and using a standard-cell library in a 0.35 μm technology takes an area of 300μm x 300μm approximately.

C. Network Analyzer

The inherent synchronization between the sinewave generator and the sinewave evaluator makes possible the direct application of equations (4) and (5) to compute the amplitude of the DUT response and its phase shift with respect to the modulating square wave, respectively. Nevertheless, a network analyzer relates the DUT input and output signals to obtain the DUT gain and phase shift. So the test input must be also characterized. This is done just by bypassing the DUT, feeding the generated waveform directly to the evaluator block and computing its amplitude and phase shift. This calibration allows to evaluate the gain of the DUT as the ratio of the DUT output and input amplitude measurements, and the phase shift between both signals as the difference between the DUT input and output phase shifts. Since the amplitude and phase shift of the generated stimuli are accurately and externally set by the DC voltage V_{A+}–V_{A-} and the digital control signals c_k, respectively, this calibration only needs to be performed once.

IV. Experimental results

The presented sinewave generator and evaluator were fabricated in a standard CMOS 0.35μm technology. Fig.6 shows microphotographs of both systems. The sinewave generator occupies an area of 0.15mm^2 while the sinewave evaluator occupies only 0.065mm^2.

As a proof-of-concept, the network analyzer shown in Fig.1 has been built on a test board. An active-RC 2nd order low-pass filter has been included as DUT to evaluate the performance of the proposed scheme. The general test set-up is depicted in Fig.7. It makes use of the Agilent 93000 test system. It generates the digital control signals

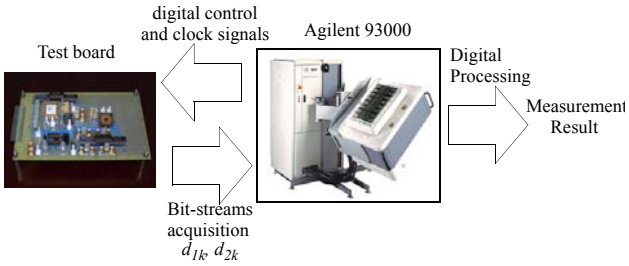

Fig. 7: Test set up.

and clock, provides the supply and analog reference voltages, and acquires and processes the digital output of the evaluator acting as the DSP block in Fig.1.

A. Sinewave Generator

Fig.8a shows three output waveforms from the sinewave generator. The frequency of the signal is 62.5kHz. The amplitudes are 300mV, 500mV and 600mV, corresponding to the reference voltages ±75mV, ±125mV, and ±150mV, respectively. Fig.8b shows the measured spectrum for a 62.5kHz signal with an amplitude of 1Vpp. The SFDR is 70dB and the THD is 67dB. However, it is worth to mention that these results correspond to the continuous-time analysis of a sampled signal. A discrete-time application will improve these figures.

B. Sinewave Evaluator

Fig.9 shows the measurements, relative to the full scale range of the modulator, of a multitone signal composed by three harmonic components: A_1=0.2V, A_2=0.02V, and A_3=0.002V. This signal is generated by the Agilent 93000 and fed directly to the evaluator. The oversampling ratio was fixed to N=96, while the number of periods M taken for the evaluation has been varied from M=20 to M=1000. Twenty-five runs of this experiment were carried out to demonstrate that the measurements are repeatable. It is clear to see how the measurements of the second and third harmonics are 20dB and 40dB below A_1. Also, Fig.9 shows that the error in the measurements decreases as M increases, achieving sensitivities of fractions of dBm very quickly. In other words, because of this important feature, the evaluator does not limit the dynamic range of the

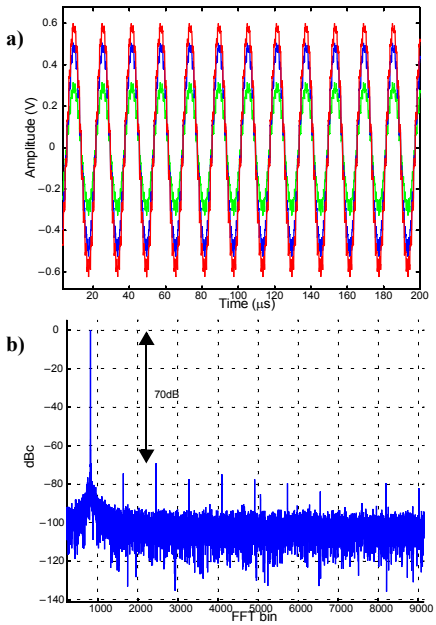

Fig. 8: a) Generator output signals.
b) Output signal spectrum.

network analyzer, since the accuracy of the evaluation can be selected by choosing a proper number of periods for the evaluation, M. So, in last instance the main limitations in this line, to a first order, is given by the available test time.

C. Network Analyzer

To prove the performance of the proposed network analyzer, the magnitude and phase response characterization of the selected DUT was carried out. The employed DUT is an active-RC 2nd-order low-pass filter with a cut-off frequency of 1 kHz. Fig.10a and b show the obtained Bode magnitude and phase diagrams. Measurements were performed taking 200 periods for the evaluation. Accordingly to (4) and (5), the relative error increases as the response magnitude decreases. If a better precision is needed, it can be achieved increasing the number of evaluation periods.

The harmonic-distortion measurement capabilities are verified in Fig.10c. This figure shows the estimation of the

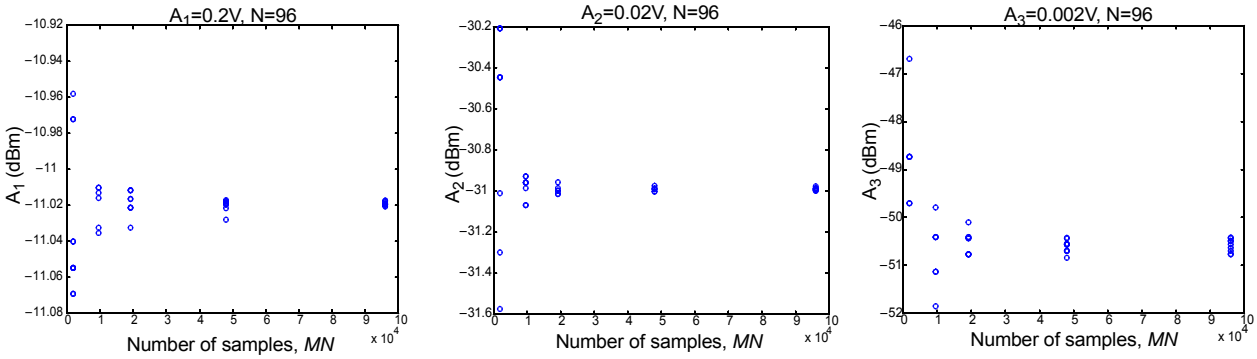

Fig. 9: Harmonic component measurements as a function of the number of samples.

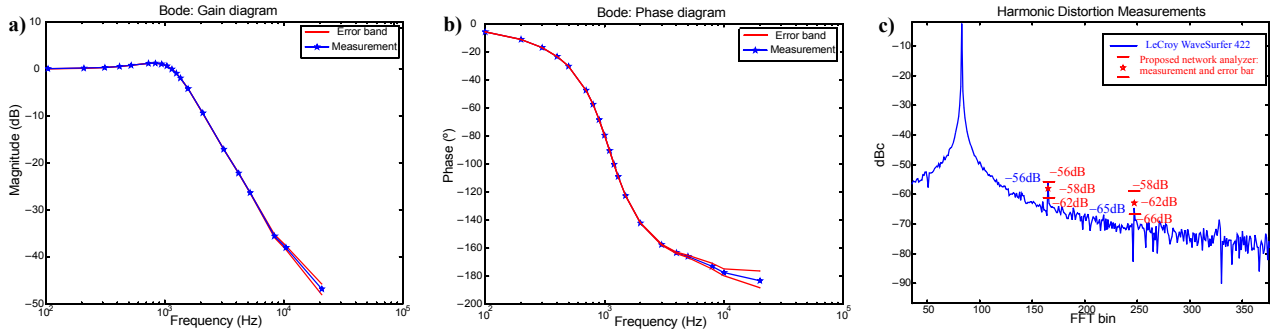

Fig. 10:a) Magnitude response. b) Phase response. c) Harmonic distortion measurement.

second and third harmonic components of the filter output when its input is set to a 800mVpp, 1.6kHz sinewave signal. The solid line is the spectrum measured with a digital oscilloscope. The agreement between the commercial system and the proposed network analyzer is excellent. Harmonic distortion measurements were performed taking 400 periods for the evaluation. Again, if a better precision is needed, it can be achieved just by increasing this number.

V. Conclusions

A practical network analyzer for analog BIST applications has been presented. The proposed scheme allows the on-chip frequency response characterization, both magnitude and phase, and the harmonic distortion estimation of an analog DUT in the range of audio. The developed network analyzer has the attributes of digital programming and control capabilities, robustness and reduced area overhead, what make it suitable for BIST applications.

The main building blocks of the proposed network analyzer have been implemented in a standard CMOS 0.35µm technology. Some design considerations and experimental results for the different building blocks were provided. The proposed scheme has been validated on a test board which demonstrates the feasibility of the approach.

The presented network analyzer has been proved to be suitable for the characterization of analog circuits in the frequency range up to 20kHz, with a dynamic range up to 70dB.

ACKNOWLEDGEMENTS

The authors thank José Miguel Mora Gutiérrez for his invaluable help with the Agilent 93000 test system.

This work has been funded in part by the Spanish Government through the project TAMBIST, under contract TEC2004-02949/MIC, and the Junta de Andalucía through the Proyecto de Excelencia TIC-927.

REFERENCES

[1] M. J. Barragán, D. Vázquez, and A. Rueda, “Practical Implementation of Sinewave Generators for Mixed-Signal BIST”, Proc. of the 8th Latin American Test Workshop (LATW’07), Cúzco, Perú, 2007

[2] M. J. Barragán, D. Vázquez, and A. Rueda, “A Sinewave Analyzer for Mixed-Signal BIST Applications in a 0.35 µm technology”, Proc. of the 9th IEEE Workshop on Design and Diagnostics of Elec. Circ. and Sys., Prague, 2006

[3] SIA Roadmap for semiconductors. http: //public.itrs.net

[4] M. M. Hafed, et al, “A 4GHz Effective Sample Rate Integrated Test Core for Analog and Mixed-Signal Circuits”, IEEE J. Solid State Circuits, vol. 37, no 4, pp. 499-514, 2002

[5] M. Negreiros, L. Carro, and A. A. Susin, “A Statistical Sampler for a New On-Line Analog Test Method”, J. Electronic Testing vol.19, no5, pp. 585-595, 2003.

[6] A. Valdés-García, et al. “An Integrated Frequency Response Characterization System With a Digital Interface for Analog Testing”, IEEE J. Solid-State Circuits, vol. 41, no 10, pp.2301-2313, 2006

[7] A. P. Jose et al. “On-Chip Spectrum Analyzer for Analog Built-In Self-Test” Proc. of the 23rd IEEE VLSI Test Symposium (VTS’05), 2005

[8] M. G. Méndez-Rivera, et al. “An On-Chip Spectrum Analyzer for Analog Built-In Testing”, J. Electronic Testing, vol 21, pp. 205-219, 2005

[9] G. Prenat, et al, “A Low-Cost Digital Frequency Testing Approach for Mixed-Signal Devices Using ΣΔ Modulation” Elsevier Microelectronic Journal vol. 36 (2005) pp. 1080-1090

[10] J. Galan, et al. “A low-power low-voltage OTA-C Sinusoidal oscillator with a large tuning range”, IEEE Trans. on Circ. and Systems, vol. 52, no 2, 2005.

[11] B. Dufort and G. W. Roberts: “On-chip analog signal generation for mixed-signal Built-In-Self-Test”. IEEE J. Solid-State Circuits, 1999, Vol 33, N 3, pp. 318-330

[12] H. C. Patangia and B. Zenone: ”A programmable switched-capacitor sinewave generator”. Proc. of 37th Midwest Symp. on Circ. and Systems, 1994, pp. 165-168.

[13] D. Vázquez, et al: ‘Sine-wave signal characterization using square-wave and ΣΔ modulation’, J. Electronic Testing, vol. 21, pp. 221-232, 2005

[14] H. C. Hong et al., ‘Practical considerations in applying sigma-delta modulation-based analog BIST to sampled data systems’, IEEE Trans. on Circuits and Systems-II, vol. 50, no 9, pp. 553-566, 2003