Fabrication of gold nanowires on insulating substrates by field-induced mass transport

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A method for the fabrication of nanometer size gold wires on insulating surfaces is presented. An oscillating gold-coated atomic force microscope tip is brought into close proximity of a silicon dioxide surface. The application of a negative sample voltage produces the transport of gold atoms from the tip to the surface. The voltage is applied when there is a tip–surface separation of ~3 nm. The finite tip–surface separation enhances the tip lifetime. It also allows the application of sequences of multiple voltage pulses. Those sequences allow the fabrication of continuous nanowires. The atomic force microscope gold deposition is performed at room temperature and in ambient conditions which makes the method fully compatible with standard lithographic techniques. Electron transport measurements of the wires show a clear metallic behavior. Electrical resistivities of $\sim 3\times10^{-7}\ \Omega$ m and current densities of up to 5×10^{11} A m^{-2} are reported. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1408911]

Several methods based on scanning probe microscopy (SPM) have been proposed for the fabrication of gold nanowires.[1–5] The most extended method to fabricate and measure the electrical properties of gold nanowires consists of establishing mechanical contact between a gold tip and a flat and clean surface, usually Au(111). This approach has allowed the study of the electrical transport through monoatomic chains of gold atoms.[3,6] Stockman *et al.*[4] were able to use a scanning tunneling microscope to pattern Langmuir–Blodgett films and fabricate metallic gold wires on SiO_2 surfaces. Recently, Ramsperger *et al.*[5] have demonstrated that gold nanowires could be fabricated on a Si(111) surface by establishing a gentle contact between a gold-coated atomic force microscope (AFM) tip and the surface. The mass transfer is inhibited if the surface is oxidized or covered with adsorbed layers. A successful fabrication implies ultrahigh vacuum requirements.

The restriction to SPM interfaces,[1–3] the complexity of the method,[4] or ultrahigh vacuum requirements[5] place severe limitations on the ability of SPM to fabricate gold nanowires on a routine basis. In this letter, we present a method to fabricate gold nanowires on insulating substrates by using an AFM operated in noncontact mode.[7] The method is based on the field-induced metal transport from the AFM tip to the insulating substrate.[8,9]

The experiments were performed with an AFM (Nanoscope III, Digital Instruments) operated at room temperature and ambient pressure. Gold-coated silicon cantilevers (10 nm Cr/100 nm Au) were used. The force constant (k_c) and resonance frequency (f_0) of the cantilevers were about 30 N/m and 314 kHz, respectively. The cantilever was excited at its resonance frequency. Si(100) surfaces with native oxides of about 2 nm and thermal SiO_2 of 4.3 nm were used as substrates.

A combination of electron beam and optical lithography are used to define a set of electrodes and conducting pads to connect the nanowires to the testing equipment. The procedure to fabricate the nanowires has the following steps. First, an AFM operated in the noncontact mode images the gap region between the probing electrodes. Second, the AFM tip is placed ~5–10 nm above the surface. The tip oscillates with an oscillation amplitude of ~5 nm, i.e., always smaller than the average tip–surface separation. This prevents tip–surface mechanical contact. To transfer gold atoms from the tip to the surface, voltage pulses in the 15–20 V range and 0.5–5 ms are applied. To prevent the formation of local silicon oxides during the deposition process,[10] the sample is biased negatively with respect to the tip. Each voltage pulse produces a gold dot on the insulating surface. The nanowire consists of a succession of gold dots which separations are smaller than their diameter. Figure 1 schematizes the deposition procedure.

Figure 2(a) shows the end of two probing electrodes fabricated by electron beam lithography on a native oxide silicon surface. The electrodes are separated by a gap of 510 nm. The electrodes were formed by thermal evaporation of 5 nm of Cr followed by 10 nm of Au. At the far end (not seen in the image) the electrodes overlap with large and thicker conducting pads made by photolithography. Figure 2(b) shows an intermediate stage of the nanowire fabrication pro-

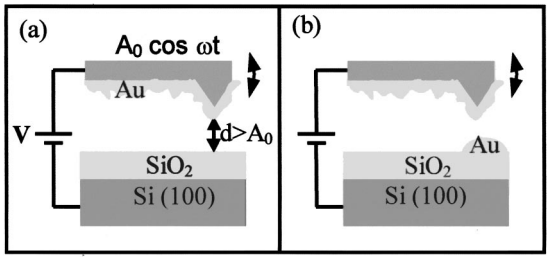

FIG. 1. Schematics of the gold deposition are shown. (a) A gold-coated oscillating tip is brought close to the surface. (b) The application of a voltage pulse between tip and sample produces the gold transport from the tip to the surface.

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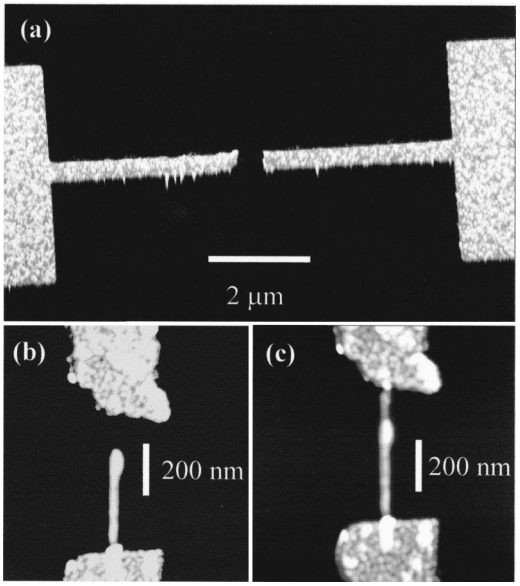

FIG. 2. Sequence of the gold nanowire fabrication is shown. (a) AFM image of the gold probing electrodes before AFM gold deposition is presented. (b) The gap between the electrodes is partially filled by a gold wire. (c) Final aspect of the nanowire bridging the probing electrodes is shown. Nanowire formed by the application of pulses of 0.5 ms at −20 V is presented.

cess. The complete wire bridging both electrodes is shown in Fig. 2(c). The nanowire is 10 nm in height and 40 nm in apparent width. The grain size of the gold film visible in Fig. 2(c). To guarantee the electrical connection of the wire to the probing electrode, several metallic depositions are performed on top of the electrodes (see white spots in the image).

The width of the wire depends on several factors such as the geometry of the tip, voltage strength, and pulse duration. Gold-coated tips usually have a large tip radius ~50–100 nm. This leaves the voltage strength and pulse duration as the only parameters to control the lateral size of the wire. The combination of relatively small voltages (always above a certain threshold) and short pulses produces the smallest dots. By applying voltage pulses of 14 V and 0.5 ms, sub-10 nm wires have been fabricated. However, there is a threshold voltage to produce the formation of a gold dot. The length of the nanowire is limited by the amount of metal deposited on the apex of the tip. This protocol allows one to use the same tip to fabricate nanowires of about 2 μm in length.

Several physical processes have been proposed to explain the formation of nanometer-size gold mounds on gold and silicon surfaces. Field evaporation and dot formation after mechanical contact between the tip and surface have been invoked. Here, due to the absence of tip–sample contact, we favored a process based on the field-induced mass transport from the tip. The field evaporation is also consistent with our observation that, for a fixed separation, the mass transport vanishes if the applied voltage is reduced below a critical value. The minimum total electrical field needed to form a gold dot on silicon oxide is about 2–5 V/nm. We have some incertitude in the measurement of the real tip-conducting substrate separation (~1 nm). This gives rise to some dispersion in the determination of the field evaporation threshold. Nevertheless, the aforementioned values are about one order the magnitude smaller than the values obtained in field ionization microscopy (~35 V/nm) but of the same order than

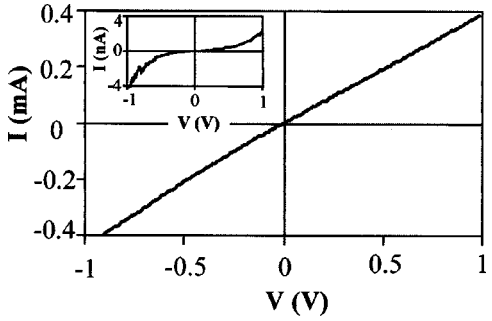

FIG. 3. $I-V$ characteristics for the gold wire of Fig. 2(c) are shown. An ohmic behavior is observed. At large negative voltages (close to −1 V), a slight nonlinear dependence is observed. The inset shows the current flow between the electrodes before the gold wire fabrication. Measurements were performed at room temperature.

those reported by Mamin *et al.*[8] on gold (4 V/nm) and Hosaka and Koyanagi[9] on silicon dioxide (5–6 V/nm).

Figure 3 shows the electrical characteristics of the wire shown in Fig. 2(c). An ohmic (linear) behavior is observed. At negative voltages close to −1 V, a slight nonlinear dependence is observed. The leakage current measured between the electrodes in the absence of the nanowire is five orders of magnitude smaller (inset of Fig. 3).

Metallic nanowires have also been fabricated on thermal grown oxides. Figure 4(a) shows a metallic wire bridging two electrodes on a 4.3 nm SiO_2 layer on Si(100). The corresponding $I-V$ characteristics are shown in Fig. 4(b).

The wires shown in Figs. 3 and 4(b) have resistance values of 1128 Ω and 359 Ω, respectively. To derive those values, we have subtracted the resistance of the probing electrodes from the $I-V$ curves. In both experiments, the current densities through the nanowires have high values ~5

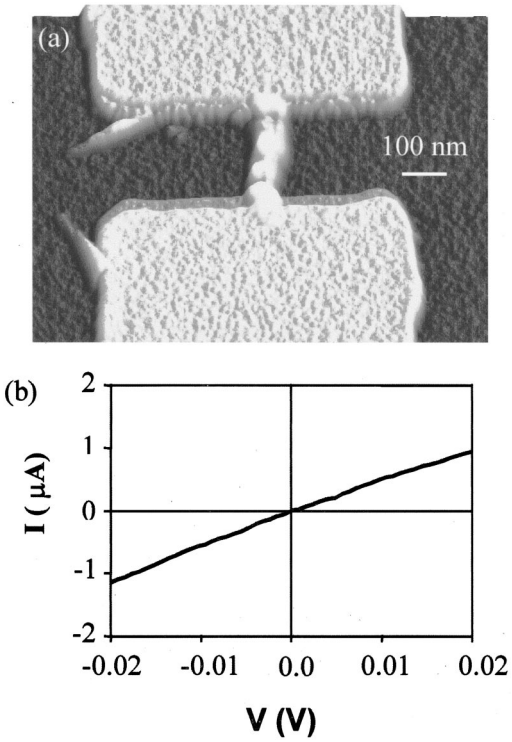

FIG. 4. (a) AFM image of a gold nanowire on a 4.3 nm oxide film is shown. The wire was formed by the application of pulses of 5 ms at −18 V. (b) $I-V$ characteristics of the nanowire obtained at room temperature are shown.

$\times 10^{11}$ A m and 10^{10} A m^{-2}, respectively. However, they are smaller than the failure current density determined for Au nanowires of the same thickness ($\sim 8\times 10^{12}$ A m^{-2}).[11]

The electrical resistivity can be estimated by using $\rho = Rwt/L$, where *w, t,* and *L* are the width, thickness, and length of the wire, respectively. For the gold wire fabricated on the native oxide an electrical resistivity of $9\times 10^{-7}\,\Omega$ m is obtained while the gold wire fabricated on the thermal oxide gives a resistivity of $3\times 10^{-7}\,\Omega$ m. Those values are about one order of magnitude higher than the resistivity of Au bulk ($2.8\times 10^{-8}\,\Omega$ m at room temperature). Nevertheless, they are considerably smaller than the values reported by Ramsperger *et al.*[5] ($\sim 10^{-4}\,\Omega$ m).

Differences between the bulk and thin film resistivities have been extensively reported on the growth of Au thin films on several substrates.[12] The resistivity of a thin film increases when one or more dimensions of the film (nanowire) become comparable with or less than the mean free path ($\sim$30 nm at 300 K). In addition to this effect, these nanowires have a granular structure and electron scattering at the grain boundaries should also become a source of electrical resistance. Here the average grain size is 7 nm.

In short, we report a simple and general method to fabricate metallic gold nanowires on silicon oxide substrates. The method is compatible with other lithographic and microelectronics processes. The absence of a tip–surface mechanical contact enhances the tip lifetime and reproducibility of the process. These features make this method suitable for the fabrication of nanometer-scale devices.

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