Silicon microcantilevers with MOSFET detection

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Abstract

We report the fabrication of silicon microcantilevers with MOSFET detection, to be used in force measurements for biomolecular detection. Thin cantilevers are required for a high force sensitivity. Therefore the source and drain of the transistors have been fabricated by As implantation to obtain shallow PN junctions. The cantilevers have been oriented on the non-standard (100) crystallographic direction of silicon, to maximize the stress response of the NMOS transistors. The force sensitivity and resolution of the cantilevers have been tested by applying a force with an AFM tip. Values of 25 μV/pN and 56 pN respectively have been obtained for a force applied at the tip of a cantilever with a length of 200 μm, a width of 24 μm and a silicon thickness of 340 nm.

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1. Introduction

Silicon microcantilevers, originally developed for atomic force microscopy (AFM), are being increasingly used in the field of biological and chemical sensing [1]. Typically, the cantilever detects the binding of biomolecules to its surface, by measuring either the static cantilever deflection due to surface forces [2] or the change in resonance frequencies due to mass addition [3]. A high sensitivity can potentially be obtained by detecting intermolecular binding forces between a functionalized cantilever tip and a functionalized surface [4]. With the aim of using this method for detecting biomolecules we have previously fabricated piezoresistive polycrystalline silicon cantilevers with [5] and without [6] integrated circuit signal processing. The self-sensing capability of the piezoresistive approach is preferred over optical detection for small cantilevers and for system simplicity. The forces involved in inter molecular binding are in the range of 10-200 pN, which for piezoresistive detection require very low spring constants in the order of mN/m and cantilever dimensions around 100 μm in length, 1 μm in width and <1 μm in thickness [6].

Polycrystalline silicon was used in [5,6] for technological compatibility with the on-chip circuit integration, although it has a lower piezoresistive coefficient than crystalline silicon. We have also fabricated cantilevers on crystalline silicon [7], using N-doped piezoresistors to obtain a small PN-junction depth and orienting the cantilevers on the non-standard (100) direction on the wafer surface to optimize the piezoresistive coefficient. In this work we propose a novel device design in which the u-shaped cantilever deflection is detected electrically by one embedded, long channel, Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

Self-sensing cantilevers with piezoresistive detection have been used for a long time [8-10], but they suffer from high noise which limits their force resolution. MOSFET-based stress detectors can offer improved performances due to their sensitivity to local stress at the channel surface and their better noise properties. They have long been used in MEMS [11] and AFM probes [12], but they have only recently been applied to cantilever sensors [13,14]. In our case the cantilevers are supported by two legs to

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reduce the stiffness, and are oriented in the non standard (100) direction to optimize the piezoresistive properties of the N-type transistors.

2. Device design and fabrication

The cantilevers have been fabricated in <100> SOI wafers with a P-type active layer with a thickness of 340 nm. The fabrication process has 7 photolithographic steps and is schematically shown in Fig. 1. Two MOSFETs in series are fabricated using As implantation (10^{15} cm^{-2} at 100 keV) for source and drain with the channel and the cantilever aligned on <100> direction, i.e. rotated 45º respect to the wafer flat. The (100) longitudinal piezoresistive coefficient for N-type conduction is higher than the normally used (110) orientation for P-type [15]. Indeed, the electron mobility increase in uniaxially stressed MOSFETs has been shown to be higher in the (100) direction than in the (110) direction [16]. This also results in a lower spring constant due to the lower Young modulus of silicon in this direction.

The transistors have an aluminum gate and a non-self-aligned structure. Arsenic is used to obtain a shallow PN-junction, which is required to avoid doping the whole 340 nm cantilever thickness. The first steps define the source and drain of the transistors (Fig. 1.a). Then the cantilevers are defined on the silicon active layer by using a deep reactive ion etching (DRIE) process, suitably tuned for a shallow etch with smooth vertical walls (Fig. 1.b). The As impurities are activated by a thermal treatment at 900ºC. A 400 nm silicon dioxide layer is deposited by plasma-enhanced chemical vapour deposition (PECVD). The transistor gate areas are then opened and the gate oxide is thermally grown to a thickness of 37 nm. The contact windows in the sources and drains are then opened (Fig. 1.c), and a metal layer (0.5 µm Al) is deposited and patterned. A layer of 100 nm of PECVD silicon nitride (not shown in Fig. 1) is deposited and patterned to passivate the conductive areas on the devices. The devices are completed by etching away the silicon substrate from the backside by DRIE, stopping at the buried oxide layer, and releasing the cantilevers by wet etching of the resulting oxide membrane (Fig. 1.d).

Every chip consists of a couple of identical cantilevers (Fig. 2), with lengths L of 200 or 400 μm, a total cantilever width of 24 μm and a leg width of 10 μm. The corresponding spring constants k range from about 0.5 to 4 mN/m. The transistors have a channel width $W_{ch} = 4$ μm and channel lengths L_{ch} of 10 or 20 μm.

3. Results and discussion

We have measured the electrical properties of the transistors and the electromechanical behaviour of the cantilevers. The electrical characteristics $I_D(V_{DS})$ of the transistors have been measured with a semiautomatic probe system Karl Suss PA200 and a semiconductor parameter analyzer HP4155. The transistor characteristics (Fig. 3) present small deviations (3 %) inside the chip and a standard deviation between 6% and 12% on wafer. The non-uniformity was mainly caused by the last step of the fabrication, the release of the cantilevers, in which the aluminium conductors were partially damaged, and it will be improved in future fabrications. It can be seen that the threshold voltage V_{Th} is positive and lower than 1 V. The saturation current I_{Dsat} for $V_{GS}=4V$ increases (from 42.5 μA to 85.0 μA) by decreasing the channel length from 20μm to 10 μm. This agrees with the expected W_{ch}/L_{ch} dependence of I_D in a MOSFET. We have also observed a dependence of I_D on the cantilever length (85.0 μA and 97.3 μA for L=200 μm and 400 μm, respectively, for L=10 μm). This was not expected but it can be correlated to the different residual stress present in the two cantilever designs, which affects the channel mobility.

The electromechanical characteristics of the cantilevers ($L_{ch}=10$ μm and L=200 μm) were obtained by using an AFM to deflect them, as described in [6]. A stiff probe (k= 40 N/m) was used in dynamic mode. The output voltage V_0 of the voltage divider (Fig. 4) was recorded continuously as a function of the cantilever deflection, Δz, for both movements downwards and upwards of the AFM tip after the introduction of an offset signal, amplification and one filter stage. For this signal treatment an application-specific integrated circuit [5] has been used, with a total amplification factor of 630. The

results, averaged over 25 measurements, are shown in Fig. 5. The AFM force was applied at 50 μm from the cantilever clamping edge. The measured displacement sensitivity is $\Delta V/\Delta z = 2.46$ V/μm, from which one can calculate a force sensitivity of $\Delta V/F = 25$ μV/pN for a force F applied at the end of the cantilever. For the analytical calculation we considered that the cantilever is made by two serially-connected elements. The first one is a multilayer beam (20 μm wide and long) clamped to the fixed substrate and composed by silicon, silicon dioxide, aluminium and silicon nitride. The second one is a silicon monolayer beam (24 μm wide and 180 μm long) clamped to the end of the first multilayer element. Considering the following values for the Young moduli ($E_{Si}= 130$ Gpa, $E_{SiO2}=75$ Gpa, $E_{Al}= 70$ Gpa, $E_{Si3N4}= 250$ Gpa) it is possible to calculate the force needed for the measured deflection.

The minimum detectable force is the noise equivalent force, which is defined as the noise voltage divided by the force sensitivity ($F_{min}=V_{noise}/(\Delta V/F)$). The total noise of the cantilever plus circuit was calculated by integrating the power spectral density measured, between 0.1 Hz and 10 kHz, by a dynamic signal analyzer (Stanford Research SR785) yielding a value of 1.4 mV. With these values the minimum detectable force is $F_{min}=56$ pN.

The sensitivity and resolution are not affected by the observed deviations of a few percent in the electrical characteristics of the MOSFETs on different cantilevers, which were produced by deviations on the contacting metals. The sensitivity is related to the relative variation of the electron mobility in the channel due to mechanical stress, and the resolution depends on this and on the noise properties of the transistor.

4. Conclusions

We have fabricated silicon microcantilevers for force measurements with MOSFET detection. The source and drain regions have been defined by shallow PN junctions obtained by As ion implantation. To improve the stress response of the NMOS transistors, the cantilevers have been fabricated parallel to the (100) direction of the

silicon wafer. A force sensitivity and resolution of 25 µV/pN and 56 pN respectively have been obtained for a force applied at the tip of the cantilever.

Acknowledgements

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Figure captions

Fig. 1. Schematic view of the cantilever fabrication process: a) transistor source-drain implantation, b) definition of the cantilever by DRIE etching, c) gate oxidation and definition of the contact windows, d) metallization, backside DRIE to remove the substrate and cantilever release. (S: transistor source; G: gate; D: drain).

Fig. 2. SEM micrograph of a pair of identical MOSFET cantilevers.

Fig. 3. Electrical characteristics of the longitudinal MOSFETs integrated in 200 μm long cantilevers. The devices have a channel length of 20 μm. The two sets of curves (dashed and continuous) correspond to the two cantilevers in the same chip.

Fig. 4. Electronic setup used for the measurement of the electromechanical behavior of the cantilevers. a) Two MOSFETs in series on a single cantilever are connected on a bridge configuration; b) Structure of the ASIC used for signal treatment and amplification.

Fig. 5. Electromechanical response (ΔV in Fig. 4) of the cantilever against the deflection produced by a stiff AFM probe, as described in the text. The amplitude of the AFM cantilever vibration is also shown.
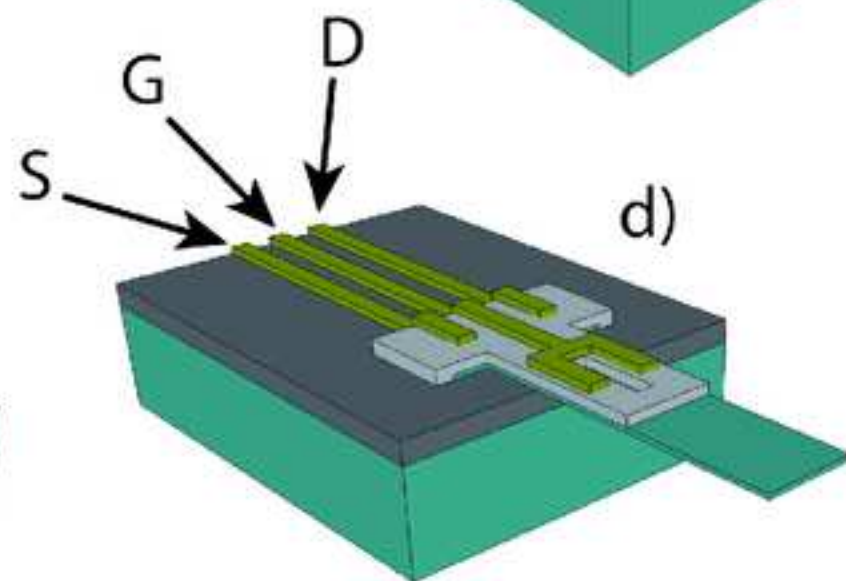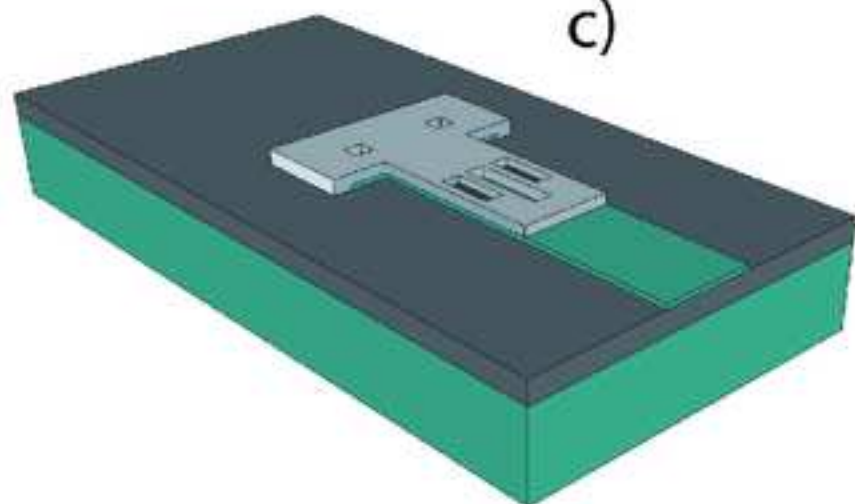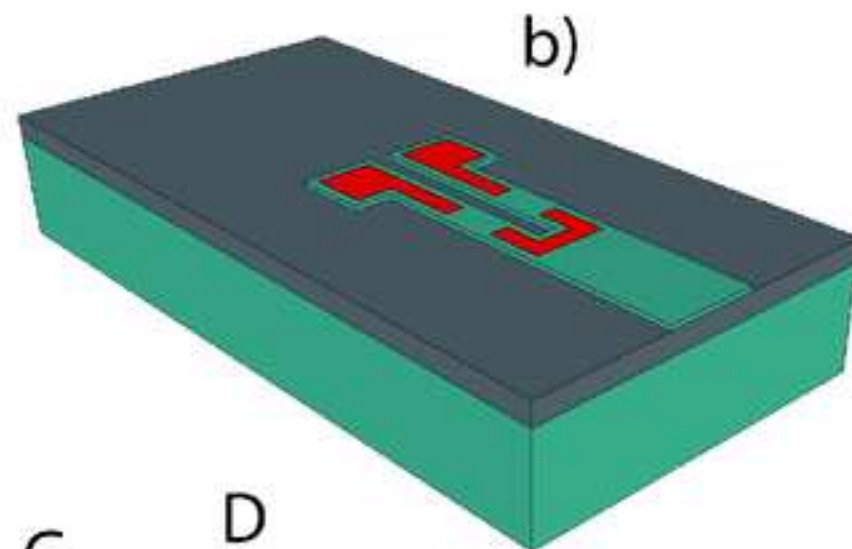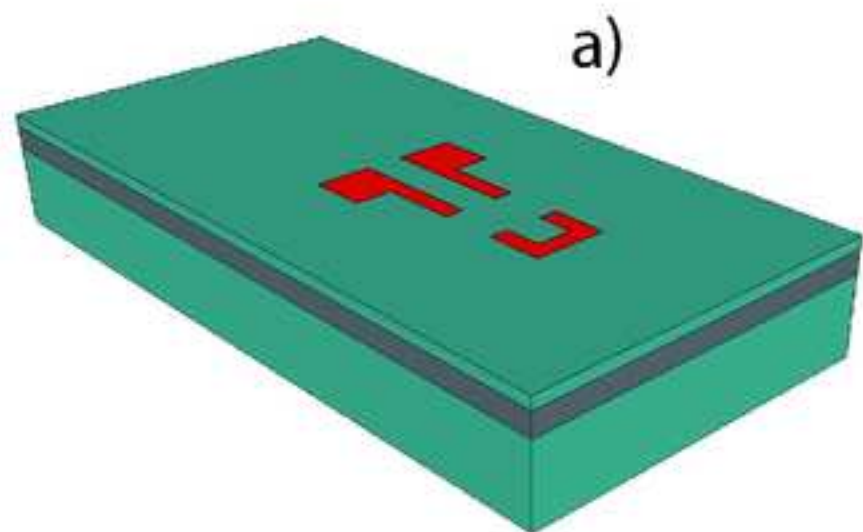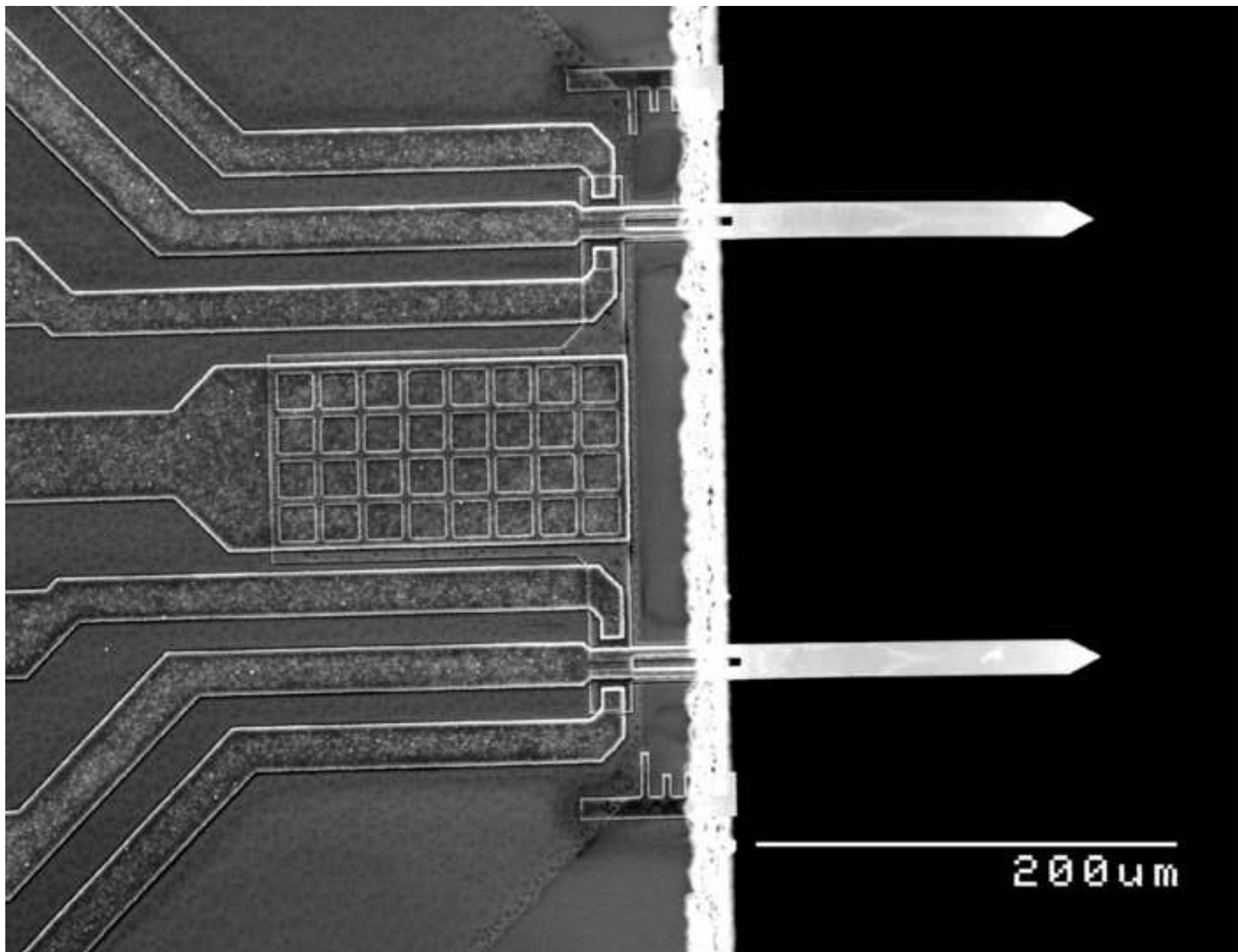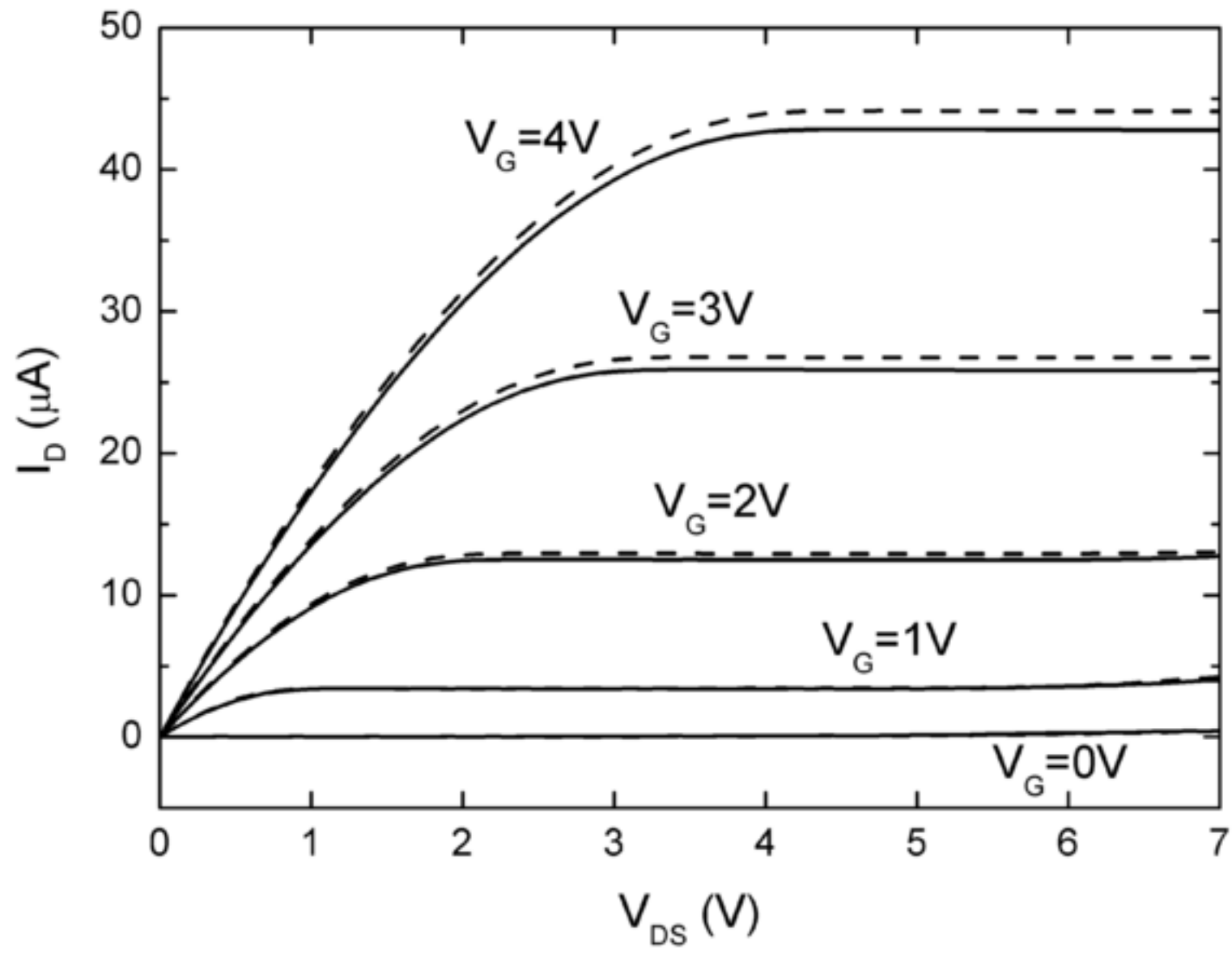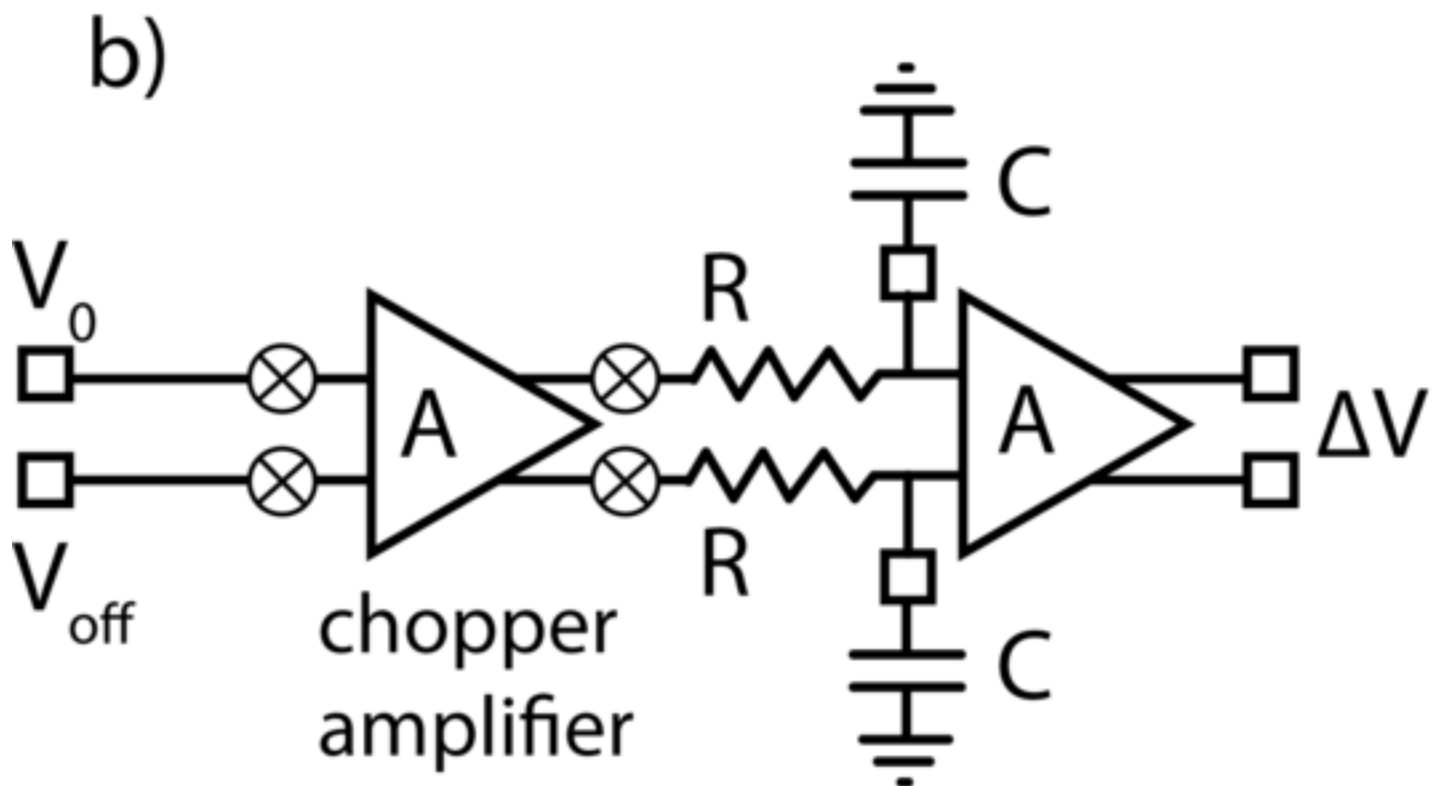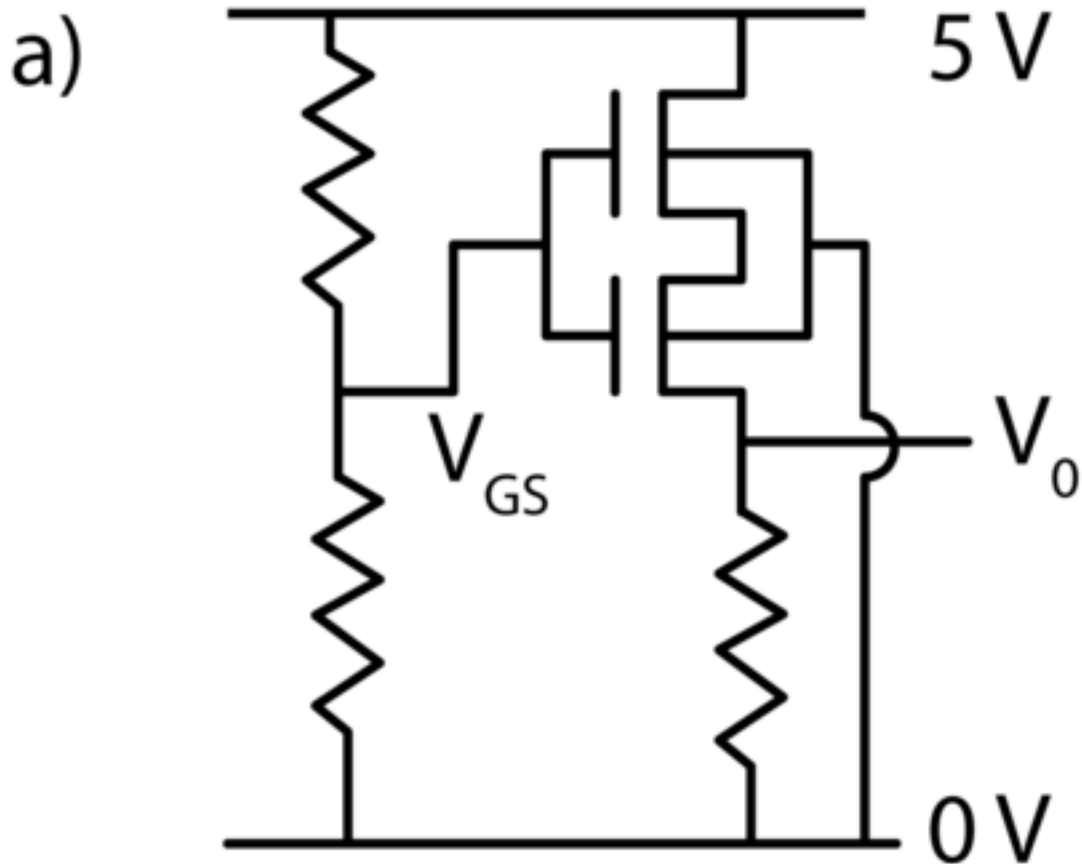
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