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An RF Approach to Modelling Gallium Nitride Power Devices Using Parasitic Extraction

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Abstract: This paper begins with a comprehensive review into the existing GaN device models. Secondly, it identifies the need for a more accurate GaN switching model. A simple practical process based on radio frequency techniques using vector network analyser is introduced in this paper as an original contribution. It was applied to extract the impedances of the GaN device to develop an efficient behavioural model. The switching behaviour of the model was validated using both simulation and real time double pulse test experiments at 500 V, 15 A conditions. The proposed model is much easier for power designers to handle, without the need for knowledge about the physics or geometry of the device. The proposed model for Transphorm GaN HEMT was found to be 95.2% more accurate when compared to the existing LT-spice manufacturer model. This work additionally highlights the need to adopt established RF techniques into power electronics to reduce the learning curve while dealing with these novel high-speed switching devices.

Keywords: gallium nitride; power electronics; power device; parasitics; device modelling; switching model; Vector Network Analyser

1. Introduction

To enable commercialisation of GaN high-speed power switching circuits, there are problems caused by parasitics that need to be overcome. Ultra-fast dv/dt and di/dt cause significant instability issues stemming from the inductive, capacitive, package and PCB parasitic elements [1]. With devices having near ideal characteristics, the effect due to parasitics can have a detrimental impact on their switching performance that can no longer be neglected.

The cause and effect of parasitics on GaN switching performance have been explored in a few different ways in the literature. The effects of parasitics have been studied focusing on resonances and self-sustained oscillations [2–4]. These are more pronounced for GaN circuits due to its complex structures and operation at high frequency and current levels [5]. Thus, it is imperative that power application designers have an idea about how to evaluate the effects of these parasitics when switching at very high speeds. Many techniques are suggested for dealing with this issue:

1. The first method is to make use of different GaN HEMT physics models to experimentally extract the parasitic elements of the device studying their effects [6]. Although there have been detailed

studies regarding this, development of physics and analytical models are very time consuming. There is only one major study available on behavioural model of the GaN cascode which is discussed later on in this paper.

2. The second method is to study the effect of parasitics through experimental switching waveforms. However, this is a highly intuitional and observational method. The validity of the experiments depends on the accuracy of the measurement systems in use, and they mostly fail to predict the reasons behind these observations [7,8].
3. The third method is to use software (e.g., TCAD, Ansoft or Maxwell Q3D) simulations to extract parasitics to model the device. This requires knowledge about the physics and geometry of the devices, which are complex and not always available to the designer. It also does not fully explain the underlying reasons behind the observations [9].

Accurate non-linear or large-signal behavioural models for HEMTs are crucial for proper circuit and systems design and do not exist as of now. The models that exist now are complex, preventing the understanding of the switching behaviour for the power designer. Considering all these facts, this paper first reviews the device and package parasitics of three different commercial GaN HEMTs. Secondly, it introduces RF process to accurately extract the impedances of the circuit. The switching behavioural model is then developed from the extracted parasitic impedances using a Vector Network Analyser (VNA). Numerical simulation in LT-Spice modelling was used to demonstrate the behavioural model. A double pulse test was performed for comparing the simulation results with experimental results to validate the dynamic performance of the developed model. This research paper proposes a new behavioural model of GaN for application engineers without the need for any in depth knowledge about the physics nor geometry of the device.

2. Existing GaN Models: A Review

Although several GaN HEMT devices are reported, very few reliable device switching models have been developed for GaN HEMTs—the proposed models are as listed in Table 1.

1. Behavioural Models: In [10], based on the Efficient Power Conversion Corporation (EPC) device model, a small-signal SPICE model of GaN HEMT is developed. In [11], a behavioural model is constructed with a GaN HEMT in cascode with a Si MOSFET.
2. Semi-Physics based Models: The Statz model is customised to model both static and dynamic characteristics of GaN HEMTs based on EPC devices [12]. In [13], calorimeter measurements are used to develop a loss model for the GaN HEMT.
3. Physics based Models: The 2-DEG charge density is measured to design an analytical model of a GaN HEMT device [14]. Other physics-based models which takes in to account in-depth physics of the device are presented in [15,16].
4. Numerical Models: A Sentaurus TCAD model for a GaN HEMT device is developed in [17].

Table 1. Review of existing GaN models [18].

Authors	Year	Type of Model	Contribution	Simulation Tool
Okamoto [19]	2011	Behavioural	Power-loss estimation for AC-AC converter.	SPICE
Khandelwal [20,21]	2012	Physics	Parameter determination: carrier-velocity saturation, channel length modulation and self-heating	ADS
Yigletu [22]	2013	Physics	Measurement of 2DEG charge density	ADS
Waldron [23]	2013	Semi-Physics	Static and dynamic characteristics	SPICE
Hoffmann [24]	2014	Semi-physics	Electrical and RC thermal model	SPICE
Huang [25]	2014	Behavioural	Capacitance models	Unspecified
Mantooth [26]	2015	-	Review	-

The above models are accurate in terms of explaining the device operation. However, they are complex and not always suitable for study of dynamic/switching performance. The GaN parasitic model developed by Huang investigates the dynamic performance of the device by exploring the switching performance of the GaN cascode. However, it is not generic to the other available GaN device structures.

The literature survey presented in Table 1 proves that switching events are challenging to measure and characterise. Additionally, it is difficult to separately determine circuit-level parasitics. The existing models clearly fail to achieve this. Furthermore, the methods used for modelling are very time intensive and involve many methodologies from analytical analysis to customised measurement circuitry development. This paper identifies two factors that need to be resolved for developing an accurate and simple GaN behavioural model:

1. An approximate model based on the parasitics of GaN devices without the need for delving into the detailed physics of the structure
2. Extracting the parasitics of the device using a simple, practical and accurate methodology

3. Developing a GaN HEMT Behavioural Model

The main objective in this modelling is to establish a predictive account of the switching voltage and current flow through the GaN device as a function of the applied voltages using the double pulse testing experiment.

For device models, the electrical variables and their dependencies needs to be captured with precision. The device engineers consider accuracy and simulation time as crucial factors. A simple device model generally provides fast simulation speed but compromises on the physics-based aspects of device behaviour and simulation accuracy. Thus, for determining the operation of a device, a physics-based analytical model is usually used for simulation, but it is very complex to understand. In addition, it is tediously long and is not practical for circuit design. Thus, the choice of a model is dependent on the practical application for which it is intended. Based on these factors, a basic device modelling procedure can be generalised, as shown in the block diagram of Figure 1.

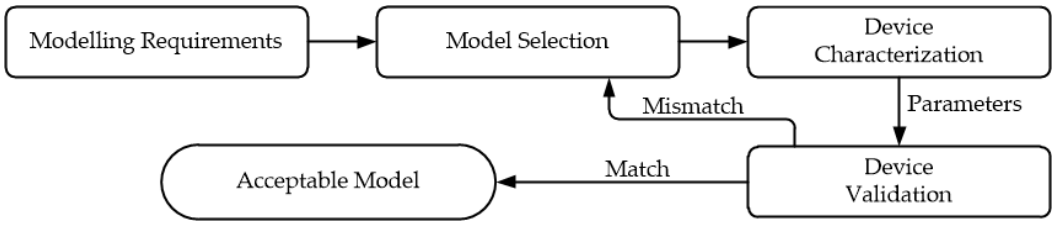


Figure 1. Block diagram for power device modelling.

For power semiconductor device models, the intended use is typically as a power switch in power electronics applications. Usually for power devices, Double-Pulse test (DPT) circuit is used to validate the switching behaviour of the device model. Additionally, it is sometimes used for device characterisation if the dynamic performance is of interest for the investigation. Based on the experimental validation results, the proposed model may be either selected or rejected. If the device model cannot be accepted, a new device model needs to be designed repeating the above process. In this paper, the process designed for GaN HEMT modelling is as elaborated in Figure 2.

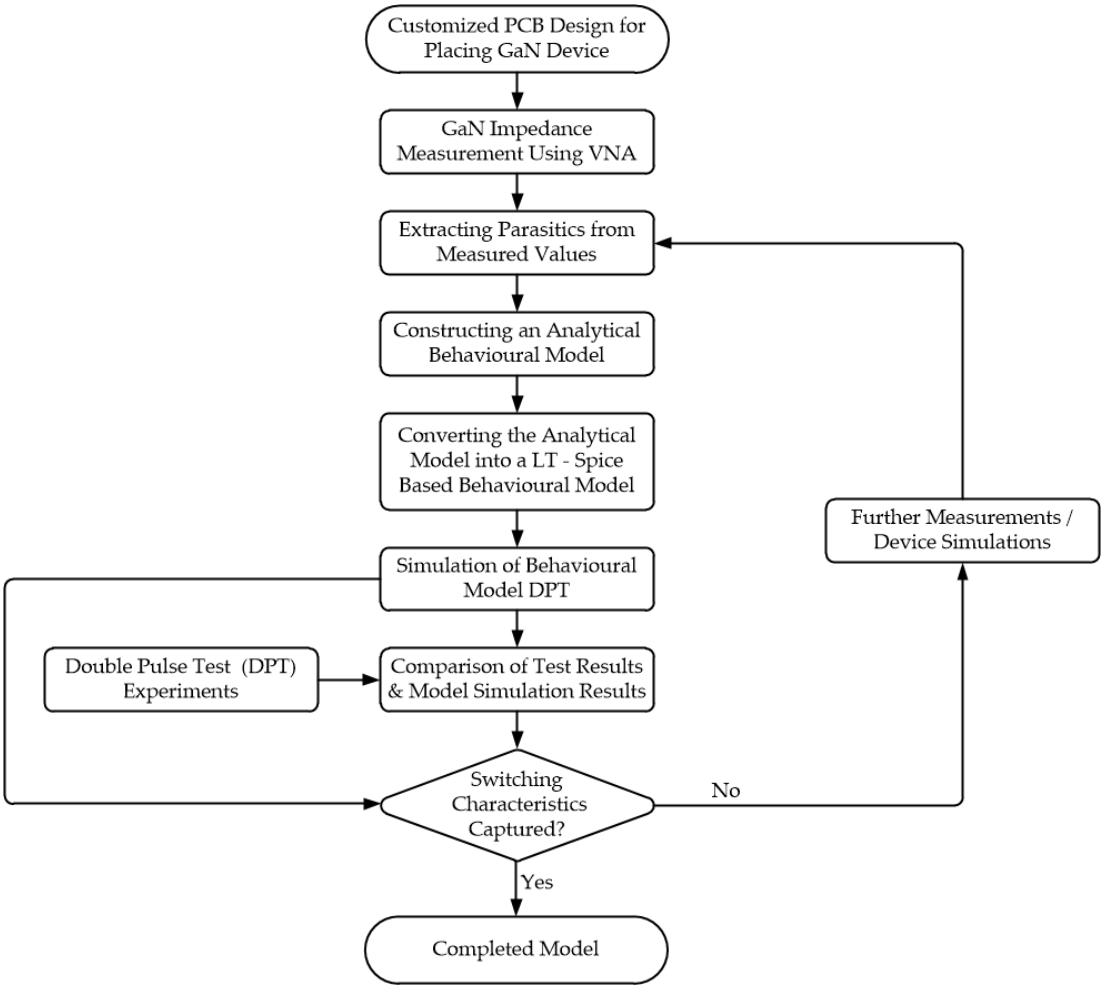


Figure 2. Flow diagram of the GaN device modelling design using VNA measurement and DPT results.

3.1. Overview of Parasitics for a High-Voltage GaN HEMT Device

In power electronics applications, the parasitic impedances of the high-speed switching device play a detrimental role in limiting its maximum achievable performance. Unlike commercial applications based on traditional power devices, these high speed GaN switching devices have their spectral content in the radio frequency region. This can lead to spurious and oscillatory circuit behaviour due to resonances excited in the parasitic elements. To investigate, analyse and mitigate this unstable behaviour, it is important that application engineers have an approximate estimation of these impedance values. Although direct measurement of impedance using LCR can be done, it is limited due to accuracy [27]. Based on the established practical efficacy of the proposed approach for RF devices, VNA measurement is used in this work. It was validated through the demonstration of a modelling study using commercially-available GaN HEMT devices. The measured impedances were validated through switching experiments.

The parasitics of the enhancement mode GaN HEMTs/GITs structure are as shown in Figure 3. As shown in Figure 4, the cascode device has an additional set of parasitic elements due to the low voltage Si device.

The original GaN device structure was of normally ON-type and hence not preferred in power applications due to safety and acceptability considerations. As a solution to this, the power device engineers came up with the cascode structure to convert it into normally OFF-type. As shown in Figure 4, a normally OFF-type low-voltage Si MOSFET (typically 30 V) is connected in cascode to a normally ON-type high-voltage GaN HEMT (600 V+). Additionally, the source of the MOSFET is

connected to the gate of the HEMT. This combinational design produces an effective normally OFF device. In this structure, the gate of the Si MOSFET is used to regulate the ON/OFF state of the GaN HEMT. This operational flexibility makes the GaN HEMT cascode more convenient and adaptable with the generic Si drivers though it compromises the very high switching speed of GaN.

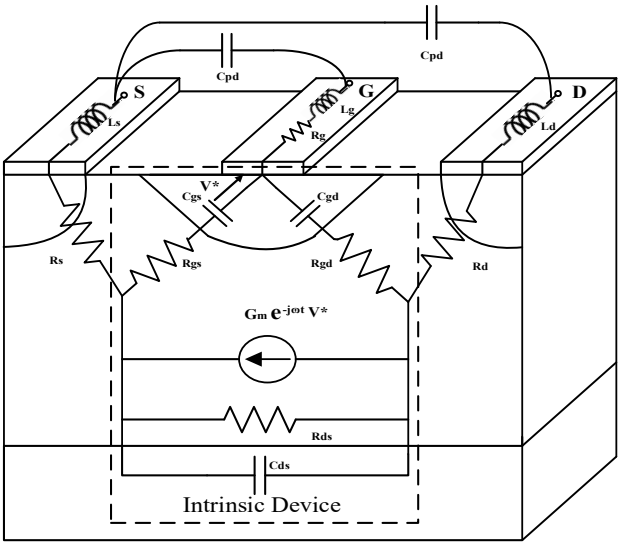
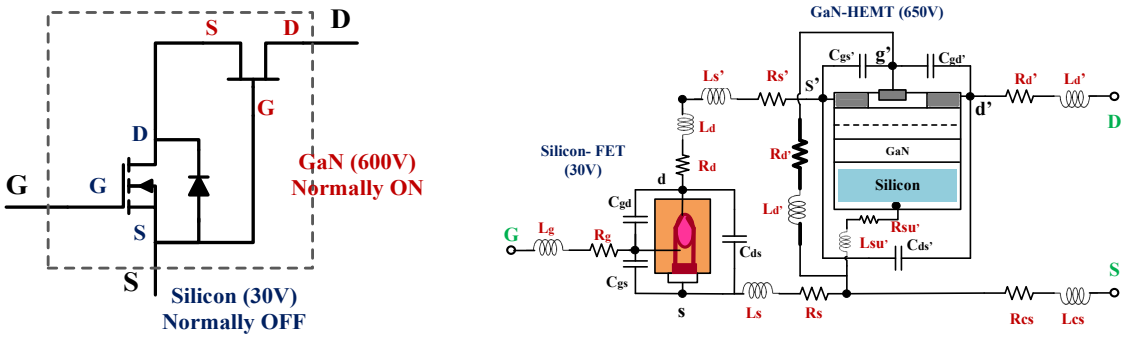


Figure 3. Structure of GaN HEMT with parasitic elements (adapted from [28]).



(**a**) (**b**)

Figure 4. (**a**) Cascode GaN HEMT TO-220 package; and (**b**) simplified bonding diagram (adapted from [29]).

According to Huang Cascode device model, the most critical internal inductances are as shown in Figure 5a. Figure 5b shows the layout of the GaN HEMT cascode inside a conventional TO package. The arrangement of the device shows that parasitic inductances are primarily caused due to the interconnection between the device die, the leads and other interconnections. As the device currents with rapid transitions are restricted to such a compact area, the coupling effects between different conductors become significant and cause deviation from the expected behaviour. In this paper, we use this Cascode model which has been highly regarded by the power electronics community. According to this model, Lint3 is the current source inductance (CSI) for both Si MOSFET and GaN HEMT, as shown in Figure 5a. Thus, it is the most critical parasitic inductance. Lint1 is estimated to be the second most critical inductance. This is because it is the CSI of the high-voltage GaN HEMT which contributes to the majority of switching loss when compared to Si. Ls is found to be the third most critical inductance.

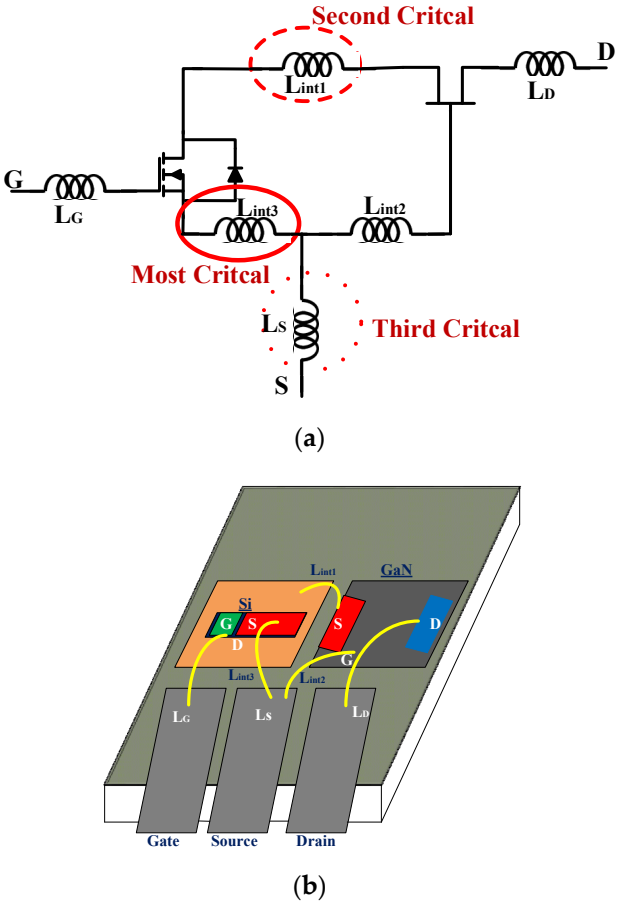


Figure 5. Cascode GaN HEMT: (**a**) package parasitic inductance schematic; and (**b**) TO-220 package simplified bonding diagram (adapted from [30]).

It is observed that available simulation models neglect some of these parasitic inductances, which are critical in understanding the dynamic behaviour of the device.

The development of the model in this work is based on the assumption that for GaN, the device parasitics are based on this arrangement. To validate the proposed work, the developed model is based on a two-port impedance measurement using VNA. The impedance across the G-D, G-S and D-S are measured, the inductance and capacitance values are extracted. These values are also compared with LT-SPICE model values supplied by the manufacturers and with existing papers where a similar procedure is used for SiC modules. The final switching model is thus developed from this extracted data and is simulated in LT-Spice. The simulation results are then compared with available manufacturer device models with experimental waveforms from DPT.

3.2. Behavioural Modelling of High-Voltage GaN HEMT

The proposed modelling design procedure is based on developing a dynamic behavioural model, as shown in Figure 6. This analysis is based on the two-port representation and is estimated via frequency-dependent impedance measurements taken between the source, gate and drain terminals. As discussed above, within the device package, it is the device linkage and package which are dominantly inductive, while the semiconductor die is principally capacitive. This simple model estimates that for any two terminals chosen for analysis, the impedance sweep will output a second-order RLC network. This simplification has been used by many research groups and is proved to produce approximate inductance values with minimum error. Based on the existing models and device parameter extraction, the small signal model of GaN HEMT in Figure 6 can be approximated as shown in Figure 7 [31].

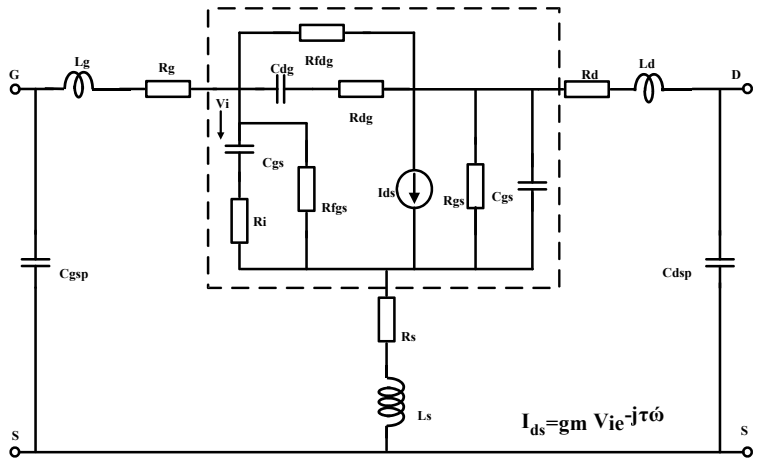


Figure 6. Small signal model of GaN HEMT (adapted from [31]).

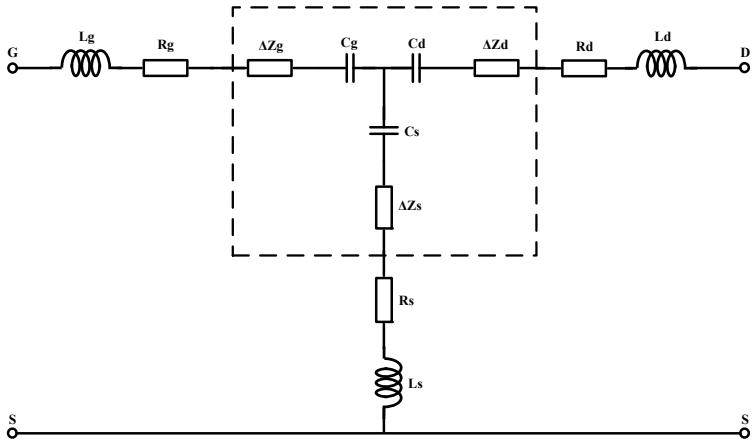


Figure 7. Simplified parasitic circuit model of GaN–reduced zero bias form (adapted from [31]).

The small-signal equivalent circuit model developed does not intend to obtain the specifics of semiconductor die and wire-bond interconnections. Thus, in this work, the measured lumped inductance values are compared to the extracted values of the model proposed by Huang to determine the individual wire-bond inductances of the TO packages. Since SMD package is devoid of such large interconnection inductances, it is assumed to be zero in this work. Measuring the combined impedance for each possible pairing of terminals for the device will produce a set of three combined inductance values. These combined inductance values are related to the individual parasitic inductance values in the equivalent circuit of Figure 6 by linear Equations (1)–(3). The device capacitance is considered intrinsic and shows the reduced zero-bias equivalent.

$$Ld + Rd + Ls + Rs = Lds + Rds \tag{1}$$

$$Ld + Rd + Lg + Rg = Ldg \ + Rdg \tag{2}$$

$$Lg + Rg + Ls + Rs = Lgs + Rgs \tag{3}$$

Figure 7 is simplified for zero bias conditions depending on the device structure to simplify the circuit model to a symmetry form in favour of parameter extraction.

3.2.1. Packaging Impedance Analysis

The analysis procedure used in this work is adopted from the technique employed in [32] for extracting SiC module impedances. This technique is based on the use of a Vector Network Analyser

(VNA) to measure impedances and compute inductances from it. This is done as an extension of the procedures outlined for RF devices in [33].

In this study, the frequency sweep was done using an Agilent E5061B Network Analyzer. This experiment was carried out between 100 Hz and 3 GHz. A critical step for this procedure is the calibration of the VNA, as shown in Figure 8. Proper calibration must be performed every time the set-up is detached from the device mount or when the test rig is disturbed or changed in any way.

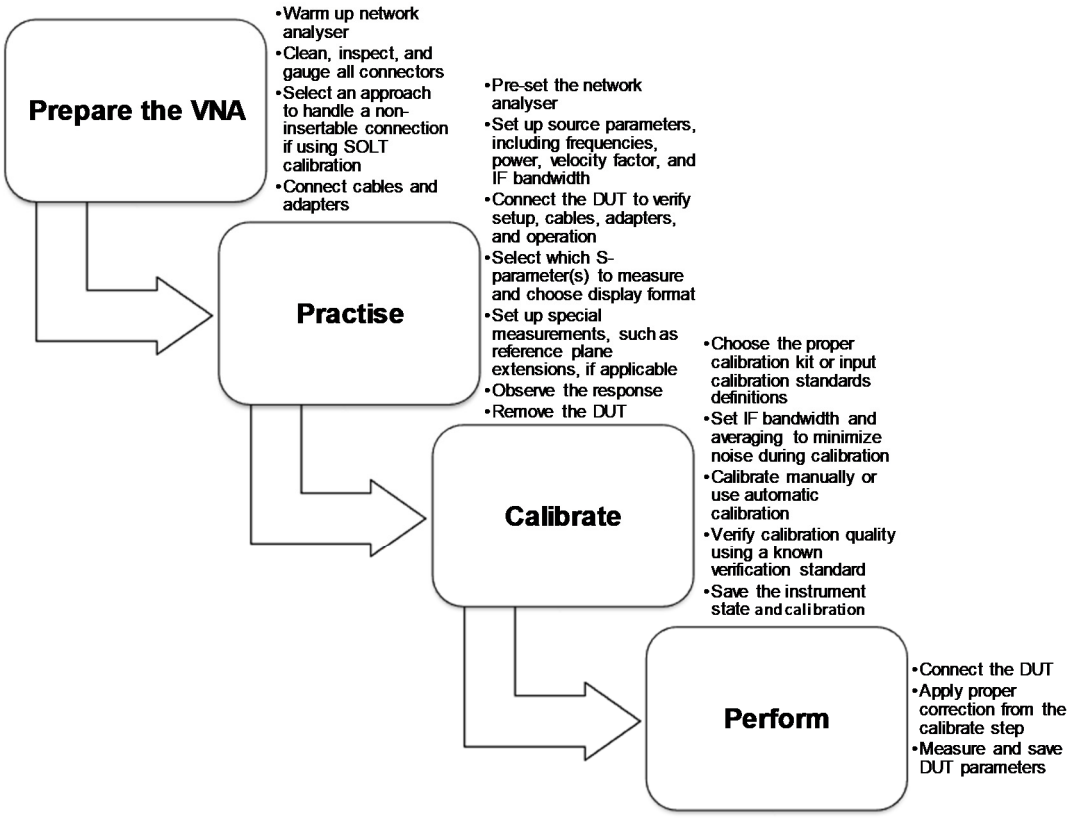
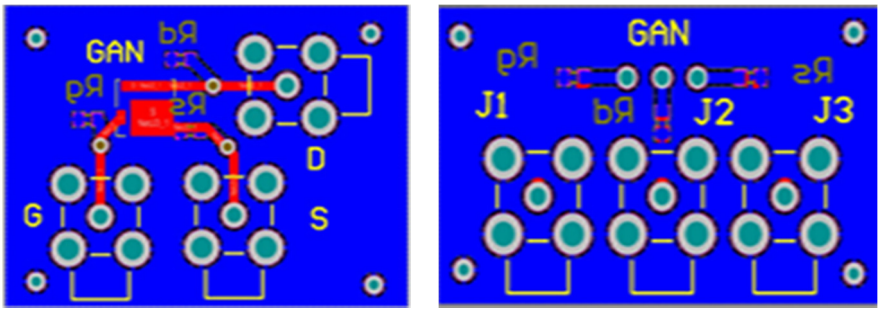


Figure 8. VNA calibration and set-up for impedance extraction.

This work is based on the full two-port calibration procedure described in [34]. The "short", "open" and "load" steps were carried out using the calibration apparatus. Custom adapter PCB was used to implement "through" calibration step via extending the calibration plane. The PCB used for mounting the device is as shown in Figure 9, and the test setup used to apply these characterisation procedures is shown in Figure 10.



(**a**) (**b**)

Figure 9. PCB designed for GaN device fixture for: (**a**) SMD packages; and (**b**) TO.

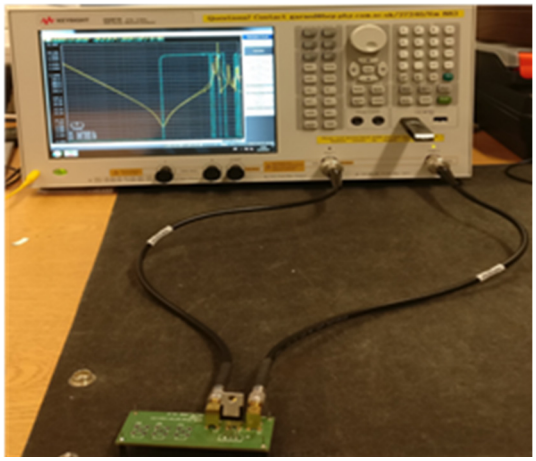


Figure 10. Measurement set-up for GaN device impedance extraction using VNA.

3.2.2. DUT Device under Test

Using the prescribed techniques, it was possible to curve-fit each terminal pair in the module to a series RLC equivalent model. As discussed in the previous sections, the effective capacitance is contributed by the paralleled HEMT and anti-parallel diode intrinsic capacitance, and the effective inductance is the series and parallel combination of the wire bonds and interconnects structures within the module [35,36].

An illustration of the curve-fit agreement achieved by this procedure for Transphorm HEMT is shown in Figure 11. This plot represents the impedances of the GaN HEMT terminal pairs with the gate biased turned OFF. In this plot, the device impedance structure contains additional higher-order terms which are not captured by the simple series LC model and are beyond the scope of this work. However, the primary resonant frequency can be easily determined from the curves, and it is used to formulate an estimate of the equivalent lumped inductance for this terminal pair.

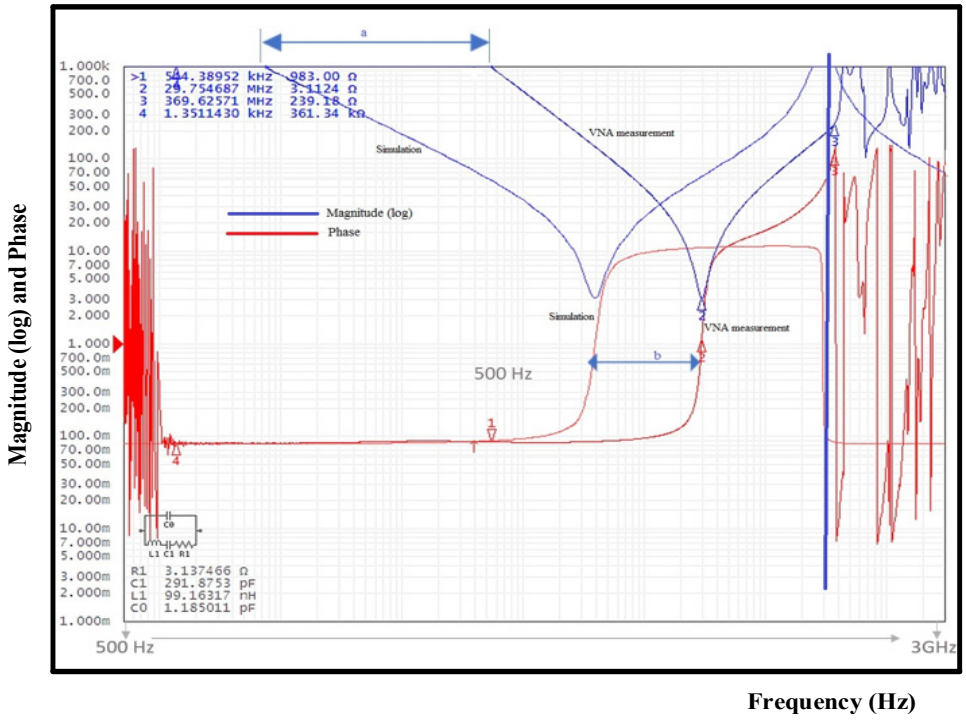


Figure 11. Impedance response for the terminals of Transphorm device.

In Figure 11, the impedance responses are plotted from 500 Hz to 3 GHz. For the devices, until 688 kHz, the impedance is very high, and then, with increase in frequency, the impedance decreases significantly and again increases after 1 kHz. The response is similar to a series RLC circuit for DS and GS terminals as expected. (The light blue colour graph shows the simulated response of the RLC circuit. The dark blue graph with noise is the experimental measured response of the RLC circuit).

In Figure 11, there is a considerable difference (lengths a and b) between the simulation and VNA measurement response. This can be attributed to the fact that the actual device parasitics are not only composed of a series RLC structure. It is due to a parallel combination of other elements such as the capacitor, as shown in the above figures.

In general, it is observed that, until 500 kHz, there is very high impedance and then the circuit behaves inductive with self-resonant frequency at 29 MHz. The impedance response after around 370 MHz becomes dominated by the transmission line behaviour of the co-axial cable and PCB vias, which is highlighted in Figure 11. This is due to the five-point model behaviour of the coaxial cable, the details of which are outside the framework of this research work.

For Transphorm HEMT device, due to the two-device structure, the parasitic inductance is slightly higher than Panasonic GIT. The values are much higher than GaN systems devices because both are TO packaged devices. The PCB terminal inductance is also measured to account for the inductance due to the track inductance and cable inductance. Based on the extracted impedance values in the ON and OFF states, the behavioural model is framed based on extracting the inductance values. Then, finding the capacitance from the resonant frequency of the curve, this is further simulated in LT-Spice and tuned for the values of inductance to verify the accuracy.

The obtained values are plugged into Equations (1)–(3) to extract the aggregate inductance values for all pairings of terminals. The inductances due to PCB are subtracted from the measured values and the final results are presented in Table 2. The individual circuit inductance values are listed in Table 3.

Table 2. Measured lumped inductance of the terminals of the devices.

Combined Inductance (nH)	L_{GD}	L_{DS}	L_{SG}
Transphorm GaN HEMT (VNA)	7.45	4.99	5.04
Panasonic GaN GIT (VNA)	4.465	2.565	3.10
GaNSystems GaN HEMT (VNA)	3.02	1.880	2.76

Table 3. Derived inductance values of gate, drain and source terminals.

Inductance (nH)	L_G	L_D	L_S
Transphorm GaN HEMT (VNA)	3.75	3.7	1.29
Transphorm SPICE model	2.8	2.06	1.04
Panasonic GaN GIT (VNA)	2.815	1.67	0.895
Panasonic SPICE model	2.97	1.55	1.0
GaNSystems GaN HEMT (VNA)	1.04	1	0.67
GaNSystems SPICE model	NA	NA	NA

Based on the extracted impedance values in the ON and OFF states, the behavioural model is framed based on extracting the inductance and capacitance values from the curve. This is further simulated in LT-Spice and tuned for the values of inductances to verify the accuracy. Figure 11 shows that the impedance response obtained for the experimental and simulated responses are in agreement. This simplified behavioural model is then used in simulation to predict the effect of various parasitics on the switching performance.

At low frequencies, reactance is very small and might be masked by capacitive reactance, which makes the extraction challenging. At higher frequencies, there are errors caused due to text fixture and calibration issues. For GaN, extraction is extremely complicated as inductances in the package are very small (≤5 nH). This very small inductance is thus extremely susceptible to systematic errors introduced

by poor calibration. Since the calibration standards used are not true open/shorts, scattering(s) parameters can be applied to de-embed for validating the impedance measurements. However, here, the extracted values are directly compared to the manufacturer model inductance values and found to be very close and reasonable, as shown in Table 3.

4. Switching Tests: Double Pulse Test

To validate the model, the performance of the simulation using the proposed model was compared with the performance of the commercial device using an experimental rig (DPT in this case). The test rig is shown in Figure 12 and was supplied by Sanken Inc as part of our collaborative work with them. This circuit can be customised to use TO and other SMD packages and is thus preferred for convenience and flexibility. The supply voltages for gate drive are customised according to the specification and structure of the GaN device under test.

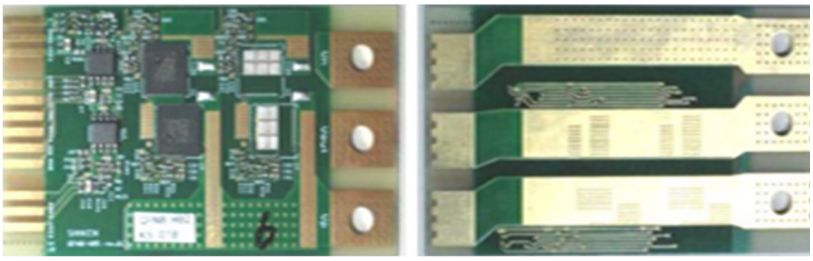


Figure 12. Prototype of the DPT with the inbuilt gate drive circuitry (provided by Sanken Inc).

The test set up is as follows:

1. 500 V dc-bus, 15 A from inductive load
2. Customised measurement set-up
3. Agilent oscilloscope with double pulse signal from Agilent waveform generator
4. Electrical power from bench top power supplies

The device current measurement is done using a current probe. The voltage measurements were checked using a precision probe. The circuit was tested using GaN Systems, Transphorm, Panasonic and Sanken devices. Due to restricted access to the full datasheet and discrete Sanken devices, it is not investigated further in this work. The switching characteristics for the devices tested are detailed in the following sections:

4.1. GaN Systems GS66508B HEMT (650 V, 30 A, SMD Package)

Figure 13 shows the switching characteristics at 200 ns per division. After the initial start, the switching voltage Vds rises sharply with a high dV_{ds}/dt around 10,000 V/s. Afterwards, there is only a small overshoot with no considerable ringing. The current fall measured appears noisy due to interaction of the measurement circuitry with other components on the board. There is a rise in the Vds before turn OFF and is mirrored in the Vgs dropping. At turn ON, the current reaches its on state. All throughout, the gate voltage remains fairly clean with only very small ringing.

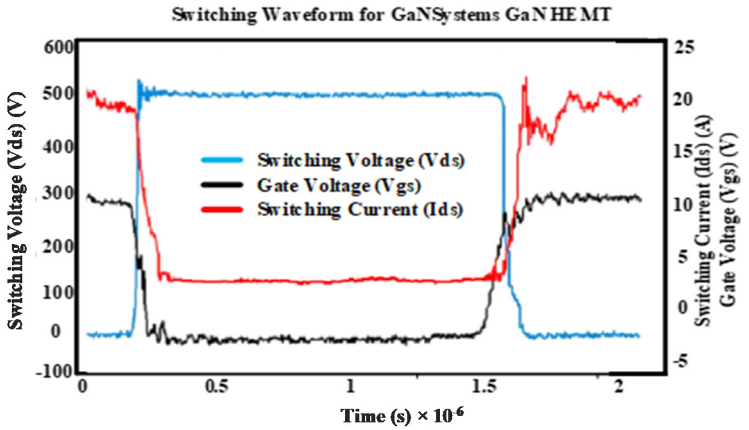


Figure 13. Switching waveforms for GaN Systems GaN HEMT.

4.2. Panasonic GIT PGA26C09DV (600 V, 30 A, TO Package)

In Figure 14, at turn OFF, the dVds/dt is around 35,000 V/s with no overshoot. The current waveform is free of very high frequency ringing and shows a sluggish fall. As the voltage rises and the free wheel diode turns ON, the current falls rapidly. The gate waveform also falls rapidly with no much ringing. At turn ON, the current rises very rapidly with a very small overshoot and the voltage then falls in steps. The voltage and current capture is distorted due to measurement inconsistencies. The voltage falls with an initial fast dV_{ds}/dt followed by a step fall.

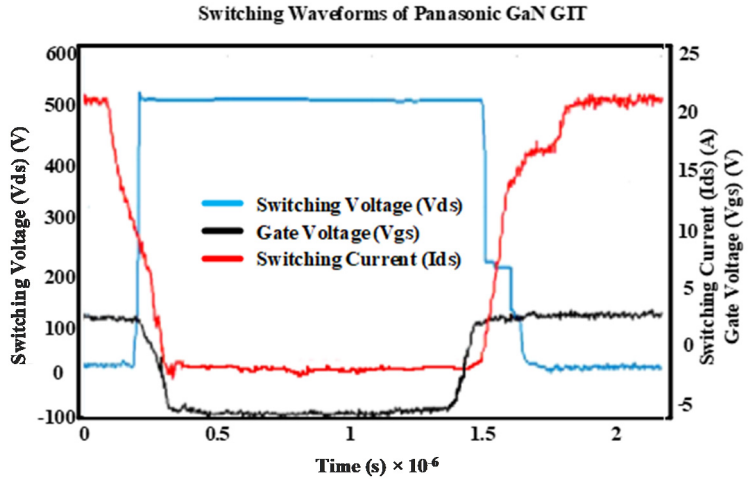


Figure 14. Switching waveforms for Panasonic GaN GIT.

4.3. Transphorm Cascode GaN HEMT TPH3212PS (600 V, 30 A TO Package)

Transphorm is a cascode device, hence can be driven the same as a Si FET. However, since this driver is made with the stringent gate voltage control, for using Transphorm, the gate voltage was increased to +8 V. This caused some unexpected variation of gate voltage. In Figure 15, at turn OFF, the dVds/dt is around 42,000 V/s, with a second-order response with overshoot and oscillations. The current fall is rapid initially followed by a slow fall. The gate voltage has a very clear dip at turn OFF before the voltage rise. This final stage is accompanied by a slow rise in the gate voltage. The gate voltage continues to build up with a steep rise until the device is fully ON.

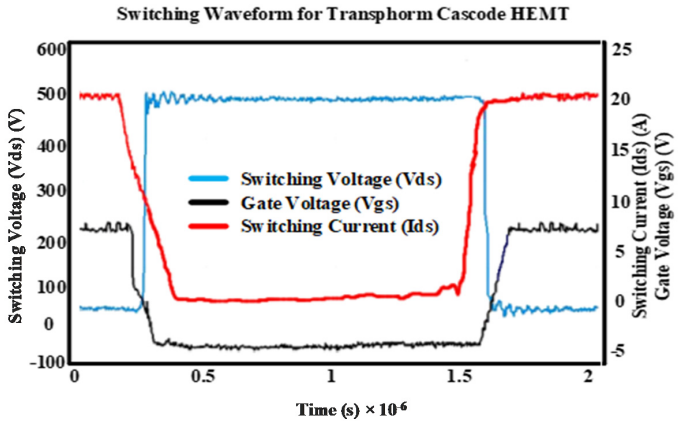


Figure 15. Switching waveforms for the Transphorm GaN HEMT cascode.

5. Simulation of the Double Pulse Tests Using the Proposed Model and Manufacturer Model

For this research, the proposed behavioural model was demonstrated and validated by redesigning the LT-Spice model provided by the manufacturer. The parameters of the existing model were customised to bring the model into alignment with the extracted measurements. Figure 16a,b is a replication of the simplified zero bias model of Figure 7. The manufacturer and proposed models are both simulated in LT-Spice for comparison, as shown in Figure 16.

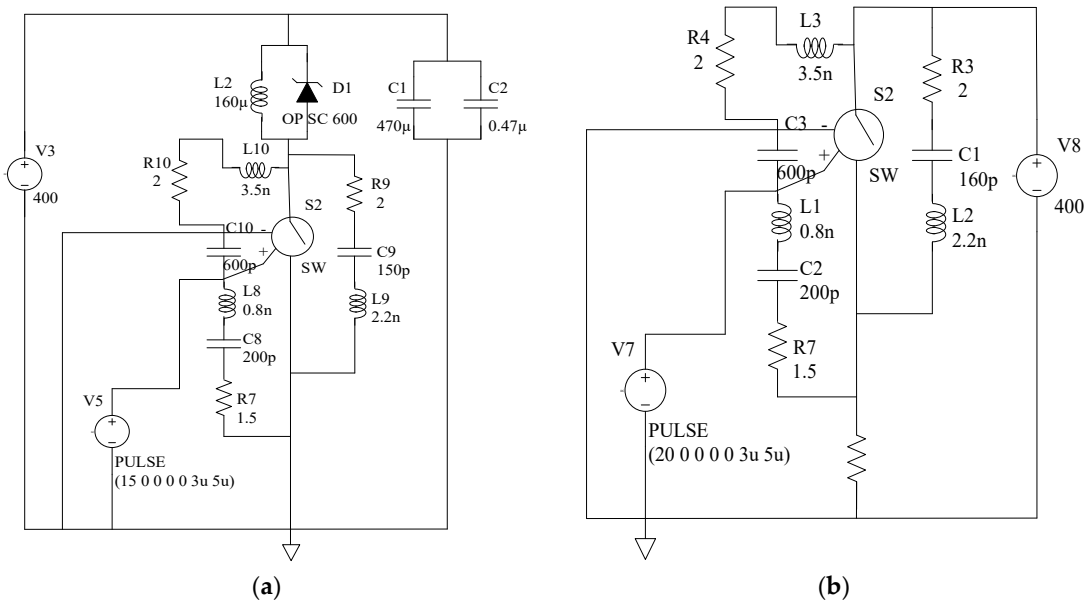


Figure 16. (**a**) Proposed behavioural model for GaN HEMT; and (**b**) DPT simulation of the proposed model.

6. Comparison of Lt-Spice Simulation with DPT Output

First, we integrated the parasitic model with the existing manufacturer models of the device. Then, an overlay of the simulation output from the manufacturer model, developed behavioural model and experimental waveforms were compared for switching trajectories at 15 A and 500 V. The resulting switching voltage, gate voltage and current comparisons are presented in the subsequent sections.

In Figure 17, Figure 18, Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, reasonable agreement is noted between the simulated and experimental waveforms. The most significant switching characteristics of the waveforms are reproduced in accordance with the experimental waveforms. Specifically, the voltage switching transition rates appear to be in good conformity. These results suggest that the

critical parasitic impedances are reasonably well-matched. The simulation current, on the other hand, is not always well matched to experimental waveforms. As shown in the figures, the measurement of current was not accurate due to noise interference. This makes the simulated current waveforms of the proposed model and manufacturer model slightly different from the experimental values. Based on the waveform simulation time, repeatability comparison and by measuring the distance between the voltage waveforms for devices, accuracy of the proposed model is determined. It is based on the similarity of the proposed model switching waveforms to the expected experimental waveforms. The difference in the distance is calculated and accuracy determined.

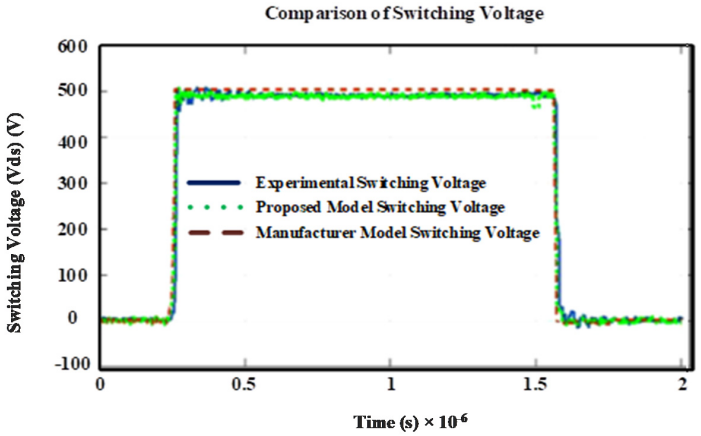


Figure 17. Comparison of switching voltage waveforms of models with DPT results.

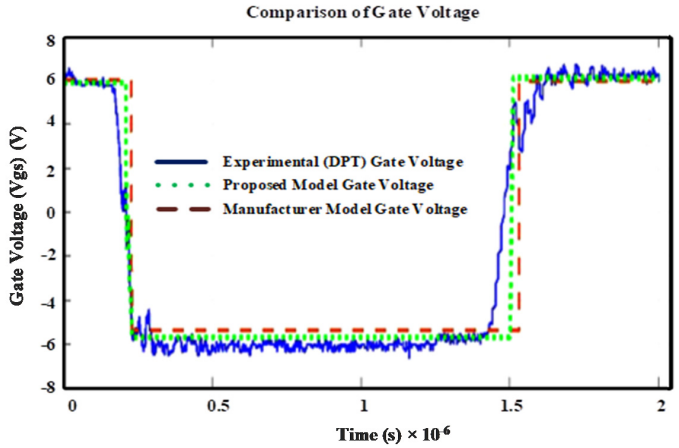


Figure 18. Comparison of gate voltage waveforms of models with DPT results.

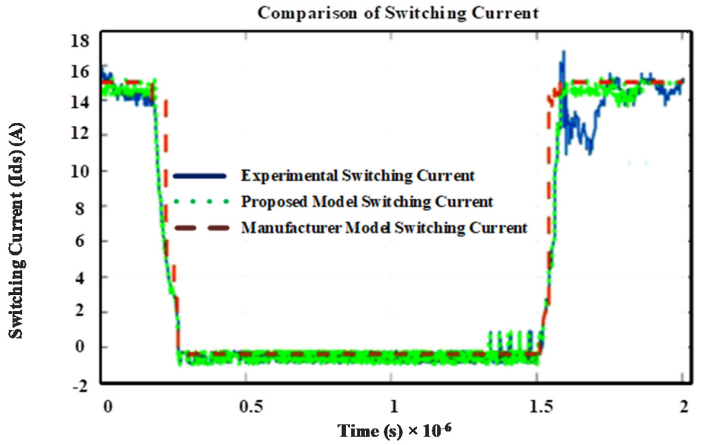


Figure 19. Comparison of switching current waveforms of models with DPT results.

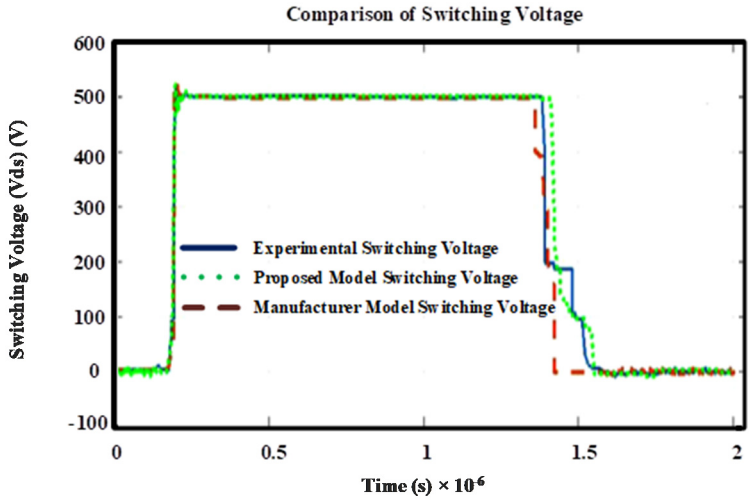


Figure 20. Comparison of switching voltage waveforms of models with DPT results.

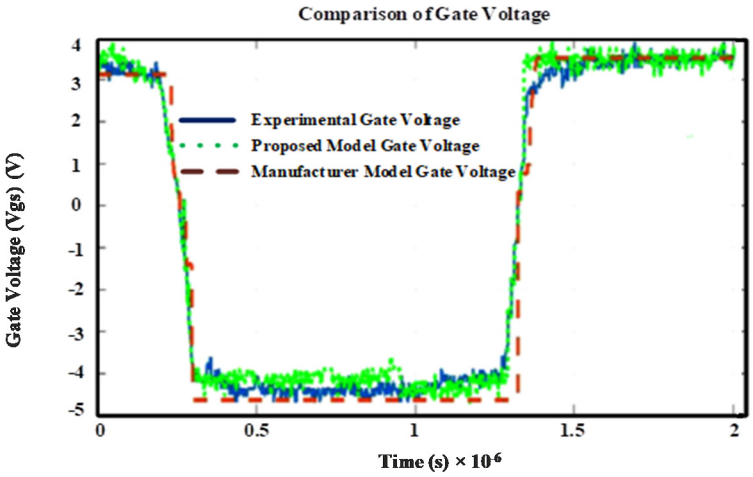


Figure 21. Comparison of gate voltage waveforms of models with DPT results.

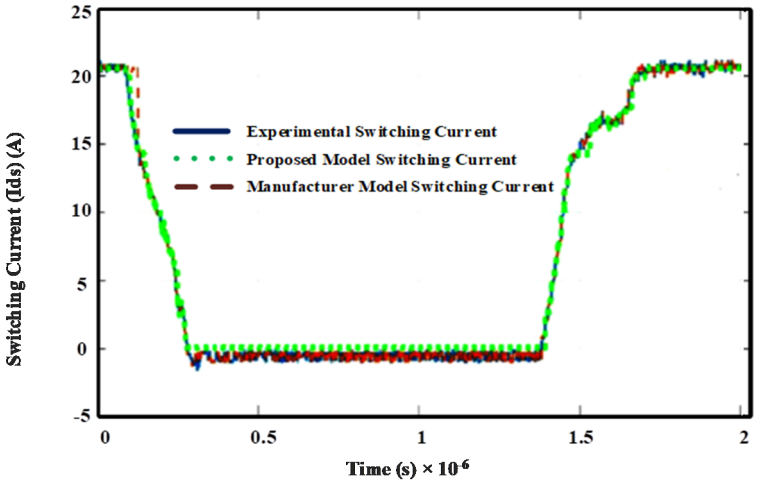


Figure 22. Comparison of switching current waveforms of models with DPT results.

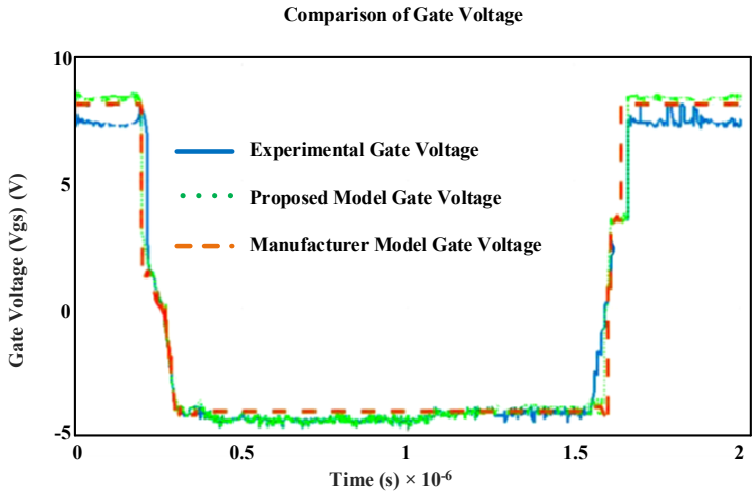


Figure 23. Comparison of gate voltage waveforms of models with DPT results.

6.1. GaN Systems GaN HEMT

For the GaN systems device, the switching voltages of the proposed model are in good agreement with the experimental results, as seen in Figure 17. This is specifically true for the transient and oscillations during turn OFF instants. In addition, towards turn OFF, it follows the experimental voltage waveform very closely.

The gate voltage in Figure 18 is relatively clean which is possibly because measurement of gate voltage was not accurate. The manufacturer and proposed model showed more ideal characteristics. The switching current measurement suffered from noise can be seen in Figure 19. However, the overall proximity of the proposed model to the experimental waveforms shows that the behavioural model is nearly accurate.

6.2. Panasonic GaN GIT

For the Panasonic device, the switching voltages of the experimental model were in steps during turn ON due to the influence of the switching current deviation and noise. As shown in Figure 20, the proposed model was in good agreement with the experimental results, especially during turn OFF and turn ON instants. In addition, towards turn OFF, it follows the experimental voltage waveform very closely.

The gate voltage shown in Figure 21 is noisier for this device due to customisation of the gate circuitry. Using external elements in the PCB has caused it to oscillate due to the parasitic inductances of the connections and the external board.

The switching current shown in Figure 22 is in close agreement and there was no significant deviation from the experimental results. Furthermore, the behaviour of the proposed model is similar to the experimental waveforms; however, during turn ON and turn OFF instants it is deviating from ideal.

6.3. Transphorm Cascode GaN HEMT

As shown in Figure 23, the gate voltage was very noisy for this device due to customisation of the gate circuitry using external elements added to the PCB which has caused it to significantly oscillate due to the parasitic inductances of the connections and the external board introduced to increase the positive input voltage to +8 V as the gate circuitry was designed in the range of 4.5–5 V.

7. Discussion

1. The measurement using VNA is relatively straightforward and does not require an accurate understanding of the packaging or structure of the device.

2. It is noted that the measured package parasitics are as expected higher than the supplied manufacturer model values specified in the LT-spice models.
3. The demonstrated model is simple, approximate and satisfactorily mimics the actual switching behaviour of the device. It can be seen from the results that the dynamic response of the modelled GaN devices are very similar to the experimental ones.
4. The fluctuation and abnormality in current is caused by the noise associated with the measurement circuitry due to interference with the surrounding circuitry. This ringing is considered to be a measurement error due to the rapid changes in voltage and current during switching. This could not be replicated in the simulation properly and so there is a mismatch in the measured and simulated device switching currents. The Transphorm gate voltage variation is noisy due to the customised gate drive circuitry inductance.
5. From this work, it is concluded that a simple behavioural model for different GaN devices can be built using extracted parasitics from the VNA measurements. The proposed behavioural model shows very close characteristics to the actual working of the GaN device when employed in a power circuit. The observed variation of the proposed model from the actual device is due to the practical inability to precisely measure impedances and simulate parasitics. Nevertheless, this model is a best approximation for a simple GaN behavioural model.
6. This proposed behavioural model is dependent on the measurement circuitry, PCB inductance, calibration errors of the VNA and human errors. To further improve accuracy and capture the response of the GaN power device more accurately, we explored the use of ML techniques to build realistic GaN models. These models can mimic the switching performance of the GaN power devices with great accuracy and fidelity.

8. Conclusions, Limitations and Future Work

Behavioural modelling, parasitic quantification and operation at higher switching frequencies were identified as the major barriers to commercial adoption of GaN at application level. To solve this issue, a simple behavioural model of GaN HEMT is developed by extracting impedances using a Vector Network Analyser. This is a practical approach to GaN power device modelling using techniques borrowed from RF space.

A comparison of the switching performance of the developed model, the manufacturer model and experimental findings show that the proposed model is simple, practical and fast. However, because of the time involved in parasitic extraction, the complexity of the analytical procedures and the dependency on human and measurement errors, the proposed behavioural model is not suitable to validate all applications. Hence, this cannot serve as a universal model for GaN. Thus, the need for a unified GaN behavioural model which is an accurate replica of the actual device dynamics was identified. An ML-based universal GaN model was developed as future work to solve the limitations of this proposed model [37]. Nevertheless, the proposed GaN model based on RF techniques can serve as the best candidate for a practical simulation design and can be used in conjunction with the existing LT-spice models.

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