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Subject review

THD Analysis of a Seven, Nine, and Eleven Level Cascaded H-Bridge Multilevel Inverter for Different Loads

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Abstract: A multilevel inverter is implemented for generating the required staircase AC voltage of output from various steps of voltages of DC sources. The multilevel inverter gives a better harmonic spectrum and a compatible quality of output. This article delves into an analytical analysis of the total harmonic distortion (THD) of different multilevel inverters which employ a multicarrier PWM technique. This technique is implemented for operating the switches at their respective angle of conduction. This paper deals with various cascaded H-Bridge multilevel inverters (CMI) with various loads that are modelled by implementing the MATLAB/Simulink platform. The output gives a better result of the proposed model in terms that it is helpful towards reducing the THD and the losses of switching.

Keywords: APOD; CMI; IPD; phase shifted modulation technique; POD; THD

1 INTRODUCTION

The multilevel inverter can be categorized as a power semiconductor device along various sources of dc voltage. Those sources may be a solar cell, fuel cell or a battery. Higher voltage and lower switching losses can be achieved by properly, i.e. with proper sequence, turning on and off the devices. There are various advantages of the multilevel inverter in comparison with the two-level inverter. It can operate over a wider range of switching frequencies. It draws the output current of a lower THD and generates the output voltage of a lower harmonic content. Additionally, it has a much lower common mode voltage. The PWM technique can be successfully applicable. It also has certain demerits that by increasing various switching devices, also increase the requirements of gate drive circuits. Such system configurations become complex and by default, there is an increase in the cost of devices.

The common recognized topologies of the multilevel inverter are known as the cascaded H-bridge and neutral point clamped inverters, among which the cascaded H-bridge inverter is popularly used for single-phase systems [1]. The PWM-based technique can give a better dynamic response in addition to the lower THD of current, and the staircase modulation (SCM) based operation can also be directed (when required) over PWM due to having a lower burden of commutation, which can result in reduced switching losses [2-5]. The method of selected harmonic elimination (SHE), based upon the concept of the elimination of harmonics, proposed by Patel for inverters of a high-power range, offers enhanced operations at the lower range of the switching frequency by decreasing the size and price of the bulky types of passive filters [6-8]. These have been effectively implemented in various topologies of the cascaded H-bridge multilevel types converters, whose N-level output of ac voltage improves the performance of the reduced THD [8-17].

The commonly implemented switching methods for a 3-phase voltage source inverter (VSI) are the space vector pulse width modulation (SVPWM) techniques and the carrier pulse width modulation (CPWM) [18-20] and the five-phase VSI [18, 20-25]. The survey verifies that CPWM reigns over SVPWM at an increased number of phases because of its speed and the structure of the modular computing type [18, 26]. However, SVPWM has greater dominance compared to the CPWM and sinusoidal PWM(SPWM) [18] due to its operational evidence such as fault-tolerant capabilities, common-mode voltage (CMV) and switching losses [27-29]. The different modulation topologies are normally computed by taking into account its computational capability, with THD being most commonly used for a specified inverter application [30]. Another general basis would be the particular harmonic amplitude limitation set up by exhortation and excellence such as RMS CMV [31, 32], IEEE Std. 519 [33], the harmonic distortion factor (HDF) [34], and peak common-mode voltage (CMV) [35].

The NPC inverter initially implemented the PWM techniques such as a simple uniform PWM [36, 37] and the selective harmonic elimination PWM (SHEPWM) [38]. Eventually, significant research was worked out based upon the SHEPWM topology [37, 39, 40]. Voltage signal pulses have a consistent amplitude over a cycle of lines for a uniform nature of PWM [37]. In the sinusoidal PWM, the width of the pulses of voltage are sinusoidally modulated based on the trend of the fundamental pattern for achieving proper spectral properties [41-46].

The development of non-conventional energy resources at higher power and voltage levels demands a sustained upgrade in power electronics converters [47-50]. The multilevel inverter has been successfully implemented at higher power and voltage levels for a single/three-phase system utility in the last decade [51, 52]. The multilevel inverter topology generates more levels of voltage in a way that it decreases the voltage stress and THD while increasing the semiconductor devices [53]. During operation at the higher ranges of switching frequencies, these additional switching devices can raise the losses of power [54-56]. The switching frequency of SHEPWM can be regulated by a proper selection of the pulses of signals in preset voltage waveforms [57-60].

In the analysis, a different study is conferred with having a 15-level inverter by implementing an asynchronous machine drive having single-phase system such that it is in the construction stage of the inverter, 16 numbers of power switches (e.g. IGBTs) are implemented [61]. Hence, in this case, a linear pulse width modulation (LPWM) may be preferred for these types of 15-level inverters [61]. The 35-level inverter can also be implemented for achieving the power line's ac voltage from the solar power plant's dc voltage [62].

There are three principal classifications of multi-level inverters [63]. These are known as the cascaded H-bridge [64] multilevel inverter, diode clamped and capacitor clamped [65] type. A comparison analysis of various multilevel inverters of the cascaded H-bridge such as the 3-level, 5-level, 7-level, 9-level and 11-level inverter is carried out in this paper. The multicarrier pulse width modulation (PWM) technique is [65] implemented in this H-bridge. Through this type of the phase shifted-PWM analogy, among two carrier waves, the Φ_1 phase displacement is achieved. It is represented as

$$\Phi_1 = \frac{360°}{m-1} \tag{1}$$

Where, m = the inverter level. In the case of the level shifted-PWM, there will be a vertical displacement of the carrier signals of triangular waves. Here, carrier waves have identical frequency. These types of PWM are principally categorized into three types. These can be represented as: a phase disposition pulse width modulation technique (IPD-PWM), a phase opposition disposition pulse width modulation technique (POD-PWM) and an alternate phase opposition disposition pulse width modulation technique (APOD-PWM).

2 TOPOLOGY OF THE MULTILEVEL INVERTER

2.1 Operational Principle

The (CMI) [66] generally consists of a certain number of inverters of full bridge types whose AC terminals are set in a series manner for synthesizing the desired output signal.

Fig. 1 represents the general diagram of the CMI, where each bridge is supplied by an individual dc voltage source. As per from Fig. 1, for an inverter of the m-level, the inverter of a full bridge has [(m−1)/2] number which is joined in pattern of series, and also, the same value of the separate sources of the DC voltage is used. In this topology, 2(m−1) switching devices are used. CMI consists of less switching devices as compared to other multilevel inverter topologies.

2.1 Modulation Methodology of CMI

In this paper, the PWM method is used to produce the desired gate pulse for the switching devices. This method requires a fewer number of components and helps reduce the harmonics of a lower order. The harmonics of a higher order will be minimized by implementing filter circuits. Basically, in the sinusoidal PWM technique, there are two signals, and one is the reference signal (sinusoidal signal) which is compared with a frequency of the higher range of the carrier signal (triangular signal), which generates the ON and OFF state. The magnitude of the voltage of output can be regulated by adjusting the modulation index (M_I). In the case of the inverter of the m-level, the triangular waves of (m−1) numbers are compared with a sinusoidal wave.

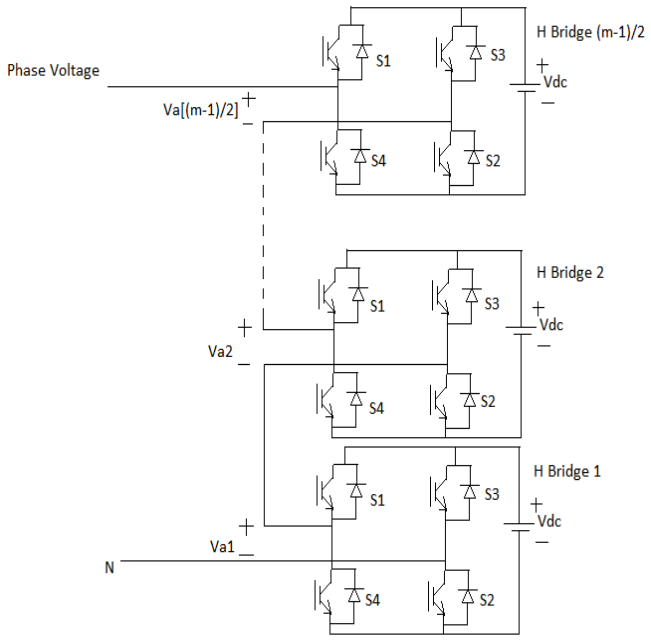

Figure 1 Basic structure of a CMI

3 METHODOLOGY

The operation of different multilevel inverters with different loads is done in the MATLAB Simulink. Among different multilevel inverters, the nine level inverter topology and its switching states are explained in Fig. 2 and Tab. 1 respectively. Fig. 2 represents 9-level multilevel inverters which have four individual bridges and are connected in a series, and four dc voltage sources are given to the individual bridge so that each bridge can be operated by single dc voltage. In this case, each dc voltage value is the same, i.e. 100 V.

In a similar manner, other multilevel inverter topologies and switching states can be verified.

In the case of the multilevel inverter, each level indicates a particular voltage level in a cycle. The multilevel inverter of a cascaded H-bridge type produces almost sinusoidal waveforms by increasing the level of voltages, and it can be implemented in HVDC systems, high power drives, SVC, renewable energy systems, traction drive systems, etc. It can be also used in variable speed drive induction motors that have a medium voltage range of an induction motor.

In the 9-level multilevel inverter, there is series connection of four numbers of full bridges that have a single phase [67]. The 9-level inverter has a voltage of output of nine values. These are: zero, V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$ [68], which is why it is called a 9-level

inverter. To get the output DC voltage V_{dc}, the semiconductor switches a, d, g, h, k, l, o, p should be turned ON. In this switching pattern, for getting a desired step voltage, there should be eight semiconductor switches turned ON. Similarly, other voltage of output can also be computed by using the pattern of switching shown in Tab. 1.

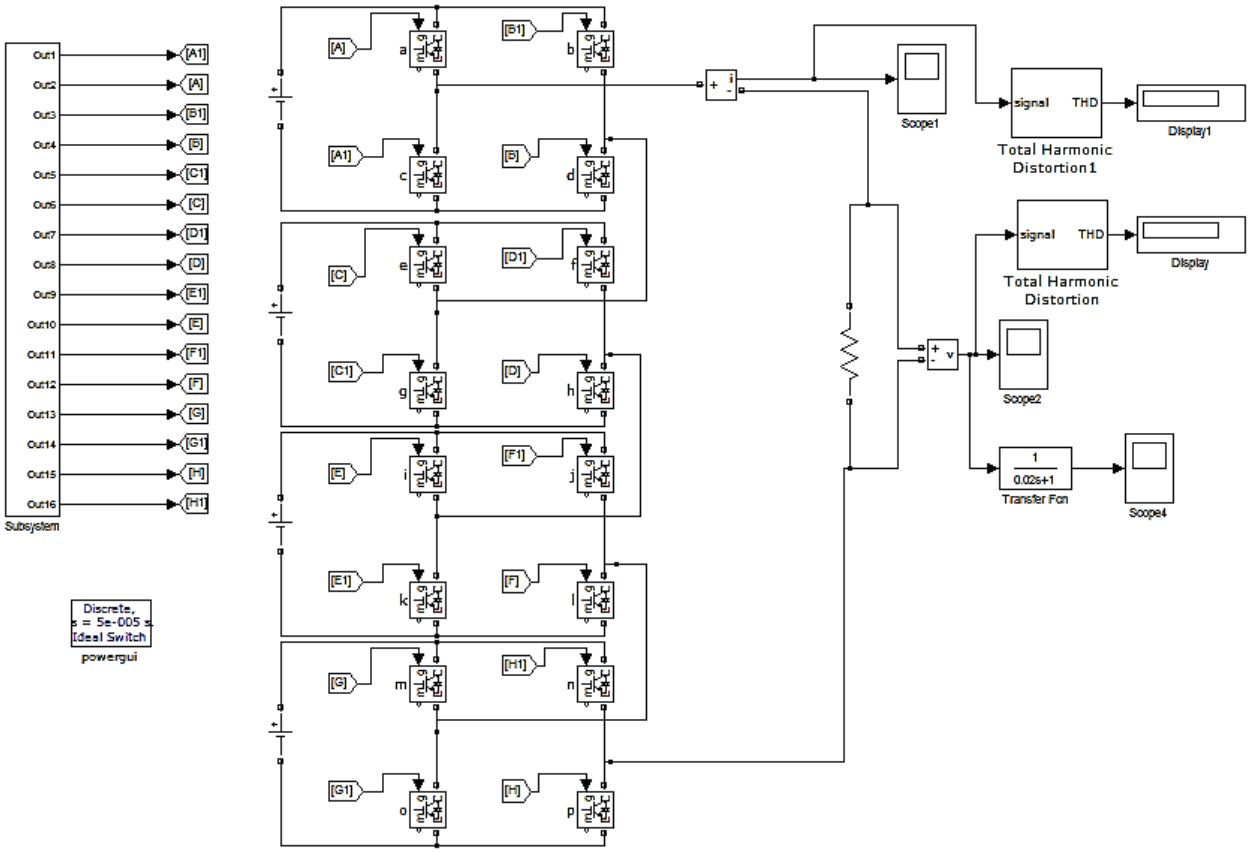

Figure 2 MATLAB model of a 9-level inverter

Table 1 The 9-level inverter switching states [72]

DC Voltage	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
V_{dc}	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
$2V_{dc}$	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
$3V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1
$4V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
$3V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1
$2V_{dc}$	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
V_{dc}	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$-V_{dc}$	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
$-2V_{dc}$	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0
$-3V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0
$-4V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
$-3V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0
$-2V_{dc}$	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0
$-V_{dc}$	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4 SIMULATION RESULTS

The simulations of different multilevel inverters, as discussed above, are computed through the MATLAB Simulation and the desired performances are verified. The THD is analysed for different multilevel inverters with different loads.

4.1 Phase – Shifted PWM Technique

In this method, the triangular waves will be phase displaced by a certain phase angle Φ_1 between the adjacent triangular waves. The phase angle Φ_1 can be calculated as per Eq. (1).

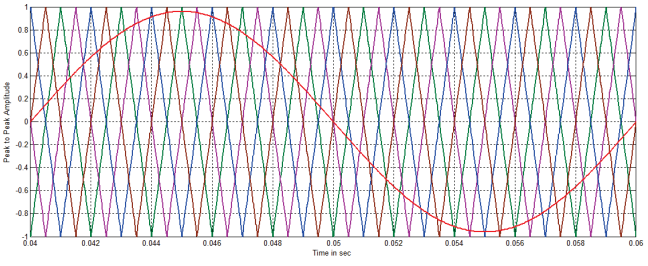

Figure 3 Simulation of a PWM topology

Fig. 3 represents the PWM method of a 5-level inverter, where the signal of a sinusoidal wave is compared with four high frequency triangular signals. It gives an idea of pulse generation for a 5-level inverter. It is produced by juxtaposing the sinusoidal signal with four high frequency carrier triangular signals. In a similar way, the gate pulse can be generated by juxtaposing a number of triangular waves with a sinusoidal reference wave for other multilevel

inverters. The harmonic spectrum present at the output voltage can be analysed through the FFT analysis. Fig. 4 represents the 3-level inverter's output voltage, and by carrying out the FFT analysis, the THD value is 56.13%. Fig. 5 shows a 5-level CMI whose THD value is 30.31%. Figure 6 shows a 7-level phase shift multilevel inverter whose THD value is 20.22%. Similarly, Figs. 7 shows a 9-level phase shift multilevel inverter, and by doing the FFT analysis, its THD value is 15.3%. As previously stated in the preceding figures, Fig. 8 shows an 11-level inverter that uses the phase shift modulation technique and generates the THD value of 13.21%.

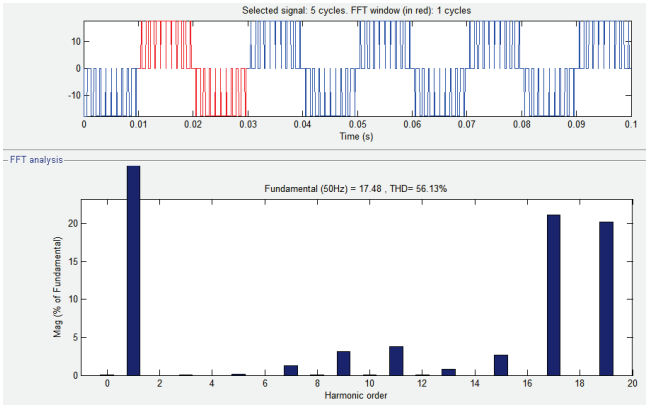

Figure 4 Output voltage's FFT analysis of a 3-level inverter [70, 71]

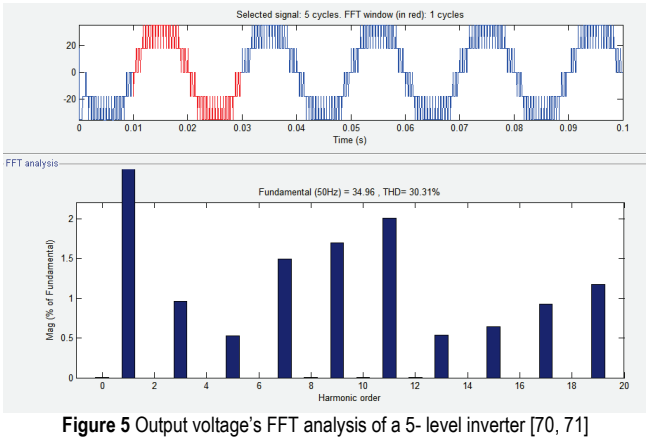

Figure 5 Output voltage's FFT analysis of a 5- level inverter [70, 71]

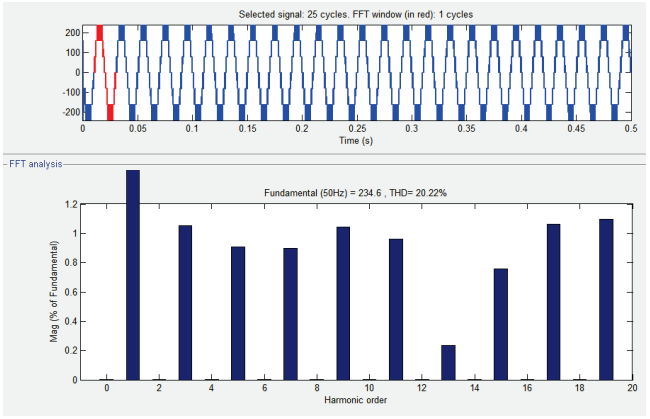

Figure 6 Output voltage's FFT analysis of a 7-level inverter [70, 71]

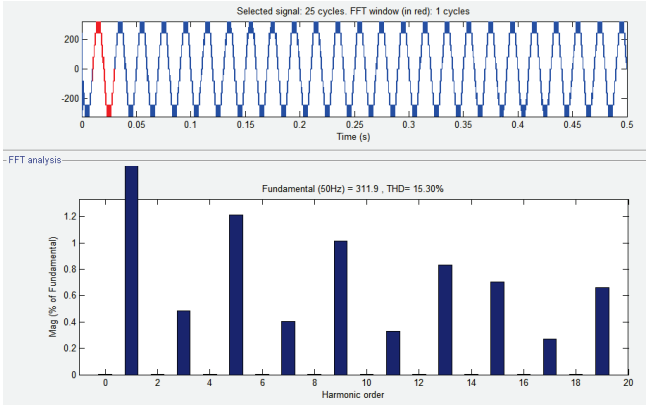

Figure 7 Output voltage's FFT analysis of a 9-level inverter [70, 71]

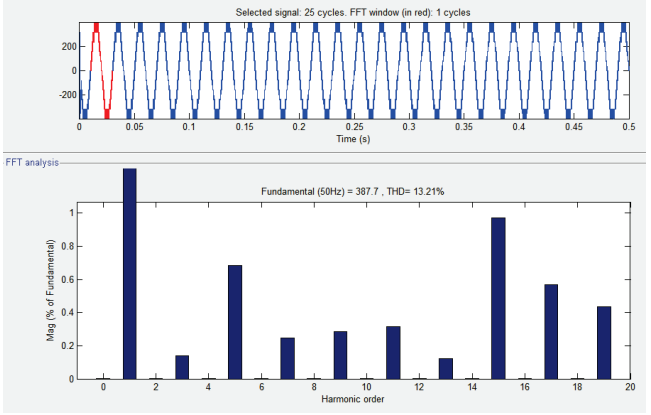

Figure 8 Output voltage's FFT analysis of an 11-level inverter [71]

4.2 Level–Shifted PWM Technique

In this case, there is a vertical shift of the triangular waves, and their peak to peak amplitude – including the frequency – is the same. There are mainly three types of strategies and they can be represented as: 1) in phase disposition (IPD) [72], 2) phase opposition disposition (POD) [72] and 3) alternate phase opposition disposition (APOD) [72] PWM technique.

4.2.1 IPD-PWM Technique

Carrier waves are here in [73] the same phase.

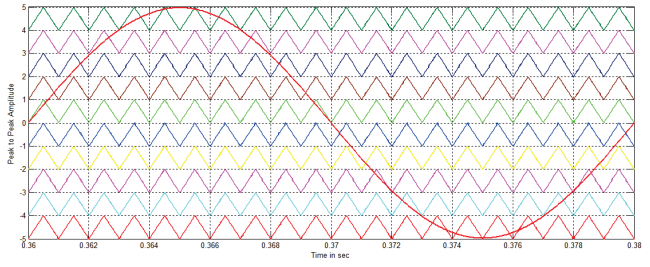

Figure 9 Gate pulse generation of an 11-level inverter [77]

Fig. 9 represents the gate pulse generated by comparing ten triangular waves with one sinusoidal wave, where each triangular wave has some magnitude for an in phase

disposition (IPD) PWM techniques of an 11-level multi-level inverter.

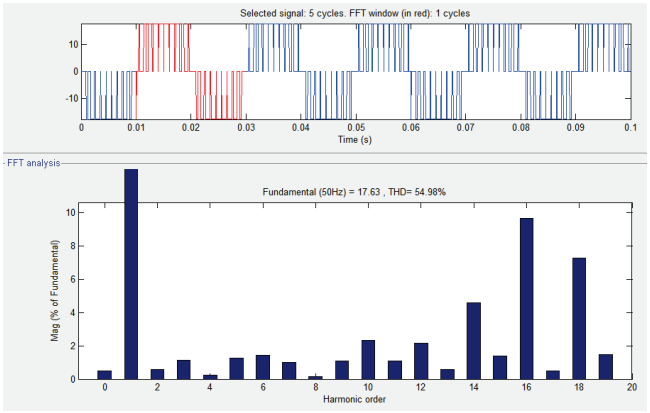

Figure 10 Output voltage's FFT analysis of a 3-level inverter [70, 71]

In a similar manner, the firing pulse can be generated for other multilevel inverter topologies. The harmonic quantity present in the output voltage can be evaluated through the FFT analysis. Fig. 10 represents the THD value of a 3-level inverter by doing the FFT analysis. The THD value is 54.98%. Fig. 11 represents the THD value of a 5-level inverter by using the IPD-PWM technique. The THD value is 28.75% by doing the FFT analysis.

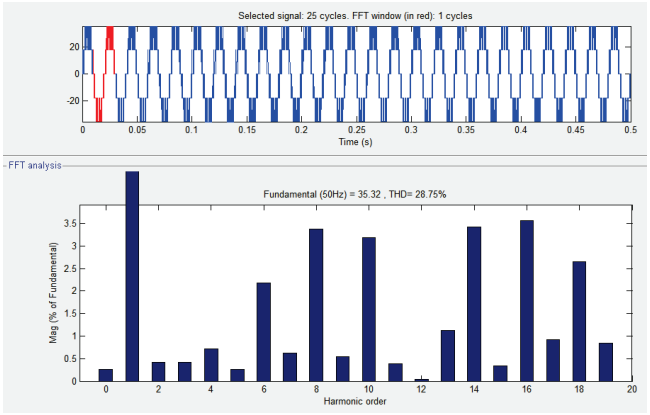

Figure 11 Output voltage's FFT analysis of a 5-level inverter [70, 71]

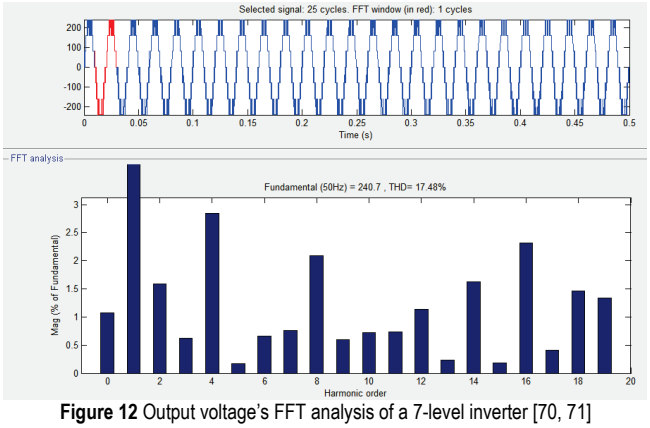

Figure 12 Output voltage's FFT analysis of a 7-level inverter [70, 71]

Fig. 12 represents the THD value of a 7-level inverter, which is 17.48% by doing the FFT analysis. Fig. 13 represents the THD value of a 9-level inverter, which is 14.4% by using the IPD technique. Fig. 14 represents the THD value of an 11-level inverter by implementing the IPD-PWM technique. Therefore, by doing the FFT analysis, the THD value is 11.11%.

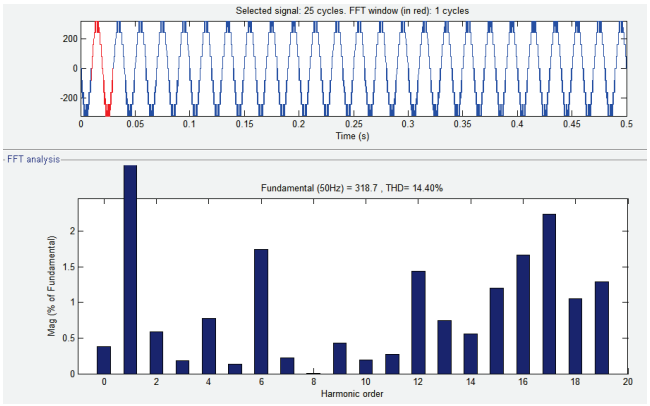

Figure 13 Output voltage's FFT analysis of a 9-level inverter [70, 71]

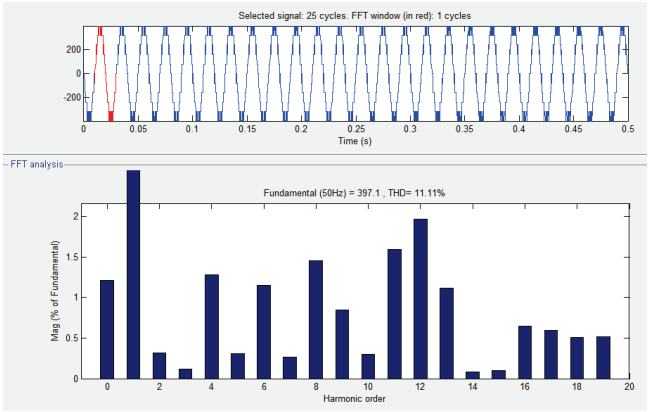

Figure 14 Output voltage's FFT analysis of an 11-level inverter [70, 71]

4.2.2 POD-PWM Technique

Here, all carrier [74] waves are in the same phase on the top and bottom sides of the zero reference and of the 180° phase displacement.

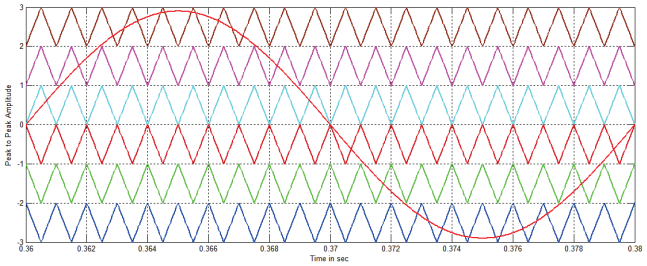

Figure 15 Gate pulse generation of a 7-level inverter [77]

Fig. 15 represents the gate pulse generation of a 7-level inverter by using the POD technique, where the firing angle is generated by comparing six high frequency triangular signals with a fundamental sinusoidal signal. In a similar way, the gate pulse can be generated for other inverters. The presences of harmonics in the output voltage are calculated

through the FFT analysis. Fig. 16 represents the THD of the output voltage of a 3-level inverter as 56.03% by doing the FFT analysis.

Similarly, Fig. 17 represents the THD value of a 5-level inverter, which is 30.63%. Fig. 18 represents the distortion value of the output voltage of a 7-level inverter, which is calculated as 18.12% through the FFT analysis. Fig. 19 represents the THD value of a 9-level inverter, which is 17.62%. Fig. 20 represents the output voltage's THD value of an 11-level inverter by using the POD-PWM technique and the THD value obtained by the FFT analysis is 11.40%.

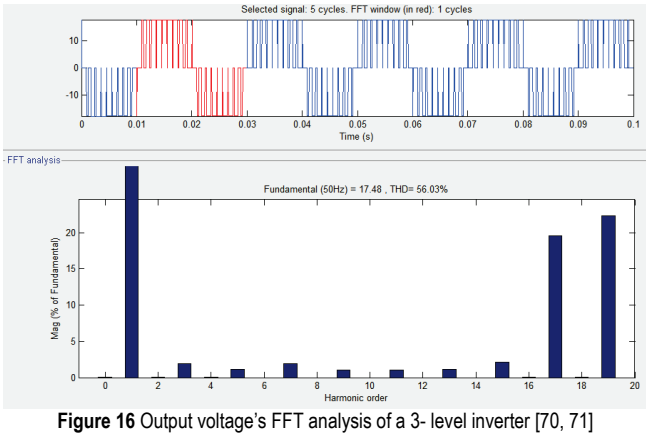

Figure 16 Output voltage's FFT analysis of a 3- level inverter [70, 71]

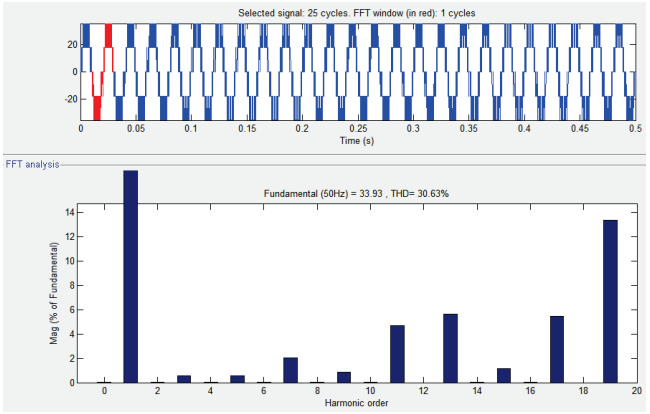

Figure 17 Output voltage's FFT analysis of a 5-level inverter [70, 71]

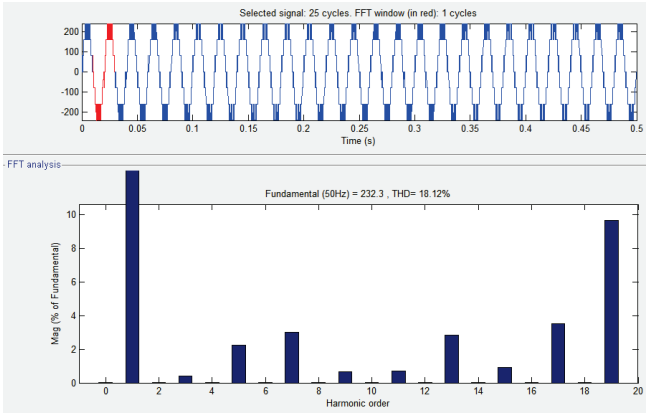

Figure 18 Output voltage's FFT analysis of a 7- level inverter [70, 71]

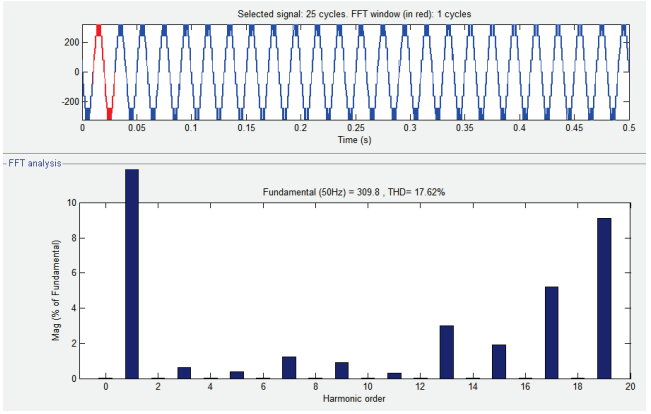

Figure 19 Output voltage's FFT analysis of a 9-level inverter [70, 71]

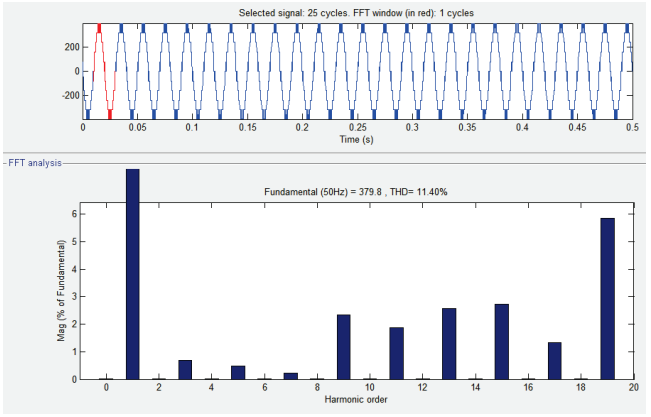

Figure 20 Output voltage's FFT analysis of an 11-level inverter [71]

4.2.3 APOD-PWM technique

Here, carrier waves are phase displaced by 180° alternately.

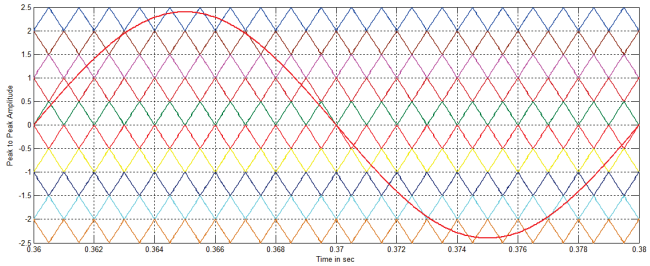

Figure 21 Gate pulse generation of an 11-level inverter [77]

Fig. 21 shows the firing angle generated by using the APOD technique of an 11-level inverter, where ten numbers of signals of high frequency are juxtaposed with a reference signal of the sinusoidal wave to get the desired gate pulse. Fig. 22 shows the THD value of a 3-level inverter, where the THD value is 58.33% by doing the FFT analysis. Fig. 23 represents the THD value of the output voltage of a 5-level inverter, which is 31.42% by using the APOD-PWM technique. Fig. 24 represents the distortion value of a 7-level inverter's output voltage, which is 19.77% by doing FFT analysis. Fig. 25 represents the percentage of the THD value of the output voltage of a 9-level inverter, which is 16.43%. Fig. 26 shows the THD value of the output voltage of an 11-

level inverter by using the APOD-PWM technique, which is calculated as 12.29% through the FFT analysis.

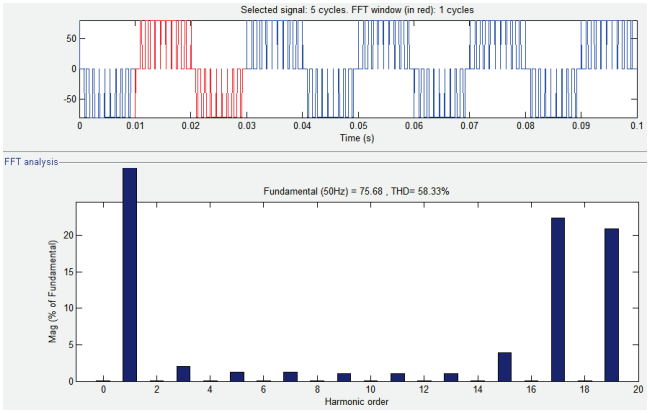

Figure 22 Output voltage's FFT analysis of a 3- level inverter [70, 71]

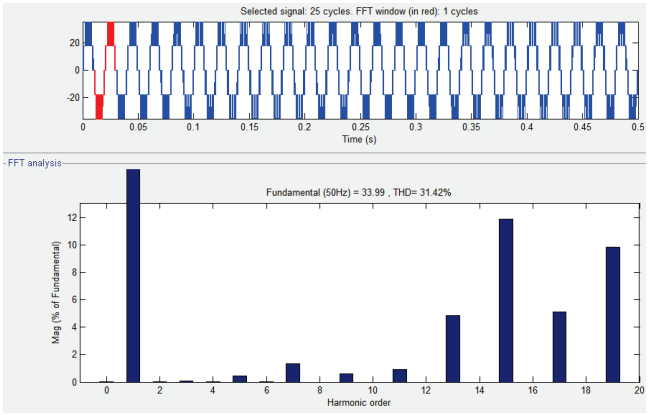

Figure 23 Output voltage's FFT analysis of a 5-level inverter [70, 71]

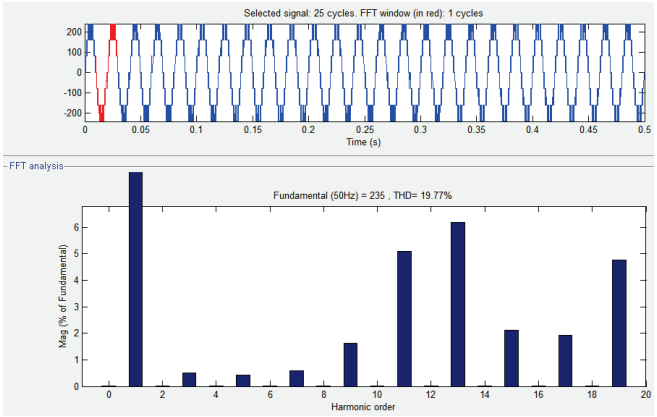

Figure 24 Output voltage's FFT analysis of a 7-level inverter [70, 71]

In the case of both the R-load and the R-L load, the harmonic quantity is the same at the output phase voltage. However, the THD value for current is different for both the R-load and the R-L load. In the case of the R-load, voltage and current are in same phase [76], which is why the THD value is same for both the phase voltage and output current.

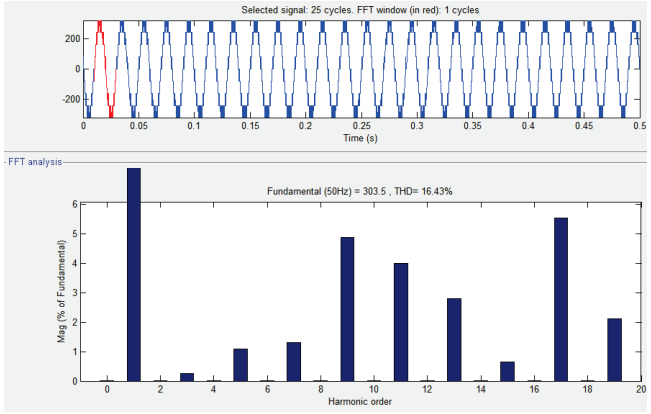

Figure 25 Output voltage's FFT analysis of a 9-level inverter [70, 71]

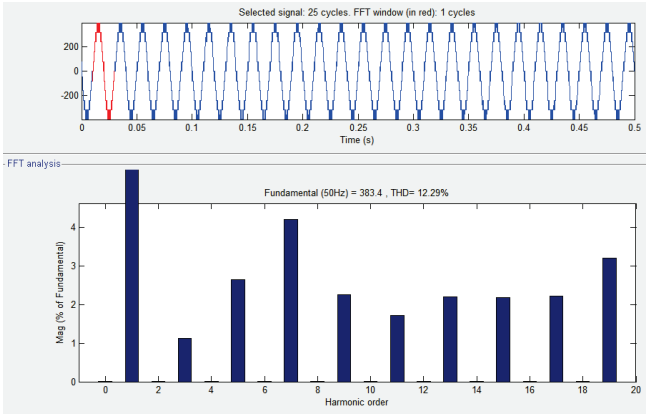

Figure 26 Output voltage's FFT analysis of an 11-level inverter [75]

Table 2 THD analysis of different multilevel inverters with an [75] R- load and without a filter [77]

Phase Voltage	IPD	POD	APOD	Phase shifted (PS)
3 Level	54.98%	56.03%	58.34%	56.13%
5 Level	28.75%	30.63%	31.42%	30.31%
7 Level	17.48%	18.12%	19.77%	20.22%
9 Level	14.4%	17.62%	16.43%	15.3%
11 Level	11.11%	11.41%	12.3%	13.21%

Table 3 THD analysis of different multilevel inverters with an R- load and with a filter circuit [77]

Phase Voltage	IPD	POD	APOD	Phase Shifted (PS)
3 Level	2.28%	2.36%	2.51%	2.34%
5 Level	1.35%	1.36%	1.38%	0.78%
7 Level	1.32%	1%	0.97%	0.53%
9 Level	0.76%	0.83%	0.95%	0.37%
11 Level	0.67%	0.65%	1%	0.23%

Table 4 THD analysis of different multilevel inverters with an R-L load and without a filter [77]

Output Current	IPD	POD	APOD	Phase Shifted (PS)
3 Level	2.68%	2.83%	3%	2.73%
5 Level	1.64%	1.63%	1.67%	1%
7 Level	1.59%	1.23%	1.21%	0.76%
9 Level	1%	1.06%	1.19%	0.62%
11 Level	0.9%	0.87%	1.27%	0.52%

5 CONCLUSION

This paper focuses on seven, nine, and eleven-level multilevel inverters, in addition to three and five-level multilevel inverters with different loads. By analysing the THD value for different multilevel inverters, it has been concluded that by increasing the level number, the %THD value decreases. Harmonics can further be decreased by using the appropriate filter circuit. It is observed that among all simulated multilevel inverters discussed in this paper, the cascaded 11-level multilevel inverter with the IPD modulation technique gives a better THD result at the output phase voltage. The computation of the generation of a signal in the IPD modulation is simpler than other discussed modulations. The harmonics present in the output current in the case of the R-L load can also minimized by increasing the number of levels. It can also be further decreased by implementing a compatible filter circuit. The multilevel inverter reduces the THD value to large extents, hence why the filter size is also reduced. The multilevel inverter can be implemented where the quality of the output is the primary need.

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