ATLAS TileCal Read-Out Driver System Production and Initial Performance Results

J. Poveda, J. Abdallah, V. Castillo, C. Cuenca, *Member, IEEE*, A. Ferrer, E. Fullana, V. González, *Member, IEEE*, E. Higón, A. Ruiz-Martínez, B. Salvachúa, E. Sanchis, *Member, IEEE*, C. Solans, J. Torres, A. Valero, and J. A. Valls

Abstract—The ATLAS Hadronic Tile Calorimeter detector (TileCal) is an iron-scintillating tiles sampling calorimeter designed to operate at the Large Hadron Collider accelerator at CERN. The central element of the back-end system of the TileCal detector is a 9U VME Read-Out Driver (ROD) board. The operation of the TileCal calorimeter requires a total of 32 ROD boards. This paper summarizes the tests performed during the ROD production and the results obtained. Data processing is performed in the ROD by digital signal processors, whose operation is based on the use of online algorithms such as the optimal filtering algorithm for the signal amplitude, pedestal and time reconstruction and the online Muon tagging algorithm which identifies low transverse momentum muons. The initial performance of both algorithms run during commissioning is also presented in this paper.

Index Terms—Data acquisition, data processing, electronic equipment testing, field programmable gate arrays, integrated circuit.
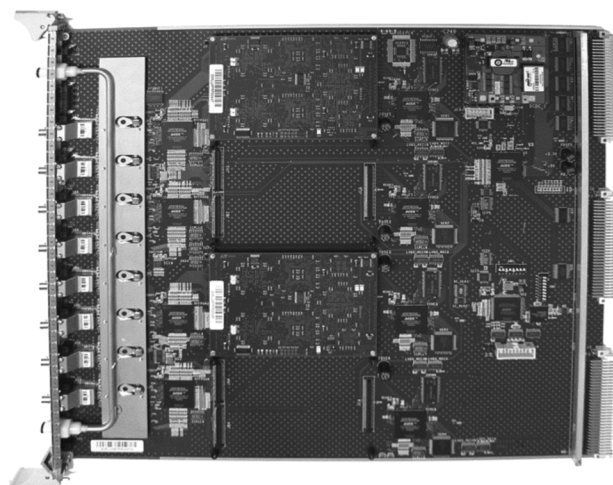
Fig. 1. Picture of the TileCal Read-Out Driver (ROD) electronic board.

I. INTRODUCTION

ATLAS [1] is a general purpose experiment for the Large Hadron Collider (LHC) [2], an accelerator where proton beams will collide each 25 ns with a 14 TeV center-of-mass energy. Both ATLAS and LHC are currently under construction at CERN and the first hadronic collisions are scheduled for April 2008. The main goal of the ATLAS experiment is to explore the physics at the multi-TeV scale, with special interest at the Higgs sector and the physics beyond the Standard Model [3]. The trigger system in ATLAS [4] is divided in three levels, which are responsible for selecting the events which contain potentially interesting physical information. This way, the 40 MHz interaction rate is reduced to only a 100 Hz data storage rate.

The calorimetry in ATLAS is comprised of two main detectors: the hadronic Tile Calorimeter (TileCal) in the central region [5], which is a sampling calorimeter made of iron and scintillating tiles, and the Liquid Argon (LAr) calorimeter [6] (with a central electromagnetic part, a hadronic endcap calorimeter and a forward calorimeter).

Longitudinally TileCal is divided in a long barrel (LB) and 2 extended barrels (EBs). Each half LB and each EB defines a detector partition, with its own trigger and dead-time logic, completely independent from the data acquisition point of view. In the ϕ direction, each TileCal barrel is divided in 64 modules.

The energy deposited by the particles in the calorimeter produces light in the active medium. This light is routed to Photo Multiplier Tubes (PMTs), which are the first elements of the Front-End (FE) electronics. The pulses from the PMTs are sampled and digitized at 40 MHz by 10-bit Analog to Digital Converters (ADCs). All FE electronics (shapers, amplifiers, digitizers, etc.) are integrated in a compact structure called superdrawer. There are 2 superdrawers in each LB module and one superdrawer in each EB module.

The Read-Out Driver (ROD) electronic boards [7] are the central element of the TileCal Back-End (BE) electronics. The RODs will process in real time the events selected by Level-1 trigger at a 100 kHz maximum rate and build the ROD fragments to be sent to Level-2 trigger. In addition, online algorithms can provide additional information which is also sent to the next trigger level, such as the energy, timing and a quality factor (pileup estimation) or muon tagging.

One ROD can handle 8 input fibres from 8 different superdrawers. Thus, 8 RODs are needed to read-out a TileCal partition (64 modules) and 32 RODs are needed to read-out the whole calorimeter. Fig. 1 shows a picture of a ROD board.
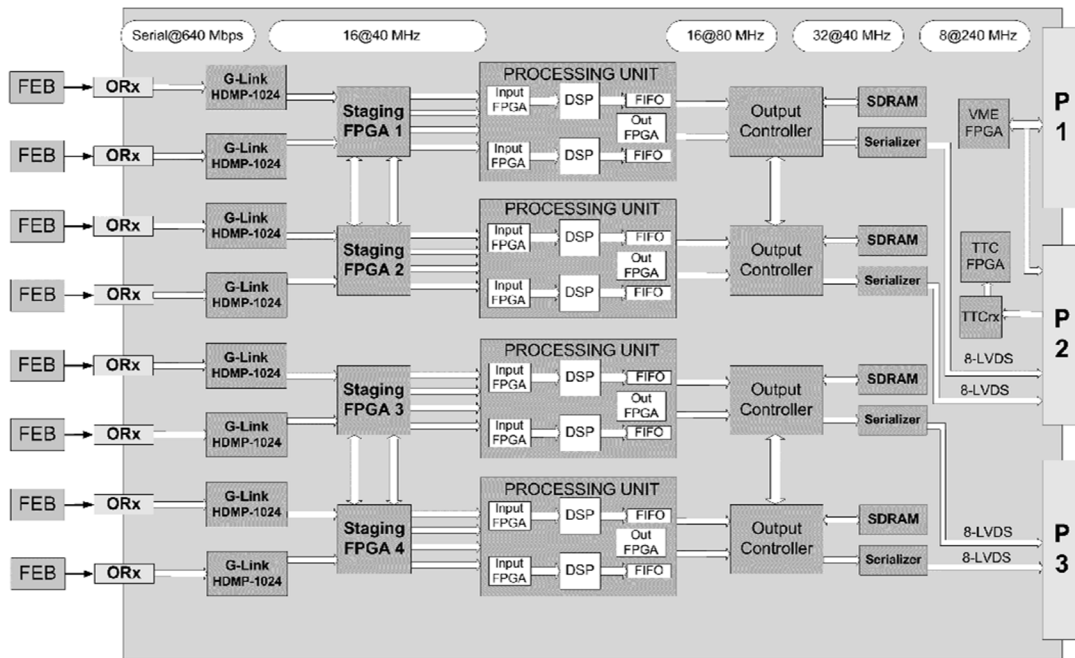
Fig. 2.   Diagram of the ATLAS calorimeters common ROD. All components described in Section II are shown.

II. TILECAL ROD DESCRIPTION

After several studies performed during the design period, both ATLAS LAr and Tile calorimeters decided to use a common ROD motherboard. Since the specifications are not the same in both detectors some adaptations are needed in order to share a common motherboard. The functionality of all the ROD components (Fig. 2) for the TileCal case is described in the following subsections.

A. Optical Receivers

The data coming from the FE are received in the Optical Receivers (ORxs) located in the front panel of the ROD. There are 8 ORxs mounted on each ROD and each one receives data from one detector superdrawer. The optical signal received is transformed by the ORx to electrical signal in Positive-referenced standard Emitter-Coupled Logic (PECL).

B. HDMP-1024 Deserializers

The signals from the ORxs are deserialized by 8 HDMP-1024 PMC-Sierra G-Links. The serializer chip used in the TileCal FE to send the data to the BE electronics is the HDMP-1032, but LAr uses the HDMP-1022. In consequence, HDMP-1024 was chosen for the common ROD motherboard. Nevertheless, the compatibility of the serializers used in the TileCal FE and the deserializers used in the ROD was checked in long term burn-in tests with optimal results. In TileCal, the G-Links are clocked at 40 MHz, which implies that each 25 ns a 16-bit word is received in the 8 G-Links, providing a maximum ROD input data bandwidth of 5.12 Gbps (the bandwidth used in ATLAS physics runs assuming the maximum Level-1 trigger rate of 100 kHz is only 3.53 Gbps).

C. Staging FPGA

There are 4 Staging Field Programmable Gate Array (FPGA) chips per ROD (ALTERA ACEX EP1K100FC484-1, 40 MHz

with 3×16 kbits internal memories) which distribute the input data to each Processing Unit (PU) (see below). Other functionalities of the Staging FPGA are, for instance, the monitoring of the G-Link temperature and data injection to the PUs from an internal memory for debug and calibration tests.

It is possible to route the output from up to 4 Staging FPGAs to one PU. Thus, with only 2 PUs all the data arriving to the ROD can be processed. This is the so-called staging operation mode which will be used by default during normal TileCal operation.

Nevertheless it is possible to mount up to 4 PUs in the ROD. In this case, each PU processes the data coming from 2 Staging FPGAs. This is the full operation mode and could be used as a future upgrade to double the processing capabilities of the ROD.

D. Processing Units

The ROD has 4 slots for PU mezzanine boards, even though only 2 PUs are currently used in TileCal, which allows flexibility for future upgrades. Each DSP PU is equipped with 2 Input FPGAs (ALTERA CYCLONE EP1C6F256C8, 80 MHz with 2×32 kbits internal memories) and 2 DSPs (Texas Instruments TMS320C6414GLZ; L1 SRAM: 32 kBytes; L2 SRAM: 1024 kBytes). These dual devices get double processing power in a single PU board, as it is divided in two independent processing chains. In the staging operation mode each Input FPGA and DSP has to process data coming from 2 Staging FPGAs.

In addition, the PU has an Output FPGA (ALTERA CYCLONE EP1C6F256C8; 80 MHz) which provides interface with the ROD VME FPGA and the Timing, Trigger and Control (TTC) [8] FPGA. Their main functionalities are the booting and configuration of the DSPs and Input FPGAs as well as the interface between the VME bus and the DSP Host Port Interface and multichannel buffered serial ports (to read histograms, to have access to the DSP internal memory and to transmit TTC information to the DSP for data synchronization).

The data received in the Input FPGA are checked to validate the correct transmission from the FE and formatted as needed by the DSP. When an event is ready the Input FPGA interrupts the DSP which initiates a Direct Memory Access (DMA) transfer to read the data. The data are processed in the DSP and stored in an external First-In, First-Out (FIFO) memory (IDT72V253L7-5BC, 70 kbits). The DSP has a 4.6-kbit input buffer where it is possible to store up to 16 physics events. In order to avoid event losses if this input buffer is almost full the DSP is able to stop the partition trigger generation by setting a busy signal.

E. Output Controller

The Output Controller (OC) FPGA (ALTERA ACEX EP1K100FC484-1; with 2 8-kbit Internal FIFOs) is the ROD output distributor. There are 4 OCs mounted in the ROD but only 2 are currently used in TileCal. Each OC reads out the data coming from one PU and builds a ROD fragment with the reconstructed data obtained from 4 TileCal superdrawers. It also adds S-Link header and trailer words to the output data according to the ATLAS Trigger and Data Acquisition (TDAQ) data format [9]. The OC sends this ROD event fragment to Level-2 trigger through the 2 S-Link Link Source Cards (LSCs) located in the Transition Module (TM) [10], module associated with each ROD. Nevertheless it is also possible to configure the OC to store the events in a 128 Mbit Synchronous Dynamic Random Access Memory (SDRAM) and to read them out from the VME bus.

F. VME FPGA

There is one VME FPGA (ALTERA ACEX EP1K100FC484-1) in each ROD which provides communication between the crate controller and all the components in the ROD. This communication allows configuration tasks, remote access to the Joint Test Action Group (JTAG) chain and PU booting. The busy logic and busy monitoring system are also implemented in the VME FPGA, as well as the interrupt handling.

G. TTC FPGA

The TTC information is received in ROD crates by the Trigger and Busy Module (TBM) [11] and it is distributed to all the RODs in the crate through the crate backplane. This information is decoded at ROD level by the TTC receiver (TTCrx) [12] chip and managed by the TTC FPGA (ALTERA ACEX EP1K30TC144) which sends this information to the PUs. It is possible to trigger the ROD by the VME bus, locally or using the TTC information, which will be the normal trigger mode at the LHC.

III. TileCal ROD Production

In addition to the 32 ROD boards needed to read out the whole TileCal, 6 boards have been produced as spare units. The ROD production consisted of the test and validation of these 38 RODs modules. In order to verify the correct performance of the RODs a set of tests were performed on a specific test bench. In this section the test bench used during ROD production, the tests performed and the results obtained are presented.
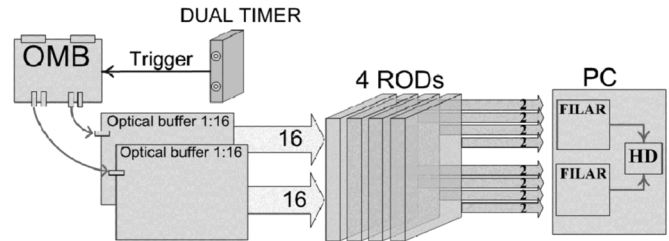

Fig. 3. Diagram of the TileCal ROD production test bench. The OMB generated events upon a trigger receipt, which were sent through the OB to the RODs under test. The output data from the RODs were sent to a PC containing FILAR cards and stored on disk.

A. Production Test Bench

The test bench designed for the TileCal ROD validation was divided into an injection part, a ROD crate and an acquisition system (Fig. 3).

The injection part emulated the FE by generating events and sending them to the RODs being tested. The data generator used was the VME Optical Multiplexer Board (OMB) 6U prototype [13] and the injection rate was controlled with a dual timer connected to the OMB. Besides, a 1:16 Optical Buffer (OB) [14] was designed for the ROD production to increase the number of optical links with data.

Apart from the crate controller computers in the crates, 3 additional PCs were used during the production for configuration tasks, acquisition and data checking. One of them ran the main user interface computer responsible for the configuration tasks of all the devices in the test bench. Another dual CPU PC, with 2 Four Input Links for Atlas Read-out (FILAR) cards installed, read out data from up to 4 RODs, and store the data in a shared file system. Finally, the third computer, with access to this shared file system, checked the data online.

The following subsections explain all the hardware and software elements used in the ROD production test bench.

1) Optical Multiplexer Board 6U Prototype: Due to the fact that the FE electronics will be affected by high radiation doses during the LHC lifetime, TileCal was designed as a data system with redundancy in such a way that the same data are processed and sent to the ROD with two separated lines. The final OMB will be placed in the ATLAS acquisition chain just after the FE receiving as input the 2 optical links with the same data. It will check for errors both sets of data and decide which one is actually sent to the ROD.

Besides, it will be possible to use the final OMB to emulate the FE in order to perform ROD calibrations and tests while the detector is not available. Taking advantage of this functionality, the OMB 6U prototype was used during the ROD production tests as data injector to the RODs to verify their correct operation.

Fig. 4 shows a picture of the 6U OMB used during the ROD production. The board was designed with 2 processing FPGAs which can handle 2 input links and one output link each. This means that the 6U OMB has 4 optical input links and 2 output links. In addition one more FPGA provides interface with the VME bus.
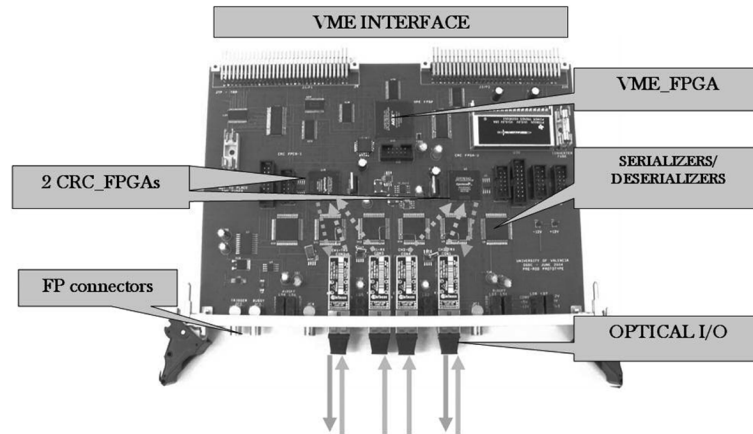
Fig. 4.   Picture of the 6U OMB prototype. The main elements of the board are labeled.

Regarding the data injection capabilities of the board, the 6U OMB has 2 different injection modes: it can either generate events internally or the events can be stored in an internal memory through the VME bus. In both cases the events are injected to the ROD on receipt of a trigger signal, which can be either external (for instance from a dual timer) or internal (using an internal oscillator with configurable rate).

2) Optical Buffer 1:16: The OB is a 9U VME board that was expressly designed for the ROD production in order to increase the number of links injecting data to the RODs by 1:16 factor. It will not be used in the ATLAS final configuration.

Thus, with only one OMB 6U prototype and 2 OBs we had 32 links, that is, data can be injected to 4 RODs simultaneously, the amount needed to read out half a TileCal partition.

3) ROD and FE Emulation Crates: Two 9U VME crates were used during the ROD production. One of them was used as injection crate and it housed one TTC VMEbus interface (TTCvi) module for trigger configuration, one 6U OMB as data generator and 2 OBs. The other crate was the ROD crate and it contained the RODs to be tested (up to 4 RODs could be simultaneously validated), the TMs and one TBM which collects the busy signal from all the RODs in the crate and vetoes the incoming triggers.

4) Software: Specific software was written for ROD production tasks based in the TDAQ framework, standard in online tasks in the ATLAS experiment. TDAQ offers a graphical user interface which was customized for ROD production. ROD Crate DAQ [15] applications were developed to access and control all the hardware modules for tests and data acquisition. Additional monitoring applications were written to check the acquired data. A ROD production database was developed to store the ROD and related modules hardware identifiers together with the test results.

B. Validation Tests

The validation process of each TileCal ROD board was divided into two different phases. The first phase covered all the ATLAS calorimeters common RODs, while the second phase involved only the TileCal RODs.

The ATLAS calorimeters common RODs were delivered from the industry with some general and mechanical checks to the University of Geneva, responsible of the production of

TABLE I
TEST PROTOCOL FOR THE TILECAL ROD VALIDATION

LEVEL	NUMBER OF RODs	RATE	MINIMUM TIME
0	1	3 DVS tests	
1	1	200 Hz	4 h
2	1	1 kHz	8 h
3	4	1 kHz	72 h

these common RODs, where functionality tests were performed on the boards to guarantee the correct performance of all their components.

After the first phase was completed at Geneva, the RODs were sent to the TileCal group at IFIC-Valencia, where they were modified in order to be adapted to the TileCal requirements. These adaptations include modification in hardware (to be compatible with TileCal FE) and firmware (TileCal specific firmware have been developed for the Staging FPGAs, the PU Input FPGAs and the DSPs).

Once the adaptations were finished, the validation of the boards started. Table I shows the 4-level test chain used in the validation protocol. The tests performed on the first level, called level 0, were static tests in the sense that no external data flow was present. This test level was composed by 3 TDAQ Diagnostic and Verification System (DVS) tests, which basically certified the correct operation of all the programmable devices on the motherboard as well as verified the correct data flow inside the ROD by injecting some events from the Staging FPGA and reading them out in the OC.

The next 3 test levels were dynamic tests with different number of RODs, injection rates and test duration. Data were generated in the 6U OMB and sent to the RODs, where they were read out, stored in disk and finally checked. The DSP online algorithms (see Section V) were disabled during the tests, so that the raw data was transmitted trough the system as they were received.

As the OMB sent the Cyclic Redundancy Check (CRC) word of each event attached as last word, it was checked after the transmission over the whole acquisition chain to verify the integrity of the data read out by the ROD system. Furthermore, the consecutiveness of the events was also checked to verify that no event was missing after the data acquisition. The maximum

TABLE II
SUMMARY OF TESTS DONE TO THE TILECAL RODS DURING THEIR VALIDATION

	LEVEL 1	LEVEL 2	LEVEL 3	EXTRA RUNS
TIME (h)	259	405	2001	560
PROCESSED EVENTS	269×10^6	2×10^9	8×10^9	3×10^9
CHECKED EVENTS	269×10^6	395×10^6	781×10^6	280×10^6

event checking rate reached by the online data check application was approximately 400 Hz. For higher injection rates the software was not able to check all the events but only a fraction of them.

For this reason, the level-1 test was meant to check all the processed events and the trigger rate was set to 200 Hz. This test was considered as passed when the ROD had processed data for more than 4 hours without errors.

The level-2 test was also a single ROD dynamic test. With the injection rate set to 1 kHz (checking only about 40% of the events processed). At such a rate, busy signals appear due to the data storage process. Thus, the correct busy handling was also checked in this test, which was considered as passed when the ROD had processed data without errors during more than 8 hours.

Finally, the level-3 test was a multiple ROD burn-in test at high rate: 4 RODs were tested together during at least 72 hours at a 1 kHz trigger rate (checking approximately 10% of the processed events).

If no errors were found during the 4 test levels, the ROD was fully validated, labeled and shipped to CERN for installation in the ATLAS USA15 cavern.

C. Validation Tests Results

Taking into account all the tests done during the production period each ROD has been processing data during at least 84 hours, that is on average 270×10^6 events with 38×10^6 events checked without errors. Besides the proper ROD production, extra runs were taken during the production period in order to validate some firmware upgrades. Table II summarizes the tests results in terms of time, events processed and events checked in the 3 dynamic test levels during the RODs production.

Globally, the ROD system has been processing data during 3225 hours with a total of 13×10^9 events processed from which 1.7×10^9 of them were checked without errors. As the events injected by the OMB had 176 32-bit words, the Bit Error Rate (BER) at a 95% confidence level is 3×10^{-13}.

D. Other Tests During ROD Production

Due to the limitations in the FILAR cards available during the ROD production the maximum event rate which could be achieved at that time was ~1 kHz, as mentioned above. However, later on, when the final ROBin cards were available high rate tests were performed on the ROD system. In these tests it was shown that the ROD can accept and process data at 100 kHz, and the output data bandwidth available is enough to transmit raw data physics events also at this rate when working in full mode. When running in staging mode the maximum achievable rate in the current configuration is 50 kHz, enough during the first operation years of LHC when the ATLAS Level-1 trigger maximum rate will be set to 50 KHz. After this period, in order to output raw data at 100 kHz the number of LSCs in the TM can be increased to 4 instead of the current 2.

In addition, tests on the system behaviour under critical situations were also performed in the laboratory. For instance, FE failures were simulated by disconnecting ROD inputs randomly in the middle of a data taking run to check that the acquisition was not stopped.

Apart of the validation of the ROD boards during the ROD production the correct performance of the selected G-Link cooling system was also tested. In the LAr RODs these chips are clocked at 80 MHz which is beyond the manufacturer specifications. Nevertheless, the LAr group demonstrated the correct performance of this chip clocked at 80 MHz if the temperature is kept below 35°C and, in consequence, water cooling is needed for these chips. In TileCal the G-Links are clocked at 40 MHz, well within the manufacturer specifications, who guarantee a correct operation of the device up to 85°C. Hence, in this case the own crate air cooling system is used instead of water cooling.

Some studies were performed in order to study the temperature behaviour of the chips and ensure that the air cooling is enough to keep the G-Link temperature inside its operation range. In all the configurations studied G-Link temperatures did not exceed 60°C, confirming the effectiveness of the cooling option chosen [16].

IV. COMMISSIONING

The main objectives of the commissioning phase of the experiment are the integration of all the hardware and software elements and the test of the whole system in a setup close to the final one. During TileCal commissioning, tests which involve data acquisition are performed for module certification and calibration studies. Furthermore, during commissioning, a program of cosmic rays data acquisition has been planned for TileCal standalone and in combination with other ATLAS subdetectors (LAr and muon spectrometer).

In the TileCal standalone cosmics runs, the trigger was given by TileCal itself without any scintillator, using custom coincidence boards which take as input the trigger tower signals from 12 superdrawers. These trigger boards have two operation modes: single tower trigger and back-to-back tower trigger (see Fig. 5). In the single tower mode, a trigger is sent if the total energy deposited in a tower is greater than a given threshold. In the back-to-back mode, a trigger is sent only if the energy deposited in a tower and in its geometrically opposite is larger than a configurable threshold, selecting events where the particles pass close to the interaction point.

Thus, data coming from TileCal during commissioning tests or cosmics physics runs are read out with the RODs and processed online using the algorithms implemented in the ROD DSPs which are described in the following section.

V. DSP ONLINE ALGORITHMS

As mentioned above, the ROD PUs are equipped with 2 DSPs. They are fixed-point processors which use the advanced Very Long Instruction Word (VLIW) architecture. These DSPs can perform up to 5760 million instructions per second (MIPS) working at 720 MHz. Their CPU contains
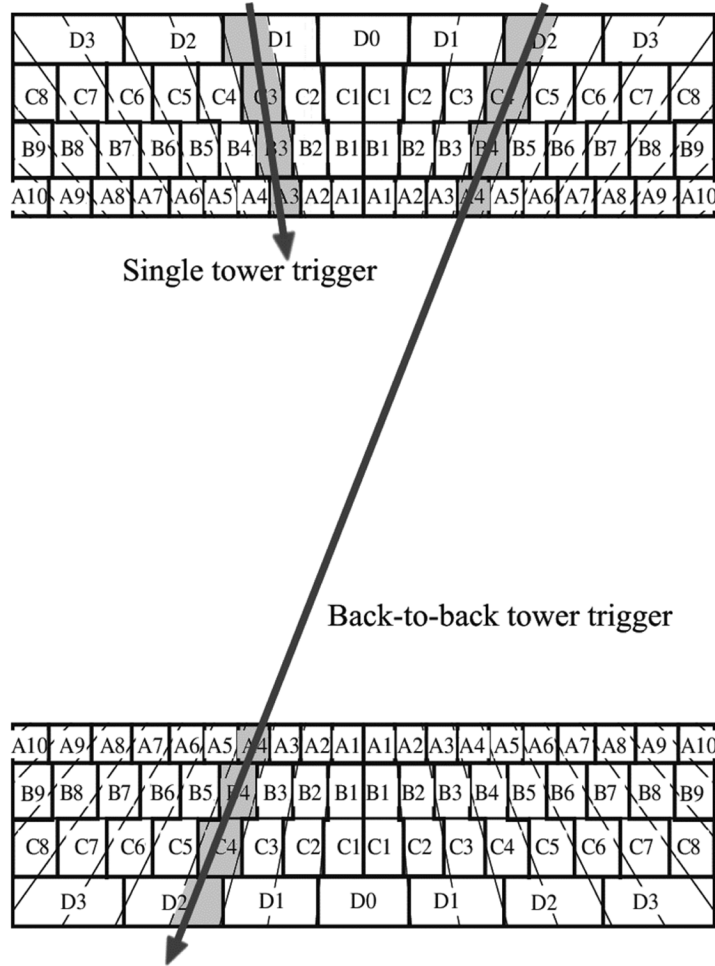
Fig. 5.   TileCal standalone cosmics back-to-back and a single tower trigger.

2 Multiplier and 6 Arithmetic Logic Units (ALUs); therefore, fast divisions should be implemented as shift instructions or using Look-Up-Tables (LUTs). The algorithms implemented in the DSPs should be accurate and fast enough to meet the 10 μs maximum latency in order not to introduce dead time at Level-1 trigger.

We present the performance of 2 algorithms: the Optimal Filtering (OF) algorithm which calculates the amplitude and the phase of the digital signal from the TileCal read-out and the Muon Tagging algorithm (MTag) which identifies the passage of η projective muons through the calorimeter.

A. Optimal Filtering Algorithm

Optimal Filtering (OF) [17] calculates the amplitude and the phase of the digitized signal through a weighted sum of its digital samples

$$A = \sum_{i=1}^{N} a_i S_i \qquad (1)$$

$$\tau = \frac{1}{A} \sum_{i=1}^{N} b_i S_i \qquad (2)$$

where S_i is the sample taken at time t_i. The amplitude, A, is the distance between the peak and the pedestal which is the baseline
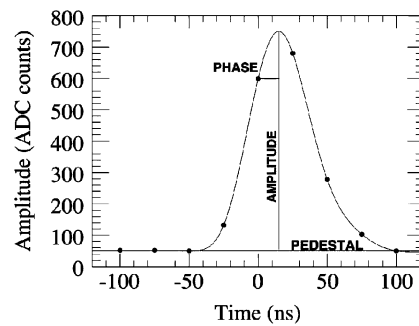

Fig. 6.   Plot of the distribution of the signal digital samples and definition of phase, amplitude and pedestal.

of the signal. The phase, τ, is the time between the peak and the central sample (see Fig. 6).

The procedure of calculating the OF weights, $\boldsymbol{a}$ and $\boldsymbol{b}$, minimizes the noise contribution on the amplitude and phase reconstruction. They are calculated assuming small phases which are not the real conditions during the TileCal commissioning, where the data arrival is not synchronized with the trigger clock. In order to use the same algorithm we have implemented iterations in the amplitude and phase calculations
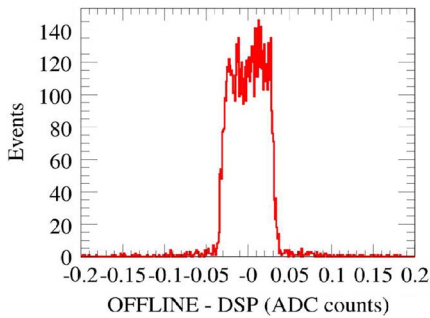
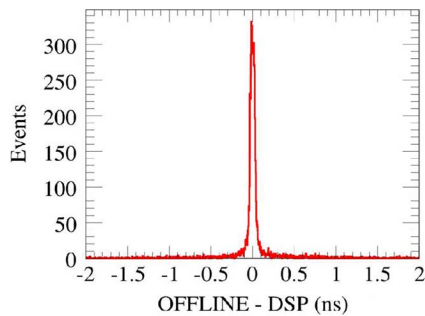Fig. 7. Histogram of the difference between the offline and online (inside the DSPs) amplitude reconstruction.

Fig. 8. Histogram of the difference between the offline and online (inside the DSPs) phase reconstruction.

$$A_k = \sum_{i=1}^{N} a_i \bigg|_{\tau_{k-1}} S_i \qquad (3)$$

$$\tau_k = \frac{1}{A_k} \sum_{i=1}^{N} b_i \bigg|_{\tau_{k-1}} S_i. \qquad (4)$$

The index k runs from 1 to 3. The initial phase, τ_0, is the time between the central and the maximum sample. During each iteration, the weights used are calculated assuming that the peak is around the previous reconstructed phase, τ_{k-1}. We have observed that the amplitude value converges with three iterations. Hence, the result of the third iteration, A_3 and τ_3, is the final value obtained for the amplitude and phase of the channels.

The DSPs performance is being tested during the TileCal commissioning with the OF algorithm. Figs. 7 and 8 show the difference between the offline calculation and the online reconstruction, inside the DSPs, for the amplitude and phase, respectively. Concerning the amplitude, the differences were around 0.03 ADC counts for amplitudes larger than few ADC counts. The differences on the phase are expected to be larger due to the use of a 16-bit LUT; in any case, the differences are around 0.3 ns for amplitudes larger than few ADC counts.

B. Low p_T Muon Tagging Algorithm

One of the ATLAS goals is to carry out a wide B-physics program [3], in which the identification of low p_T muons plays a crucial role. TileCal gives the possibility to detect these muons in the low p_T range where the first level trigger with the muon spectrometer standalone is not efficient. The aim of this Muon

Tagging algorithm (MTag) [18] is to identify muons in with less than 5 GeV, where most of them are bent by the magnetic field in such a way that cannot be properly reconstructed by the muon spectrometer or are even stopped in TileCal.

The basics of this algorithm is to search for muons in TileCal following projective patterns in η, taking advantage of its projective geometry and taking into account the typical muon energy deposition (less than 3 GeV). The muon search starts from the outermost layer of TileCal (which presents the cleanest signals due to the low background from particle showers) looking for cells with energy deposition compatible with a muon signal and continue through the central and innermost layer cells following a η projective pattern.

The energy deposition in each cell must be comprised between a lower and an upper threshold

$$\mathrm{thr}_i^{\mathrm{low}} \leqslant E_i \leqslant \mathrm{thr}_i^{\mathrm{high}} \quad i = 1, 2, 3. \qquad (5)$$

For this purpose, a set of energy thresholds are stored in a LUT and accessed during algorithm execution inside the DSP. The low energy threshold is used to cut the electronic noise and the minimum bias pileup and a value of 150 MeV is being used for all cells during commissioning runs. The high energy thresholds are meant to discard the hadronic showers and their tails and each cell has a specific threshold depending on its geometry.

The efficiencies and fraction of fakes of the MTag algorithm [19] have been studied with different samples of Monte Carlo data. High efficiencies ($\sim$80% for muons with p_T above 2 GeV) and low fraction of fakes (down to 6%) have been found during these studies. Studies on the performance of the algorithm [20] show that the estimated rate for the MTag algorithm used at LVL2 is 860 Hz, with only 200 Hz due to fake tags. As the total rate is compatible with the total LVL2 rate (1 kHz), the implementation and usage of this algorithm at LVL2 is feasible.

The MTag algorithm has been implemented in the DSP core and takes as input the energy previously reconstructed in the DSP with OF. This algorithm is processed in parallel for all TileCal superdrawers separately in all the RODs and its output (number of muons found and their η and ϕ coordinates) is encoded in a dedicated fragment to be collected for Level-2 trigger.

The MTag algorithm is currently used in the commissioning cosmics data acquisition. The algorithm online performance is being validated successfully with commissioning cosmics data, comparing with the results obtained with the algorithm applied offline.

Results of the comparison between the MTag offline and online performance are shown in Fig. 9, where the distribution of the energy deposited by the muons tagged offline and online (inside the DSPs) for a TileCal commissioning cosmics run presents a very good agreement.

C. Online Algorithms Latency

The processing time of the online algorithms implemented in the DSP is a very important issue, as the the maximum latency at Level-1 trigger will be 10 μs to meet the 100 kHz maximum trigger rate, although in the first years of operation of LHC this rate will be of only 50 kHz. The current implementation of the OF algorithm is meant to properly reconstruct desynchronized cosmics muons making use of iterations, which will not
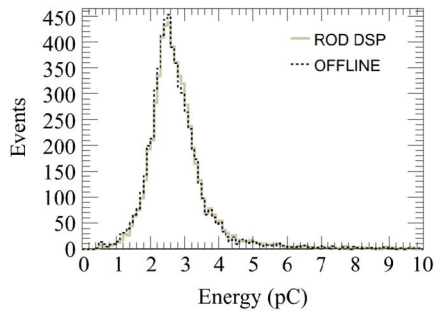
Fig. 9. Energy deposited by the offline and online (inside the DSPs) tagged muons for a TileCal commissioning cosmics run.

be needed in LHC. Furthermore, the current implementation of the DSP algorithms is coded in C and a great improvement is expected after the foreseen migration to assembler.

The current latency for the OF algorithm measured when working in staging mode and reconstructing all the channels available in a superdrawer is approximately 54 μs. Recent developments are being made in order to skip the reconstruction of pedestal-like events which will reduce the processing time. The MTag algorithm is considerably faster and its processing latency is only 2.2 μs for cosmics data in the current implementation.

VI. CONCLUSION

This paper reported on the description, production and current operation of the TileCal ROD electronics boards. The production test bench developed for the ROD production was used to fully validate the 38 ROD modules, verifying their properly operation and data processing capabilities, obtaining a data transmission BER of 3×10^{-13} with a 95% confidence level.

After their validation, the RODs have been installed for TileCal data processing during commissioning tests. Moreover, the OF and MTag algorithms in the DSP are computing the amplitude and phase for all channels and tagging muons, respectively, during commissioning cosmics runs.

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