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Ferroelectrics onto silicon prepared by chemical solution deposition methods: from the thin film to the self-assembled systems

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The work of the authors during the last years on ferroelectric thin and ultra-thin films deposited by Chemical Solution Deposition (CSD) onto silicon based substrates is reviewed in this paper. Ferroelectric layers integrated with silicon substrates have potential use in the new micro/nanoelectronic devices. Two hot issues are here considered: 1) the use of low processing temperatures of the ferroelectric film, with the objective of not producing any damage on the different elements of the device heterostructure, and 2) the downscaling of the ferroelectric material with the aim of achieving the high densities of integration required in the next generation of nanoelectronic devices. The UV-assisted Rapid Thermal Processing has successfully been used in our laboratory for the fabrication of ferroelectric films at low temperatures. Preliminary results on the CSD preparation of nanosized ferroelectric structures are shown.

Keywords:Chemical Solution Deposition (CSD), ferroelectricity, thin film, ultrathin film, nano-sized structures.

Ferroeléctricos sobre silicio preparados por métodos de depósito químico de disoluciones: de la lámina delgada a los sistemas auto-ensamblados.

Este artículo revisa el trabajo realizado por los autores durante los últimos años sobre lámina delgada y ultra-delgada ferroeléctrica preparada mediante el depósito químico de disoluciones (CSD) sobre substratos de silicio. Las películas ferroeléctricas integradas con silicio tienen potenciales usos en los nuevos dispositivos micro/nanoelectrónicos. Dos aspectos claves son aquí considerados: 1) el uso de bajas temperaturas de procesado de la lámina ferroeléctrica, con el fin de no dañar los diferentes elementos que forman la heteroestructura del dispositivo y 2) la disminución de tamaño del material ferroeléctrico con el fin de conseguir las altas densidades de integración requeridas en la próxima generación de dispositivos nanoelectróncos. Los procesos térmicos rápidos asistidos con irradiación UV se están usando en nuestro laboratorio para conseguir la fabricación del material ferroeléctrico a temperaturas bajas compatibles con la tecnología del silicio. Se muestran resultados preliminares sobre estructuras ferroeléctricas nanométricas preparadas por CSD.

Palabras clave: Depósito químico de disoluciones (CSD), ferroelectricidad, lámina delgada, lámina ultra-delgada, estructuras nanométricas.

1. INTRODUCTION

Ferroelectric materials have a wide range of properties of interest for electronic devices: high permittivity values (Dynamic Random Access Memories, DRAMs), spontaneous polarisation that can be switched with the electric field (Non Volatile Ferroelectric Random Access Memories, NVFERAMs), piezoelectric activity (sensors and actuators) or pyroelectric properties (sensors) (1-3). Ferroelectrics in thin film form deposited onto silicon substrates have been intensively studied during the last decades (4-5). The current trend in microelectronics is the reduction of the device size below the micron level (nanometer sizes) (6). This will increase the integration density of the devices, and will also allow low-voltage and low-power consumption. Therefore, ferroelectric materials with nanometer sizes are of high technological interest for the next generation of electronic devices. Fig.1 shows this trend for ferroelectric materials. The important role of ferroelectric thin and ultra-thin films, and nano-sized structures in the design and fabrication of the new micro/nanoelectronic devices is summarised in this figure.

The Chemical Solution Deposition (CSD) method is one of the different deposition techniques used for the preparation of ferroelectric materials supported onto a substrate (7). CSD is a low-cost technique that makes easy the preparation of complex mixed oxide materials (compositions with two or more cations, as it is the case for ferroelectric perovskites) with a well-adjusted stoichiometry. An important characteristic of the CSD methods is the high degree of control of the chemistry of the precursor solutions used in the deposition of the films. This opens the opportunity to produce materials with tailored properties for specific applications. All this makes CSD a powerful method for the fabrication of ferroelectric materials with different morphologies as thin or ultra-thin films, or even as nano-sized structures.

This paper reviews the work of the authors during the last years on ferroelectric materials supported onto silicon substrates and prepared by CSD. Special attention is paid on the fabrication of thin films at low-temperatures compatible with those used in the Si-technology. Following the actual trends of reduction of the microelectronic device sizes, our work has recently focused on the fabrication of nano-sized
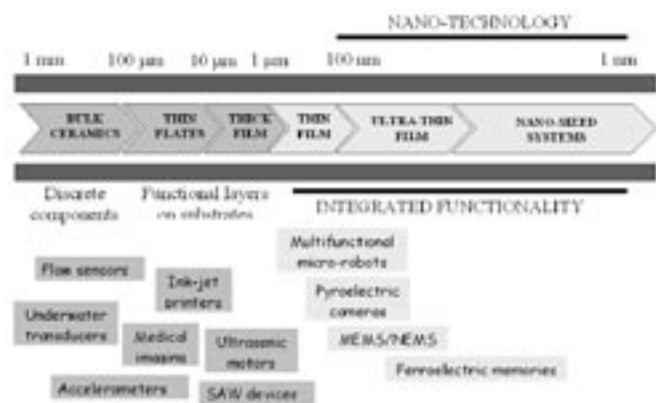
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Fig. 1- Actual trends in ferroelectric materials.

ferroectrics: in a first approach as continuous ultra-thin films (film thickness <100 nm) and in a second approach as nano-sized structures in the sub-100nm size regime (ferroelectric nano-capacitors).

2. FERROELECTRIC THIN FILMS AND THE Si-TECHNOLOGY: THE ROLE OF CSD PREPARATION METHODS

The microelectronics industry is at present based on the technology of silicon. The present trends of the microelectronics industry towards the progressive miniaturisation of devices, in order to increase its computational capability at a low cost (6), make necessary, among other things, the fabrication of extremely thin gates. This means that the SiO_2 layers of these gates must reduce their thickness down to approximately 2nm. The fabrication and performance problems that may arise as a consequence of this size reduction have been discussed by different authors. (8-10). Some authors propose the use of alternative dielectric materials more adequate for the new gate dimensions (11). Ferroelectrics are among them and, therefore,

the direct integration with the silicon semiconductor substrate needs to be completely solved first.

The CSD methods are used for the deposition of ferroelectric thin films involving solutions as precursors that can be synthesised by sol-gel or prepared from different chemical reagents (metal-organic compounds, inorganic salts, etc.) The solution is deposited on the substrate usually by spin-coating. The drying and partial pyrolysis of the wet coating results in an amorphous layer that has to be crystallized, normally by the use of Rapid Thermal Processing (RTP) (12-14).

The substrate more commonly used consists of a heterostructure formed by the (100) Si wafer, spontaneously oxidised in air, a ~50nm thick TiO_2 adhesive layer and a ~100nm thick Pt electrode. Onto these $Pt/TiO_2/SiO_2/Si$ substrates, three types of ferroelectric materials have been prepared in our laboratory: thin films, ultrathin films and nanosized structures.

The macroscopic ferroelectric characterisation of the films is carried out on capacitors, formed by the deposition of Pt top electrodes. However, the nanoscale characterization of the properties requires the use of a recently developed technique based on the scanning force microscopy. An electric field applied between a conductive tip and the sample produces a piezoelectric response that is analysed in what is called Piezoresponse Scanning Force Microscopy (PFM) (15). Local piezoelectric hysteresis loops and maps of the distribution of the polarization in the film can be obtained with this technique.

3. FERROELECTRIC THIN FILMS PREPARED AT LOW TEMPERATURES

The crystallization of the ferroelectric material requires usually temperatures over 600ºC, which are well above those allowed in the fabrication of integrated circuits to keep the integrity of all components: <550ºC.

Different approaches to lower the crystallization temperature using CSD methods have been reported in the literature for ferroelectric films (16-22). Table I summarises

TABLE I. SOME OF THE LOW-TEMPERATURE CSD METHODS REPORTED IN THE LITERATURE FOR THE PREPARATION OF FERROELECTRIC THIN FILMS [50].

| Material	Method	T cryst (ºC) Long-Times	P_r ($\mu C/cm^2$)	Ec (kV / Cm)	Obervations
$BaTiO_3$	Ferrons [16]	200	0.06	---	Very poor ferroelectric response
PZT(52/48)	Bi_2SiO_5 [17]	450	20	38	
PZT(52/48)	Precursor type solution [18]	400	20	165	Ti-rich PZT composition
PZT(30/70)		430	36	66	Ti-rich PZT (70/30) compositions (γ~1.8×10^{-4} C/m²K)
PZT(40/60)	Multi-annealing RTP and precursor type solution [21]	450	8	47	Ti-rich PZT compositions
PZT(52/48)	Low-pressure annealing [22]	550	18	50	Only ultrathin films (<25 nm) Only tested with IrO_2 electrodes
Ca-PbTiO$_3$	PHOTO-ANNEALING [24]	450	11	108	Tested up to Ca-contents of 50 mol%. Tested pyroelectric response (γ~3.2×10^{-4} C/m²K)
Ca-PbTiO$_3$ La-PbTiO$_3$	PHOTO-ANNEALING [23]	550	22	165	Tested also piezoelectric response (d_{33}~30-40 pm/V)
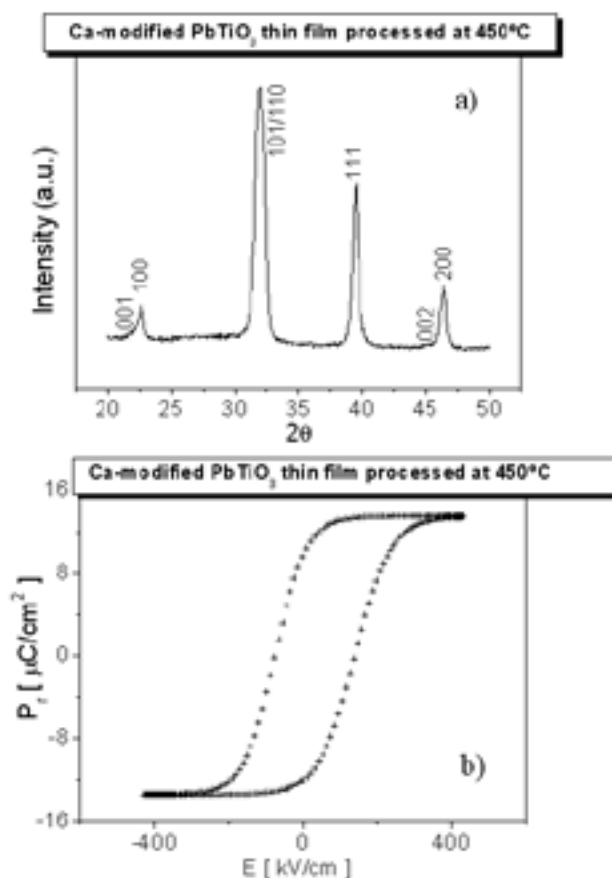
Fig. 2- PbTiO$_3$ based thin film processed at low-temperatures (450ºC) by UV-assisted RTP. a) x-ray diffraction pattern and b) ferroelectric hysteresis loop.

these methods. In all the cases, the formation of the crystalline phase occurs at a relatively low temperature, but usually the resulting films do not have ferroelectric response, mainly due to their poor crystallinity. The synthesis of ultraviolet-sensitive solutions by using sol-gel processing (UV-photoannealing, Table I) (23) has made possible in our laboratory that the amorphous layers, after irradiation with UV-light, can be crystallised at temperatures compatible with the Si technology: 450ºC (24). This treatment was carried out in a JetClip SG JIPELEC equipment (25). The UV irradiation produces the

pyrolysis and oxidation of the organic components of the sol-gel film, which makes possible the formation of the M-O-M bonds of the ferroelectric perovskite at low temperatures. Fig.2 shows the x-ray diffraction pattern of a pseudocubic Ca-modified PbTiO$_3$ film, processed by UV-RTP at 450ºC (a) together with its ferroelectric hysteresis loop (b). The film is single phase with perovskite structure, and a well-defined ferroelectric response with values of remnant polarisation (P$_r$) over 10μC/cm^2, are measured in it.

4. FERROELECTRIC ULTRATHIN FILMS

The low-operation voltage and therefore the low-power consumption have been the driven forces for reducing the thickness of the active (ferroelectric) layer in devices below 100 nm. For this, the ultra-thin ferroelectric film should maintain remanent polarisation values enough to yield large piezoelectric activity, i.e. for MEMS/NEMS, or to store sufficient information that would not be lost with time (retention) or the reading and writing of the memory (fatigue), i.e. for NVFERAM.

CSD methods can also be used to prepare high quality films of thickness below 100 nm (26-28). Among them we choose the fabrication of Sr$_2$Bi$_2$Ta$_2$O$_9$ ultra-thin films, which show high densities and good ferroelectric properties (29,30). The chemical composition and the rheological properties of the precursor solution, as well as the crystallization process, were adjusted to obtain dense and continuous films with a thickness below 100 nm (Fig.3a) and with the expected layered perovskite structure (Fig.3b). The ferroelectric hysteresis loop measured in this ultrathin Sr$_2$Bi$_2$Ta$_2$O$_9$ film is shown in Fig.3c. It has to be noted that a voltage of only 2V is enough for the switching of P$_r$~7.5μC/cm^2, with a switching time of ~1.3μs. These P$_r$ values together with the large retention of the film (~10^{5}s) and its low fatigue (~10^{10} cycles) show the suitability of these ultra-thin films for their use in high density NVFERAM, that can use a low operation voltage.

5. NANO-SIZED FERROELECTRIC STRUCTURES

The reduction of the device size is essential to achieve high densities of integration. To achieve memory capacities on the order of Gbit, it is necessary the fabrication of memory cells
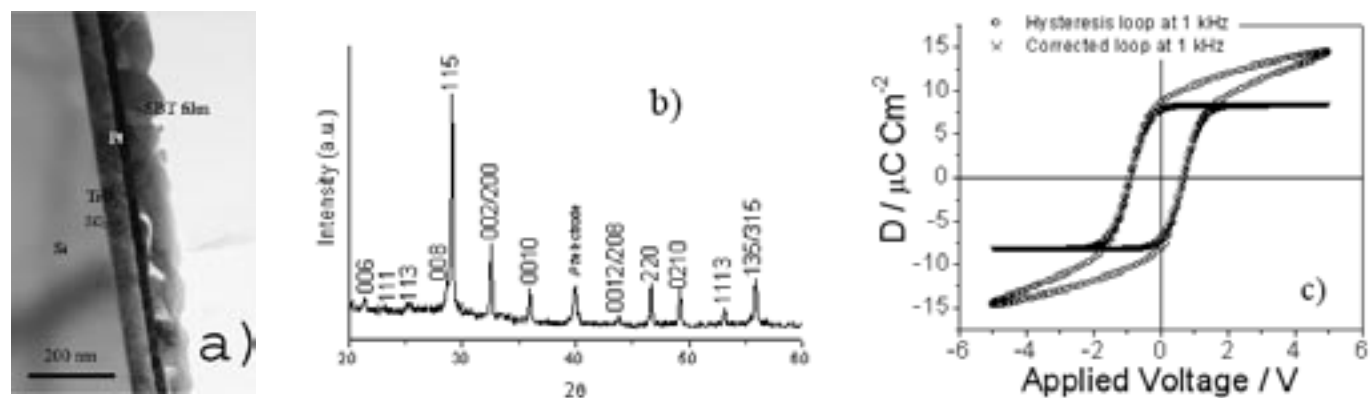

Fig. 3- Ultra-thin strontium bismuth tantalate film (30). a) Transmission electron microscopy image of the cross-section of the film, b) x-ray diffraction pattern and c) ferroelectric hysteresis loop The corrected loop, after conductance and high-field capacitance compensation using a method described in (31), is also shown.

not larger than 150x150 nm^2 and its ferroelectric capacitor will probably have a lateral dimension close to 100 nm (32). But, the fabrication of these nanosized ferroelectric structures is not straightforward and besides, difficulties for testing their ferroelectric properties will be found, since the conventional ferroelectric tests using extended top electrodes cannot be used in this case.

Piezoresponse force microscopy (PFM) is the characterisation technique more widely used nowadays in the ferroelectricity area to investigate nanoscale domain mapping and switching of nano-sized ferroelectric structures. This technique uses a scanning force microscope (SFM) with conductive tips for the application of an external ac voltage between the tip and the sample. This produces a local electromechanical response of the ferroelectric sample. The amplitude of this response provides information on the magnitude of the piezoelectric coefficient, while the phase difference between the excitation field and the piezoelectric response of the material is related to the local polarisation direction (15). Thus, information about the properties of the ferroelectric nano-capacitor is obtained (33,34).

The techniques used in the literature for the preparation of nano-sized ferroelectric structures on silicon based substrates are divided into the so-called (i) top-down and (ii) bottom-up methods (35,36). The top-down approach is based on lithographic techniques that have a good spatial resolution and positioning precision. Ordered arrays of ferroelectric cells are obtained easily by these methods, however the fabrication of structures with lateral sizes below 100 nm and
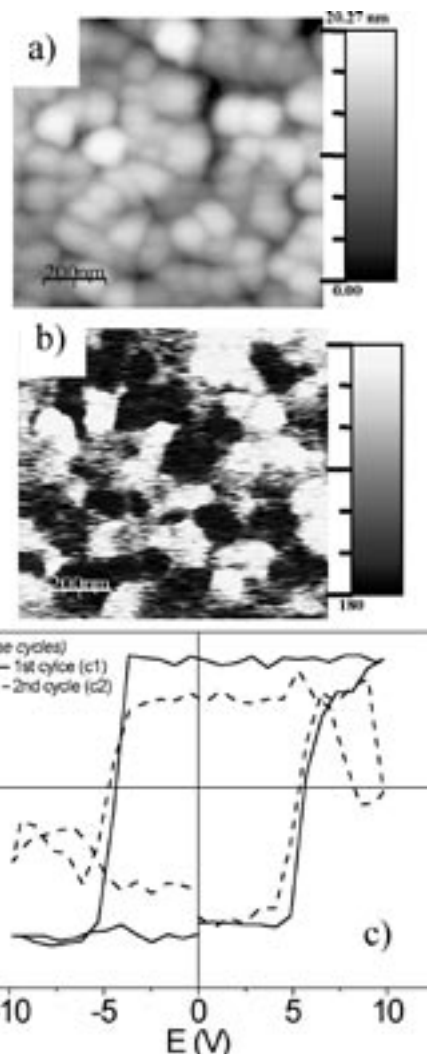

Fig. 5- PFM results. a) topographic image of PbTiO$_3$ islands onto a Pt/TiO$_2$/SiO$_2$/Si substrate. b) piezoelectric domain image of the islands and c) local piezoelectric hysteresis loops measured in one of this PbTiO$_3$ islands.
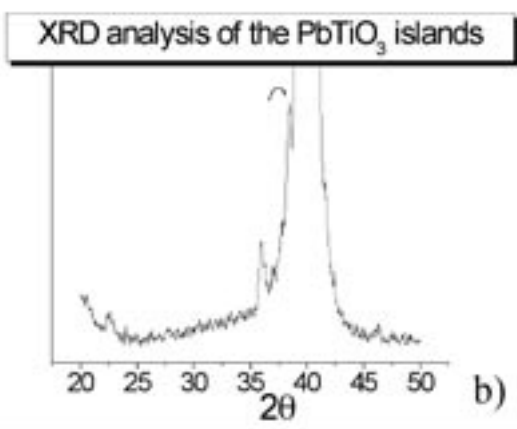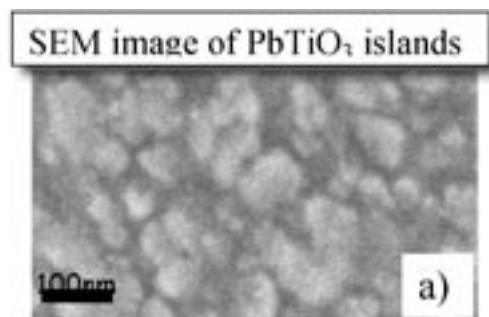

Fig. 4- a) Scanning electron microscopy image of the nanometric islands obtained onto the Pt/TiO$_2$/SiO$_2$/Si substrate after the CSD deposition of a highly-diluted PbTiO$_3$ sol-gel solution. b) X-ray diffraction pattern of the islands onto the substrate showing the peaks corresponding to the perovskite (001/100 and 111) and peaks corresponding to the Pt-bottom electrode (111 and its K$_\beta$).

with ferroelectric activity is quite difficult (32,37-38). To the authors knowledge, ferroelectric features between 70 and 100 nm with a clear piezoelectric activity have only been achieved by focused ion beam (FIB) patterning (39).

The bottom-up processes hold the promise to enable the fabrication of complex device architectures based on the intrinsic ability of the system to organise into patterns (40) in what is called sometimes self-assembly processes. They try to mimic naturally occurring processes. These are low-cost techniques that allow the relatively easy fabrication of structures with sizes ~100 nm. But, in spite of the expected self-assemblage of the structures, the major handicap of these methods is the still great difficulty for obtaining ordered arrays of structures.

For the fabrication of these nano-sized ferroelectric structures, different bottom-up methods are being tested in our laboratory. Here, preliminary results on the formation of ferroelectric nano-metric islands obtained by breaking the continuity of an ultra-thin film are shown. This method was developed in the 1990's with the objective of preparing

nanosized islands onto a single crystal substrate that serve as seeds for the epitaxial growth of films by CSD (41-43). Now, this idea is reconsidered for the fabrication of ferroelectric nano-sized cells (44,45). We have observed that the deposition of highly diluted PbTiO$_3$ solutions produces a non-continuous coating when the thickness of the deposit is below ~10nm (Fig.4a). The islands have a lateral size close to ~100nm and a perovskite structure (Fig.4b), as observed by x-ray diffraction analysis. Fig.5 shows that the nano metric islands (Fig.5a) have ferroelectric activity, as the domain image (Fig.5b) and the local piezoelectric hysteresis loop measured in one of the PbTiO$_3$ islands by PFM indicate (Fig.5c).

As mentioned before, the main disadvantage of this method of preparation is the difficulty to obtain regular patterns. Among the solutions proposed, it is the so called "lithography-modulated self-assembly" (36,46), in which we take advantage of the preferential nucleation of the ferroelectric nanostructures on a TiO$_2$ layer previously lithographically patterned. This method has been used for the preparation of ordered arrays of nanometric PbTiO$_3$ islands on a SrTiO$_3$ single crystal substrate (46) and on the conventional Si semiconductor based substrates (36). But, the major disadvantage of this method is the necessity of using an expensive lithographic technique for the fabrication of the patterned TiO$_2$ substrates. Other authors simply use monodisperse latex spheres of micron size (47) or gold nanotube membranes (48) as deposition masks with excellent results in getting patterned structures, but these cells have lateral sizes over 100nm.

Therefore, it is increasingly recognised that current technologies (lithographic based top-down methods) will not be able to scale easily to the sub-100nm level and that chemical self-assembly (bottom-up methods) will become the only economically feasible approach to the fabrication of components in this nanometer range (49). Still too much work on this thrilling area will have to be carried out in the near future.

5. SUMMARY AND OUTLOOK

- Ferroelectric oxides are being considered as alternative materials to SiO$_2$ in electronic devices. They are high-k oxides that would make possible the fabrication of thicker insulator layers than with SiO$_2$, but with a similar effective capacitance (DRAMs). Besides, ferroelectrics are multifunctional materials with a wide range of properties that can be used for the active elements in other micro/nanoelectronic devices (NVFeRAMs, pyroelectric sensors, MEMS/NEMS, ...). For the design of these devices, it is necessary their integration with the semiconductor silicon substrate. Key-points for integration is the reduction of the processing temperature of the ferroelectric films and the downscaling of the ferroelectric material.

- Chemical Solution Deposition (CSD) is a powerful technique for the fabrication of ferroelectric thin and ultrathin films, and nano-sized structures. It makes possible the tailoring of the chemistry of the precursor solutions to obtain materials with defined properties: UV light-sensitive solutions for low-temperature processing, dilution control for films with different thickness (from thin to ultrathin) or modification of the interfacial energy for the preparation of nanosized structures.

- The bottom-up approaches using CSD offer the possibility of fabrication sub-100nm ferroelectric structures, below the sizes accessible by any top-down method, at a low cost.

Although first approximations have been done, there is still much work to do in order to solve the major problem of these methods that is to obtain ordered arrays.

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