# Design Considerations for Multistandard Cascade ΣΔ Modulators

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***Abstract*— This paper discusses design considerations for cascade Sigma-Delta Modulators (ΣΔMs) included in multistandard wireless receivers. Four different standards are covered: GSM, Bluetooth, UMTS, and WLAN. A top-down design methodology is proposed to find out the optimum modulator architecture in terms of circuit complexity and reconfiguration parameters. Several reconfiguration strategies are adopted at both architecture- and circuit-level in order to adapt the modulator performance to the different standards requirements with adaptive power consumption. Time-domain behavioural simulations considering a 0.13μm CMOS implementation are shown to validate the presented approach.†**

## I. INTRODUCTION

The extraordinary growth of wireless communication technologies has prompted the emergence of multitude of new applications and standards. These new standards —like IEEE 802.11 Wireless Local Area Network (WLAN) and Universal Mobile Telecommunications System (UMTS)— are complementing rather than replacing the existing ones —such as Global System for Mobile (GSM) communication— giving rise to the so-called *universal* or *multistandard* transceivers. These systems are able to operate over a variety of specifications, thus benefiting of the different services and functions offered by co-existing wireless standards [1].

Multistandard transceivers need to be implemented by reconfigurable building blocks that can be adapted to each specification with little adjustment made to their circuit parameters and with adaptive power consumption. One of the most challenging building blocks is the Analog-to-Digital Converter (ADC), because of the different sampling rates and dynamic ranges required to digitize the wide range of signals coming from each individual operation mode [2].

Sigma-Delta Modulators (ΣΔMs) are good candidates for the implementation of the ADC in multistandard, multimode communication systems [3][4]. This type of ADCs combines redundant temporal data (*oversampling*) to reduce the quantization noise and filtering (*noise shaping*) to push this noise out of the signal band. On the one hand, the use of these characteristics results in high-performance, robust ADCs, which have lower sensitivity to circuitry imperfections than Nyquist-rate ADCs, thus making easier to include reconfigurability and programmability functions without significant performance degradation. On the other hand, ΣΔMs trade analog accuracy by signal processing, thus facilitating their integration in modern deep-submicron VLSI technologies, more suited to implement fast digital circuits than precise analog functions [5].

Several multistandard ΣΔM Integrated Circuits (ICs) have been reported up to now [6]-[10]. Most of them are based on reconfiguring architecture-level parameters (modulator order, oversampling ratio and/or number of bits of the internal quantizers), whereas less emphasis is normally put at circuit-level parameters.

This paper presents design considerations applicable to expandible cascade ΣΔMs intended for multistandard receivers, covering four standards: GSM, Bluetooth, UMTS, and WLAN, considering a 0.13-μm CMOS technology. A complete top-down design procedure is described from system-level to building-block level, putting special emphasis on optimizing the circuit design for different operation modes. To this purpose, different strategies are adopted at both architecture-level and circuit-level in order to fulfill the required specifications with minimum power consumption.

## II. MODULATOR SPECIFICATIONS

The ΣΔM in this paper has been designed to meet the requirements of Direct-Conversion Receivers (DCRs) like that shown in Fig.1. This receiver architecture is commonly used in multistandard applications because it eliminates the need for both IF and image reject filtering and requires only a single oscillator and mixer [11]. In order to cope with the requirements of the different standards, separate (switchable) RF hardware paths (normally one per standard) are used whereas a single, digitally-programmed baseband section (from the mixer to the ADC) is implemented [12].

The receiver must detect a wanted signal at the antenna in presence of strong unwanted signals (generally called *interferes*) without causing a degradation of the receiver performance. In multistandard implementations, the receiver must fulfill the performance

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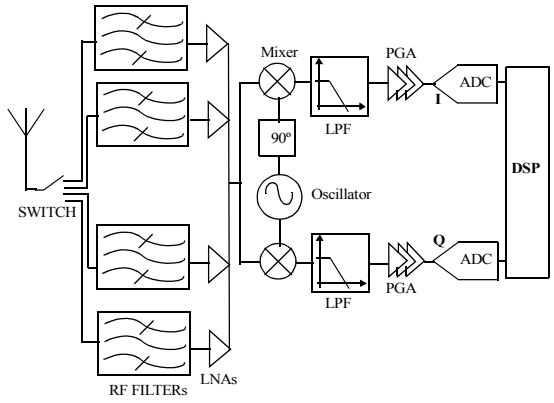


**Fig. 1:** Block diagram of a multistandard direct-conversion receiver.

requirements of each standard [1]. Unfortunately, standards do not give explicit recommendations for the physical realization of the receivers. Instead of that, a black-box approach is assumed, and a set of evaluation tests are outlined to validate the receiver performance in terms of three basic aspects: *sensitivity*, *selectivity*, and *linearity* [13]. As an illustration, Table 1 summarizes the input-referred receiver requirements from these tests for the standards covered in this paper.

Receiver requirements are mapped onto building-block specifications (gain, dynamic range, linearity, and noise figure) in an iterative synthesis process, generally referred to as *receiver planning* [13]. This process is usually accompanied by a level diagram which shows how the different signals (wanted signal and interferes) evolve along the receiver chain.

TABLE 1. Input-referred requirements for the different standards.

| | GSM | Bluetooth | UMTS | WLAN |
|---|---|---|---|---|
| Sensitivity | -102dBm | -70dBm | -117dBm | -65dBm |
| Max. signal | -15dBm | -20dBm | -25dBm | -30dBm |
| Bandwidth | 200kHz | 1MHz | 3.84MHz | 20MHz |
| Interferer level | -49dBm | -39dBm | -46dBm | -45dBm |
| Max. out-band blocker | 0dBm | -10dBm | -15dBm | 0dBm |
| Max. in-band blocker | -23dBm | --- | -44dBm | -30dBm |
| Max. adjacent channel | -33dBm | -27dBm | -92.7dBm | -65dBm |

In this paper, a simulation-based approach has been adopted for the receiver planning. To this purpose, the receiver front-end building blocks have been modeled using MATLAB/SIMULINK [14] as illustrated in Fig.2. Behavioral models of building blocks include the following design parameters:

- Operating frequency and bandwidth.
- Amplification within the passband of the block.
- Noise figure, represented as *NF*.
- Nonlinearity, commonly expressed by the input-referred 2nd- and 3rd-order intercept points.

In addition to these general parameters, some specific parameters have been also included, like for instance, oscillator phase noise and mixer offset.

A complete receiver planning in which every building-block specification is a design parameter is beyond the scope of this work. Instead, fixed specifications extracted from reported radio receivers [15][16] were considered and the ADC effective resolution was extracted from an iterative simulation-based procedure considering the propagation of the different standard test signals through the receiver front-end. The outcome is shown in Table 2, which lists the ADC specifications for the different standards covered in this paper. In addition to the resolution, the required bandwidth is determined from the channel bandwidth for each standard. As an illustration, Fig. 3 shows the level diagram for WLAN and depicts the propagation of the maximum and minimum signal (*sensitivity*) levels ($Smax$ and $Smin$, respectively) from the antenna to the ADC input, together with that of noise and distortion. Note that the Signal-to-(Noise+Distortion)-Ratio ($SNDR$) peak at the ADC input is measured as the difference of $Smax$ to the noise plus distortion. The test recommended by the standard with maximum spurious signals is also

TABLE 2. ADC specifications.

| | GSM | Bluetooth | UMTS | WLAN |
|---|---|---|---|---|
| Resolution | 13bit | 11bit | 9bit | 7bit |
| Bandwidth | 200kHz | 1MHz | 3.84MHz | 20MHz |

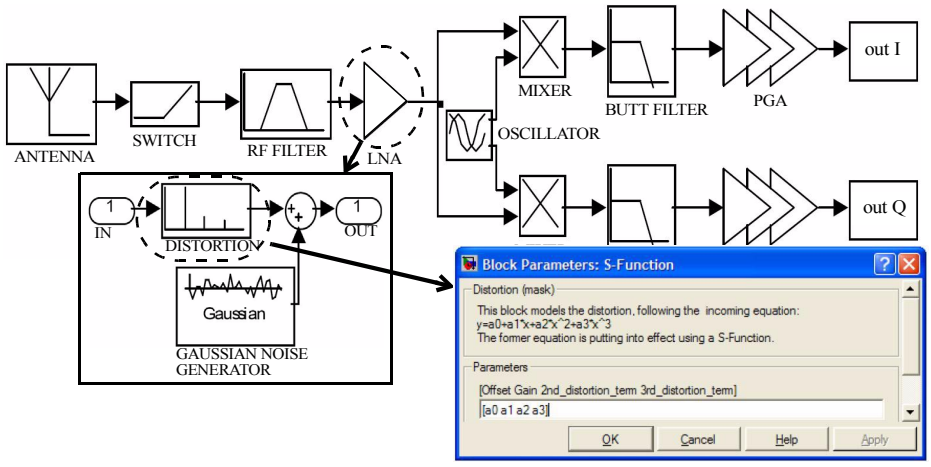


**Fig. 2:** Illustrating the behavioral model of the DCR in SIMULINK.

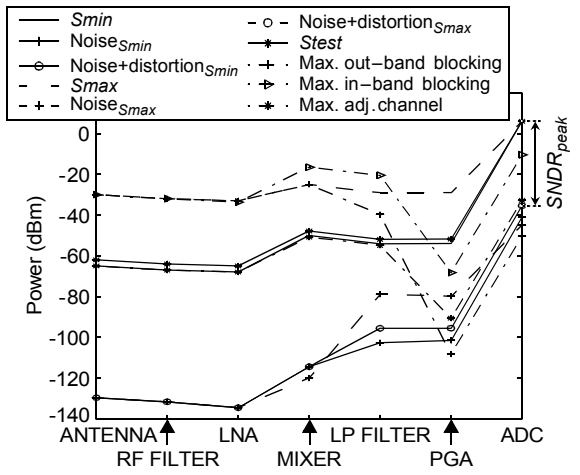


**Fig. 3:** Level diagram for WLAN.

included, with $Stest$ being the wanted signal level.

The specifications in Table 2 are the starting point for the modulator high-level synthesis, detailed below.

## III. ARCHITECTURE SELECTION

### *A. Expandible modulator architecture*

Given that reconfigurability issues must be boosted in the targeted multistandard application, the expandible cascade ΣΔM in Fig.4*a* [17] has been selected as the best suited architecture. This cascade topology comprises a 2nd-order first stage followed by 1st-order stages, and can be easily extended to build a ΣΔM of a generic order $L$ by simply adjusting the number of 1st-order stages. Note that the selected architecture can exploit the benefits of an unconditionally stable high-order shaping thanks to the cascade structure and a robust, linear multibit quantization by incorporating it only in the modulator last stage [18].

Fig.4*a* depicts the selected set of integrator weights and the required digital cancellation logic in this architecture, henceforth called 2-1$^{L-2}$ ΣΔM. Altogether, the main advantages are [17]:

- The systematic loss of resolution that is typically present in every cascade ΣΔM in comparison with an ideal $L$-th order loop is only 6dB.
- The modulator overload level remains constant at −5dBFS, regardless the order of the expandible cascade. This feature is illustrated in Fig.4*b*.
- The output swing required in the integrators is only the modulator reference voltage ($\pm V_{ref}$).
- The weights in the 1st-order stages can be distributed into only two SC branches. Also those in the second integrator can be distributed. The total number of unit capacitors is thus reduced to only $2 \times [5 + 4(L-1)]$, what benefits area occupation, thermal noise, and amplifier dynamics.
- All 1st-order stages contain the same weights, so that they can be electrically identical ††. This can considerably simplify the electrical and physical implementation of the modulator.

### *B. Exploration of cascade candidates*

Note that every cascade ΣΔM belonging to the family in Fig.4*a* can be univocally described by three parameters: the modulator order ($L$), the oversampling ratio ($OSR$), and the number of bits in the last stage ($B$). Thus, a $\{L, B, OSR\}$ triad is used to codify them.

The first step in the design of the multistandard ΣΔM is the exploration of the $\{L, B, OSR\}$ candidates for each standard that achieve minimum power consumption while fulfilling its corresponding requirements. At this step, an updated version of the analytical procedure described in [17] to estimate the power consumption of 2-1$^{L-2}$ ΣΔMs has been followed. The procedure, based on compact expressions that contemplate both architectural and technological features, schematically consists of the following steps:

1) The in-band quantization error power ($P_Q$) is calculated for given values of $\{L, B, OSR\}$ and $V_{ref}$. Noise leakages due to capacitor mismatch, finite amplifier DC gain, and errors in the multibit quantizer (if $B > 1$) are also contemplated.
2) The in-band error power due to circuit noise ($P_{CN}$) is considered. The value of the sampling

††. If multibit quantization is used in the modulator last stage, its weights are usually doubled to easy the implementation of the corresponding ADC and DAC. This issue, together with the larger integrator load due to the ADC, normally prevents from using the same electrical design.

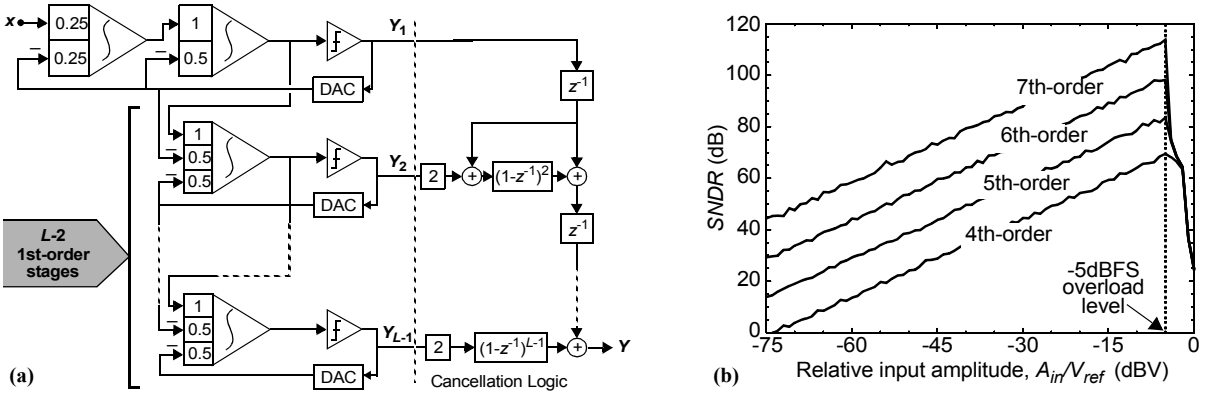


**Fig. 4:** 2-1$^{L-2}$ cascade ΣΔM: (a) Block diagram; (b) Illustration of the constant overload level ($SNDR$ curves for $OSR$ = 16).

capacitor at the modulator front-end ($C_S$) is selected so that $P_Q + P_{CN}$ is smaller than the maximum allowed total in-band error power. $P_{CN}$ will be mainly contributed by $kT/C$ noise, but some room is left at this step for the contribution of the front-end amplifier noise.

3) The amplifier Gain-Bandwidth product ($GB$) is estimated so that the in-band error power due to the integrator defective settling ($P_{st}$) is non-limiting ($P_{st} \ll P_Q + P_{CN}$). A linear settling model is used, considering that it takes a number $\ln(2^{ENOB})$ of time constants to settle within $ENOB$ resolution.
4) The amplifier $GB$ is related to its power dissipation, for which the amplifier topology must be known a priori. Suitable candidates are closely related to the process technology: supply voltage, minimal device length, etc. Usual choices are folded cascodes for supplies above 3V (like in our case) or two-stage amplifiers below 2.5V [19].
5) Once the power dissipation of the front-end integrator has been estimated, that of the remaining ones (with, in practice, less demanding specifications) is estimated as a fraction of it. The overall estimated modulator power is then basically obtained by adding up all contributions, together with the dynamic power in the SC stages.

Given the targeted multistandard application, the design space has been explored in terms of suitable $\{L, B, OSR\}$ triads for each standard by applying the former procedure under the next global constraints:

- The modulator reference is fixed to 1.2V in order to place the input signal level at –5.6dBFS and maximize the $SNDR$ (see Fig.4*b*).
- The explored values of $L$ are restricted to 2, 3, and 4. Given the targeted range of resolutions ($\leq$ 13bit), ΣΔMs with $L \geq 5$ are not considered.
- The sampling frequency ($f_s$) is restricted to values $\div 1$, $\div 2$, $\div 4$, etc., from a maximum of 160MHz, in order to easy the frequency division of a master clock frequency from one standard to another. This imposes a constraint on the practical $OSR$ values that are explored and forces to expand the bandwidth in WLAN from 3.84MHz to 4MHz.
- The smallest value for the unit capacitor ($C_u$) is fixed to 0.25pF for mismatching issues.
- In order to easy the circuit reconfiguration, the sampling capacitor at the modulator front-end can only take values that are multiple of $C_u$.

Table 3 summarizes the ranking of ΣΔMs with the lowest estimated power for each standard. Together with the values for $\{L, B, OSR\}$, those required for $f_s$ and $C_S$, and the obtained Dynamic Range ($DR$) and $SNDR$ peak are also enclosed for comparison purposes. The highlighted rows in Table 3 correspond to the ΣΔMs for each standard that we have selected for further consideration. Note that the rest of candidates

TABLE 3. Ranking of ΣΔMs according to their estimated power.

| Standard | $L$ | $B$ | $OSR$ | $f_s$ (MHz) | $C_S$ (pF) | $DR$ (bit) | $SNDR_{peak}$ (bit) | Power (mW) |
|---|---|---|---|---|---|---|---|---|
| GSM | 4 | 1 | 50 | 20 | 0.50 | 14.42 | 13.59 | 10.9 |
| | 3 | 2 | 50 | 20 | 0.50 | 14.39 | 13.56 | 11.7 |
| | 3 | 3 | 50 | 20 | 0.50 | 14.41 | 13.58 | 12.5 |
| | 4 | 2 | 50 | 20 | 0.50 | 14.42 | 13.59 | 13.4 |
| | 3 | 4 | 50 | 20 | 0.50 | 14.41 | 13.58 | 14.1 |
| | 4 | 3 | 50 | 20 | 0.50 | 14.42 | 13.59 | 14.2 |
| | 4 | 4 | 50 | 20 | 0.50 | 14.42 | 13.59 | 15.8 |
| | 3 | 1 | 100 | 40 | 0.25 | 14.42 | 13.59 | 17.0 |
| | 4 | 1 | 100 | 40 | 0.25 | 14.42 | 13.59 | 20.0 |
| Bluetooth | 4 | 1 | 20 | 40 | 0.25 | 12.82 | 11.99 | 18.1 |
| | 3 | 3 | 20 | 40 | 0.25 | 12.76 | 11.93 | 20.6 |
| | 3 | 4 | 20 | 40 | 0.25 | 13.05 | 12.22 | 22.5 |
| | 4 | 2 | 20 | 40 | 0.25 | 13.16 | 12.33 | 23.0 |
| | 4 | 3 | 20 | 40 | 0.25 | 13.21 | 12.38 | 23.9 |
| | 4 | 4 | 20 | 40 | 0.25 | 13.22 | 12.39 | 25.5 |
| | 3 | 1 | 40 | 80 | 0.25 | 13.40 | 12.57 | 32.1 |
| UMTS | 3 | 4 | 10 | 80 | 0.25 | 10.81 | 9.98 | 37.3 |
| | 4 | 2 | 10 | 80 | 0.25 | 10.45 | 9.62 | 38.6 |
| | 4 | 3 | 10 | 80 | 0.25 | 11.46 | 10.63 | 42.0 |
| WLAN | 3 | 6 | 4 | 160 | 0.25 | 8.12 | 7.29 | 70.9 |
| | 4 | 6 | 4 | 160 | 0.25 | 8.57 | 7.74 | 80.8 |

are directly covered by the selected ones, since the former just imply an increase of the modulator order or of the internal multibit resolution. Thus, the selected ΣΔMs at this step globally comprise:

- 3rd- and 4th-order cascades.
- Single-bit quantization and multibit quantization of 2, 3, 4, or 6 bits.
- Sampling frequencies of 20MHz, 40MHz, 80MHz, or 160MHz.
- Sampling capacitors of 0.25pF or 0.5pF.

The former issues can be handled at circuit level, by reconfiguring the last stage of the expandible cascade to either single-bit or multibit with programmable resolution, by dividing the master clock frequency by a factor 2, 4, or 8, and by using switchable capacitors at the modulator front-end, respectively.

Seeking for a single circuit that covers all the former possibilities can a priori be done, but such a large degree of freedom in the reconfigurability will considerably increase the circuit complexity. Thus, only one $\{L, B, OSR\}$ triad will definitively be selected for each standard. However, given that the estimated power consumptions are not very different from one case to another, the final decision will be taken after extracting their complete set of building-block requirements using more accurate behavioral simulations.

## IV. HIGH-LEVEL SYNTHESIS

### *A. Design methodology*

The formerly selected candidates (3 architectures for GSM and 2 for Bluetooth, UMTS, and WLAN) have been extensively simulated using SIMSIDES

[20], a time-domain simulator for ΣΔ modulators that includes accurate behavioral models for thermal noise, integrator defective settling, distortion sources, etc. This way the architecture specifications can be mapped onto more refined building-block requirements in terms of amplifier DC gain, $GB$, Slew Rate ($SR$), equivalent input noise, switch on-resistance, etc.

The followed steps for this process are:

1) Validate that the ΣΔMs selected from Table 3 achieve the required $DR$ for each standard, taking into account quantization error and $kT/C$ noise.
2) Determine the maximum equivalent input noise for each amplifier that does not degrade the formerly achieved performance.
3) Determine the required amplifier dynamics ($GB$ and $SR$), taking into account settling errors during both the integration and sampling phases [21].
4) Refine the DC gain and $SR$ requirements at each front-end integrator in order to limit the generated distortion near the modulator overload level.

At this step different amplifiers are considered for each integrator in order to gain insight on their individual needs. Once the final architecture is selected for each standard, the global amplifier specifications will be tried to be covered using reconfigurable amplifiers (in terms of bias currents and/or transistor sizings).

However, switches will not be reconfigured from one standard to another, so that they must be sized at this step taking into account their slow-down effect on the integrators dynamics [22] and the dynamic distortion they introduce at the modulator front-end [23]. They have been sized to exhibit a maximum on-resistance around $250\Omega$, which does not to compromise settling nor distortion in the different standards and avoids the use of clock-boosting techniques.

### *B. Building-block specifications*

The requirements of the selected ΣΔMs after the former fine-tuning process are summarized in Table 4, in terms of the amplifier equivalent input noise, DC gain, and dynamics for each integrator.

## V. SIMULATION RESULTS

As shown in Fig.5, the modulator sizings in Table 4 achieve the specifications of the different standards. The figure depicts the $SNDR$ curves obtained by behavioral simulation and shows that the ΣΔMs exhibit an $SNDR$ peak larger than 81dB for GSM, 71dB for Bluetooth, 58dB for UMTS, and 44dB for WLAN.

Based on the results shown in Table 4, especially on those related to the amplifier dynamics, the final selection of the ΣΔM architecture for each standard is:

TABLE 4. Amplifier requirements after fine tuning of the different $\{L, B, OSR\}$ candidates.

| Standard | {*L*, *B*, *OSR*} | Integrator | Amplifier input noise ($nV/\sqrt{Hz}$) | Amplifier DC gain | Transconductance (mA/V) | Output current (μA) | Equivalent capacitive load (pF) | *GB* (MHz) | *SR* (V/μs) |
|---|---|---|---|---|---|---|---|---|---|
| GSM | {3, 1, 100} | #1 | 7.0 | 1500 | 0.26 | 150 | 3.51 | 11.9 | 55.1 |
| | | #2 | 135.0 | 250 | 0.42 | 130 | 5.67 | 11.7 | 47.0 |
| | | #3 | 237.5 | 250 | 0.19 | 60 | 5.67 | 5.4 | 21.7 |
| | {3, 2, 50} | #1 | 6.0 | 700 | 0.42 | 200 | 3.70 | 18.1 | 68.1 |
| | | #2 | 32.5 | 400 | 0.62 | 130 | 5.67 | 17.3 | 47.0 |
| | | #3 | 225.0 | 250 | 0.23 | 130 | 16.03 | 2.3 | 25.1 |
| | {4, 1, 50} | #1 | 6.0 | 800 | 0.39 | 200 | 3.71 | 16.7 | 67.9 |
| | | #2 | 12.5 | 250 | 0.86 | 120 | 5.67 | 24.2 | 43.4 |
| | | #3 | 125.0 | 250 | 0.25 | 170 | 5.67 | 7.1 | 61.5 |
| | | #4 | 212.5 | 250 | 0.23 | 50 | 5.67 | 6.5 | 18.1 |
| Bluetooth | {3, 3, 20} | #1 | 8.0 | 2000 | 1.36 | 240 | 3.51 | 61.8 | 88.2 |
| | | #2 | 26.0 | 550 | 2.52 | 300 | 5.67 | 70.8 | 108.5 |
| | | #3 | 49.0 | 350 | 4.04 | 1000 | 16.03 | 40.1 | 193.4 |
| | {4, 1, 20} | #1 | 7.0 | 2000 | 1.25 | 320 | 3.51 | 56.8 | 117.6 |
| | | #2 | 12.0 | 350 | 2.52 | 300 | 5.67 | 70.8 | 108.5 |
| | | #3 | 19.0 | 400 | 1.19 | 750 | 5.67 | 33.4 | 271.2 |
| | | #4 | 40.0 | 300 | 0.46 | 375 | 5.67 | 12.9 | 135.6 |
| UMTS | {3, 4, 10} | #1 | 18.0 | 2500 | 2.39 | 413 | 3.53 | 107.6 | 150.9 |
| | | #2 | 12.0 | 500 | 6.40 | 800 | 5.70 | 178.8 | 289.1 |
| | | #3 | 35.0 | 400 | 13.26 | 2550 | 16.15 | 130.7 | 492.6 |
| | {4, 2, 10} | #1 | 11.0 | 1800 | 2.62 | 506 | 3.53 | 118.3 | 184.9 |
| | | #2 | 18.0 | 400 | 6.19 | 750 | 5.70 | 172.9 | 271.1 |
| | | #3 | 45.0 | 450 | 8.14 | 1000 | 5.70 | 227.4 | 361.4 |
| | | #4 | 35.0 | 450 | 6.61 | 1000 | 16.15 | 65.2 | 193.2 |
| WLAN | {3, 6, 4} | #1 | 45.0 | 1000 | 8.78 | 750 | 3.65 | 382.8 | 271.2 |
| | | #2 | 30.0 | 1375 | 21.50 | 1700 | 5.90 | 579.9 | 610.9 |
| | | #3 | 22.5 | 675 | 28.45 | 7000 | 16.83 | 269.1 | 1351.8 |
| | {4, 6, 4} | #1 | 45.0 | 1500 | 8.77 | 825 | 3.67 | 380.1 | 299.0 |
| | | #2 | 17.0 | 1000 | 24.29 | 1600 | 5.93 | 651.8 | 577.4 |
| | | #3 | 20.0 | 525 | 17.29 | 2750 | 5.93 | 464.0 | 992.4 |
| | | #4 | 47.5 | 650 | 19.26 | 3150 | 16.95 | 180.9 | 607.7 |

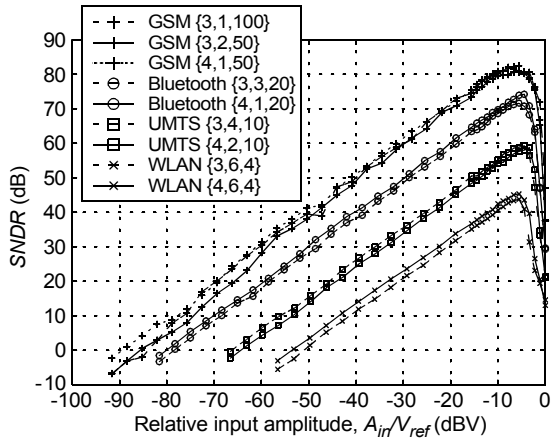


**Fig. 5:** *SNDR* curves obtained by behavioral simulation after the fine tuning of the building-block specifications.

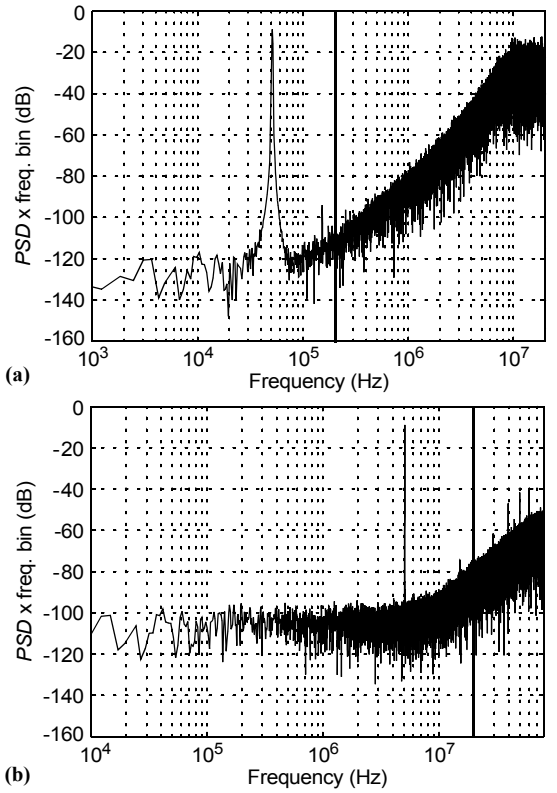


**Fig. 6:** Modulator output spectra obtained by behavioral simulation for: (a) GSM; (b) WLAN.

- For GSM: {3, 1, 100}
- For Bluetooth: {4, 1, 20}
- For UMTS: {4, 2, 10}
- For WLAN: {3, 6, 4}

The selected $\{L, B, OSR\}$ triads have also the advantage of requiring the same sampling capacitor (0.25pF —see Table 3), thus eliminating the need for switchable capacitor arrays at the modulator front-end.

Fig.6 shows the modulator output spectra obtained by behavioral simulation for GSM and WLAN.

## CONCLUSIONS

A design methodology for the design of multistandard cascade ΣΔ modulators has been described. Both architecture and circuit-level reconfiguration strategies have been considered in order to find out the optimum architecture in terms of power dissipation and silicon area. As an application of the proposed methodology, the high-level design of a 0.13-$\mu$m CMOS cascade ΣΔ modulator has been presented to cope with the requirements of several wireless standards.

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