

# A 0.13 $\mu\text{m}$ CMOS Current Steering D/A Converter for PLC and VDSL Applications

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**Abstract** – This paper describes the design of a 12-bit 80MS/s Digital-to-Analog converter implemented in a 0.13 $\mu\text{m}$  CMOS logic technology. The design has been computer-aided by a developed toolbox for the simulation and verification of Nyquist-Rate Analog-to-Digital and Digital-to-Analog converters in MATLAB. The converter is segmented in an unary current-cell matrix for 8 MSB's and a binary-weighted array for 4 LSB's. Current sources of the converter are laid out separately from current-cell switching matrix core block and distributed in double centroid to reduce random errors and transient noise coupling. The linearity errors caused by remaining gradient errors are reduced by a modified  $Q^2$  Random-Walk switching sequence. Transistor-level simulation results show that the Spurious-Free Dynamic-Range is better than 58.5dB up to 80MS/s. The estimated Signal-to-Noise Distortion Ratio yield is 99.7% and better than 58dB from DC to Nyquist frequency. Multi-Tone Power Ratio is higher than 59dB for several DMT test signals. The converter dissipates less than 129mW from a 3.3V supply and occupies less than 1.7mm<sup>2</sup> active area.

**Keywords:** digital-to-analog converters, current source, segmentation, switching sequence.

## I. INTRODUCTION

The trend to reduce the cost of market communication devices has motivated the interest for embedded high-speed high-resolution Digital-to-Analog Converters (DAC's). These converters are essential components of modern applications such as video signal processing, digital signal synthesis, and both broadband and wireless communications. Of several architecture alternatives, CMOS current steering DAC's have demonstrated to be an attractive solution for these applications [1][2][3] because of two reasons mainly: (a) they can be implemented in adverse digital CMOS technology with evident power consumption and integrability advantages and (b) they are intrinsically faster and more linear than their counterparts-based on resistors or capacitors ladders [4]. However, the combination of high data conversion rate, accuracy and linearity is difficult to achieve. In this paper, dynamic and static limitations for the circuit linearity have been investigated, resulting in the presented DAC and in the development of a behavioural simulator which has aided in its design. Details about this behavioural sim-

ulator are beyond of scope of this paper, but more information can be found in [5].

The paper is organized as followed. In Section II, the D/A converter architecture as well as the main design trade-offs are discussed. In Section III, the basic building blocks are presented, namely the current cell, the driver, the level-shifter, the latch and the thermometer decoder. Layout issues are explained in Section IV. Finally, transistor-level simulation results are shown in Section V.

## II. D/A ARCHITECTURE

The basic block diagram of a segmented current steering DAC is shown in Fig.1, where the input  $N$ -bit are split in  $b$  Least Significant Bits (LSB's), which steer a binary weighted array of current sources -binary segment-, and  $t = N - b$  Most Significant Bits (MSB's), which are thermometer-wise decoded to steer an unary array of current sources -thermometer segment. The current sources are commuted on/off by means of complementary switches which are synchronized and biased by latches and drivers circuits, respectively.

In this block diagram it can be distinguished three high-level important factors: the segmentation, i.e. the number of thermometer ( $t$ ) and binary ( $b$ ) bits, the switching scheme, that is, the sequence in which the

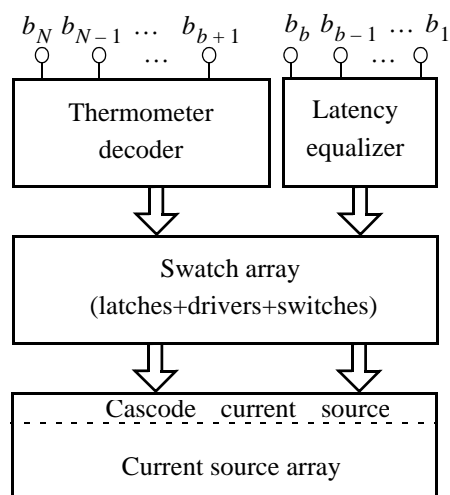


Fig. 1: Block diagram of a segmented current steering DAC.

thermometer current sources are activated and the topology of the current cell. Next subsections will focus in these issues.

#### A. Segmentation.

It is a crucial parameter because there is a direct trade-off between the DAC linearity, area, Total Harmonic Distortion (*THD*), glitch energy and the segmentation level as shown in [6]. In particular, the Integral Non-Linearity (*INL*) and Differential Non-Linearity (*DNL*) DAC depends on the segmentation as follows [7]:

$$\sigma_{DNL_{max}} = \sqrt{2^{b+1} - 1} \frac{\sigma_{i_{LSB}}}{i_{LSB}} \quad \text{in LSB units} \quad (1)$$

$$\sigma_{INL_{max}} = \sqrt{2^N - 1} \frac{\sigma_{i_{LSB}}}{i_{LSB}} \quad \text{in LSB units}$$

where  $i_{LSB}$  is the current of the LSB current cell, i.e. the ratio between the full-scale current ( $I_{FS}$ ) and the total number of current cells ( $i_{LSB} = I_{FS}/2^N$ ) and  $\sigma_{i_{LSB}}$  its standard deviation. From (1) it can be deduced that, although *INL* is independent of the segmentation, the more binary ( $b$ ) bits are employed the higher *DNL* will be. Analogously, *THD* and glitch energy increases too. Therefore, it is advisable to use the maximum number of thermometer bits. However, the area increases seriously when a high number of thermometer bits is selected. From [6][7][8] it can be concluded that an optimum segmentation for a 12-bit current steering DAC is 8 thermometer bits and 4 binary bits. This has been the adopted solution in this paper.

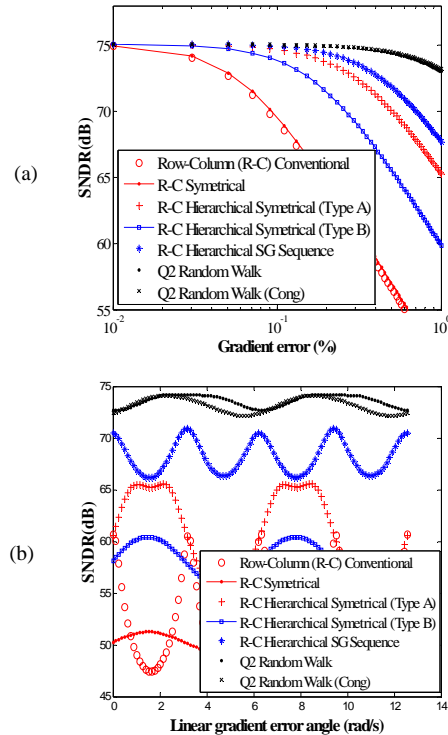
#### B. Switching scheme.

The static performance of a current steering DAC is limited by random and systematic errors. The former are caused by device mismatches and can only be palliated by increasing the active area of each current cell [9]. The latter came from thermal gradients, CMOS technology-related error components (doping gradients, oxide thickness gradients, etc...), edge effects, etc., and they can be reduced by selecting an appropriate switching sequence and/or splitting the unary current cell. Next, these techniques are detailed:

- *Splitting*. An unary current source consists of one or more parallel LSB current sources. By splitting the unary current sources and spreading them across the current-source array, the systematic errors are averaged. Splitting unary current sources is necessary for high-accuracy applications but it can result in a complex layout routing. In this current steering DAC design, each unary current source consists of 16 LSB current sources so, for the specifications required, the unary current sources have been split into 4 sub-current sources consisting of 4 LSB current sources each one and have been spread out in 4 equal quadrants in

the layout as will be shown later.

- *Switching sequence*, i.e., the sequence in which the different current sources are switched on/off in the unary current source array. An elaborated overview of different switching sequences is given in [10] and it is beyond the scope of this paper. The objective of the switching sequences is to compensate for gradient errors in the unary array of the DAC, both linear and quadratic gradients. These gradients can become very significant when the unary array active area is large, which is common in high-accuracy applications where random errors of current sources are reduced at expense of increasing the active area of each current source. Therefore, an optimum switching sequence has to be selected, so an extensive exploration of several switching sequences has been done with the aid of a dedicated behavioural simulator. In order to find out which of the switching sequences is the most appropriate, an unary current source array was defined by considering the effect of gradient errors and several switching sequences were applied. The result of this analysis can be summarized in Fig.2, where  $Q^2$  Random Walk and  $Q^2$  Random Walk (Cong) turn out to be the best switching sequences since they tolerate high gradient errors. Moreover, these switching sequences present minimum resolution deviations against the linear gradient error angle ( $\theta$ ). Although all  $Q^2$  switching sequences show good properties, we choose  $Q^2$  Random Walk (Cong) sequence because it presents light advantages as shown in [10].



**Fig. 2:** Signal-to-Noise Distortion Ratio (*SNDR*) degradation vs (a) gradient errors and (b) linear gradient error angle in the unary current source array.

### C. Topology of the current cell.

The simplest topology implementing the current cell consists of a single MOS transistor biased with constant gate-source voltage and operating in saturation. The switching is performed by means of MOS transistors operating as switches with complementary activation gate signals. This topology is illustrated in Fig.3(a). Its main disadvantage lies in that the output impedance obtained is not enough for high performance applications. In fact, the finite output impedance can become an important limitation for the Spurious Free Dynamic Range (*SFDR*) as shown in [11]. Therefore, this topology is not appropriate for this application even although the switches were biased to operate in saturation in order to increase the output impedance.

An alternative to the simple current cell is the cascode current cell showed in Fig.3(b). This circuit exhibits the output resistance of a double-cascode structure when the switches operate in saturation which is enough for low-distortion applications. This has been the topology employed in our current steering DAC. In addition, p-MOS transistors have been used because they are more robust against noise substrate. Details about the design issues will be discussed in next section.

### III. BUILDING BLOCKS DESIGN

The basic building blocks in a segmented current steering DAC can be identified in the block diagram in Fig.1, i.e., the current cell, the driver circuit, the latch and level shifter, the thermometer decoder and other auxiliary blocks such as internal voltage generators and current reference generators. Next, a detailed description of these circuits is given.

#### A. Current cell.

As shown in previous section, in order to minimize random errors, a minimum area is required for the transistor which operates as current source (*Mcs*) so the impact of the relative standard deviation of current over the static performance was neglected. The tolerable relative standard deviation can be calculated from yield simulations as shown in Fig.4(a). This figure has

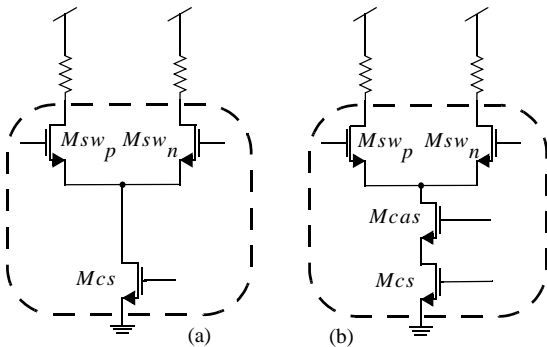


Fig. 3: Basic current cell topologies: (a) single and (b) cascode.

been obtained with the behavioural simulator and it represents the parametric yield as a function of the relative standard deviation of the current cells. A *SNDR* higher than 72dB has been considered as proper operation criterion. If 99.5% yield has to be guaranteed it is immediate to derive the required precision for the current cell, that is,  $(\sigma_{i_{LSB}}/i_{LSB}) < 0.3\%$ . Based on the mismatch statistical model[9], an expression can be derived for the gate-area  $(WL)_{min}$  of the unit current source transistor to satisfy previous condition:

$$(WL)_{min} = \left( A_{\beta}^2 + \frac{4A_{V_T}^2}{(V_{gs} - V_{th})^2} \right) / (\sigma_{i_{LSB}}/i_{LSB})^2 \quad (2)$$

where  $A_{V_T}$  and  $A_{\beta}$  are mismatch technology parameters and  $(V_{gs} - V_{th})$  is the gate overdrive voltage of the current source. On the other hand, the full scale current defines the  $i_{LSB} = I_{FS}/2^N$  and set another condition over the  $(W/L)$  ratio of the current source:

$$i_{LSB} = \frac{1}{2} \mu_o C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \quad (3)$$

Finally, only the gate overdrive voltage is a freedom degree. From (2) it can be deduced that by increasing the  $(V_{gs} - V_{th})$ , the minimum area required can be decreased. For very large values, however, the mismatch is mainly determined by the  $A_{\beta}$  term. A convenient criterion to determine the gate overdrive voltage of the current source will be that one which minimizes systematic errors. Of several systematic errors, the effects which contribute in most extent are the finite output impedance and others ones which are

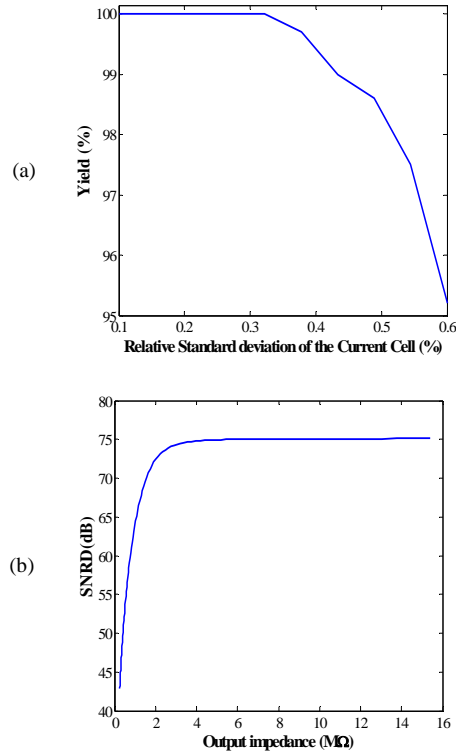


Fig. 4: Current cell sizing: (a) Yield as function of relative standard deviation and (b) minimum output impedance required.

layout-determined and are minimized by optimizing the switching scheme and by careful layout generation. In order to minimize the effect of the finite output impedance, the topology selected for the current cell was the cascode configuration as described in C.. The tolerable minimum output impedance can be calculated from the parametric analysis in Fig.4(b). To guarantee a  $SNDR > 72\text{dB}$  an output impedance higher than  $3\text{M}\Omega$  from DC to Nyquist-frequency is needed.

Taking into account the above-mentioned issues, the electrical-level sizing of the cascode current cell in Fig.3(b) was carried out by combining an statistical optimizer with an electrical simulator, considering the following constraints:

- Minimize area of the switches and the cascode transistor.
- All transistors must operate in saturation region.
- Maximize output impedance.
- Guarantee a good settling time.

The sizing of the current cell, both at high-level and electrical-level, is summarized in Table 1.

### B. Driver.

Transistors  $M_{swp}$  and  $M_{swn}$  in Fig.1 are operating as switches with complementary activation gate signals. These signals are provided by driver circuit and they must be properly generated in order to minimize two important effects which can cause glitches at the output of the converter: (a) drain voltage variations of the current-source transistor and (b) coupling of the control signal through the gate to drain capacitance of the switches to the output.

The objective is to prevent both switch transistors from being off during some period of time. In that case, the current source will make its drain node voltage to vary, producing a glitch at the output. To reduce these glitches the two complementary gate voltage waveforms must be generated in such a way that when one of the two switch transistors is turned off the other is completely turned on. Thus, the two complementary signals which control the switch operation must have a non-symmetrical crossover.

TABLE 1. Sizing of the current cell

High-level sizing		Electrical-level sizing	
Relative current standard deviation	<0.3%	$(W/L)_{cs}$	20/7.5
		$(W/L)_{cas}$	9.65/0.5
Finite output impedance (from DC to Nyquist)	> $3\text{M}\Omega$	$(W/L)_{sw}$	0.63/0.5
		$(V_{sg} - V_{th})_{cs}$	1.2V
Topology of the current cell	Cascode	DC output impedance	$139\text{G}\Omega$
Maximum gradient error	0.8%	Output impedance at 34 MHz	$10.7\text{M}\Omega$
Switching sequence	$\text{Q}^2$ Random Walk (Cong)	Switch on voltage	0.9V

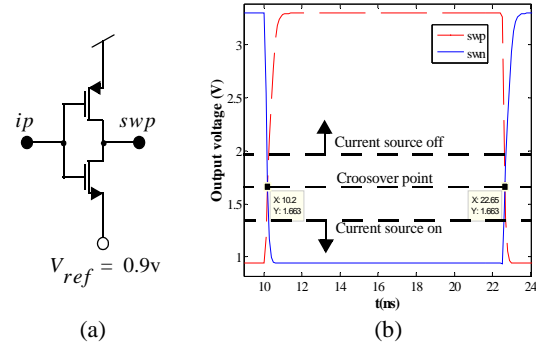


Fig. 5: Driver: (a) circuit implementation and (b) transient responses

The circuit selected to carry out this function is presented in Fig.5(a). It is an inverter supplied by the voltages which turns on ( $V_{ref} = 0.9\text{v}$ ) and off ( $V_{dd} = 3.3\text{v}$ ) switch transistors in the current cell. The transient response of the driver circuit is plotted in Fig.5(b) where it can be observed that the crossover point is under the middle of supply voltages. Besides, it has been tried to minimize the area of the transistors in order to reduce the coupling of the control signals to the output.

### C. Level shifter and latch.

The input bits to the current steering DAC are processed by digital logic circuits. These circuits are supplied by different voltages to analog circuits so that a level conversion is required. This function can be carried out by the level shifter circuit shown in Fig.6(a). In particular, this circuit must shift voltage levels from 0-1.2V to 0-3.3V.

On the other hand, the signals from the level shifter must be synchronized and shaped in order to improve the dynamic performance[8]. To do this, two latches are inserted between the level shifter and the driver. The first one is active at high level and captures the output of the level shifter while the clock signal was “high”. The second one is active at low level and provides its output to the driver when the clock signal is “low”. Note that at that moment all outputs of the digital decoder (a combinational circuit) must be established. The schematic of the latch topology used is illustrated in Fig.6(b).

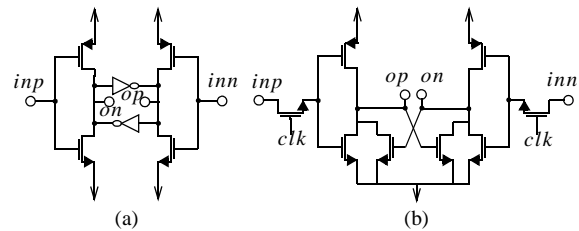


Fig. 6: Circuit implementation: (a) level shifter and (b) latch.

#### D. Thermometer decoder.

Some of the input bits are thermometer-wise decoded to steer unary current sources and the remaining input bits are delayed by an equalizer block to have the same overall delay such as illustrated in Fig.1. The thermometer decoder has been synthesized using commercial synthesis tools from a VHDL functional description based on the decoder presented in [12]. So, an efficient synthesis is achieved because the complexity is substantially reduced.

#### IV. LAYOUT ISSUES

The layout of the current steering DAC is shown in Fig.7 and it has been designed using a  $0.13\mu\text{m}$  CMOS process with 1 poly and 8 metal layers. The power supply is 3.3V and has a full scale current of 20mA over  $25\Omega$  loads. It occupies an active area of  $1.78 \times 0.96 \text{ mm}^2$ .

The decoder was placed on the top, far away and well shielded from the sensitive analog parts. The swatch array, consisting of switch transistors, latches, level shifters and drivers are placed below the decoder; in a separated array from the current sources. This is done to avoid coupling between the digital and analog parts. Besides, in this way, the layout area of the current source array is minimized and, therefore, the systematic errors are reduced.

The unary current source array consist of 255 unary current sources. Each unary current source consists of 16 parallel PMOS transistors which is split in 4 sub-current sources consisting of 4 PMOS transistors each one and have been spread out in 4 equal  $16 \times 16$  quadrants in the layout. The remain place per quadrant is occupied by the binary current sources. Inside each quadrant the switching sequence is implemented. Two

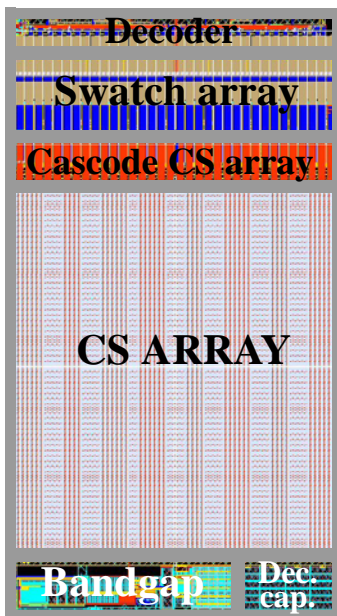


Fig. 7: Current steering DAC layout.

dummy rows and columns have been added to avoid edge effects. Finally, the routing is done on top of the transistors using high metals. In this way, both the active area of the current source array and coupling are reduced.

Different power supply lines have been used for different parts of the circuit to reduce noise coupling to the sensitive analog blocks. Besides, wide substrate contacts and guard rings have been used. On-chip decoupling capacitors are also included in any empty space of the layout.

#### V. SIMULATION RESULTS

The performance of the DAC has been evaluated by electrical-level simulations using HSPICE and SPECTRE. Moreover, the results have been checked considering all process corners from  $-40^\circ$  to  $85^\circ$  and for a nominal 3.3V analog power supply with variation ranges of  $\pm 10\%$ .

Fig.8 shows a 50-iteration Montecarlo analysis where is evaluated the influence of random errors over the resolution. This test is carried out exciting the system with a low frequency input signal (to minimize possible high frequency distortion effects) and taking into account the device mismatches. A yield better than 99.7% can be confirmed.

Fig.9(a) shows the output spectrum for a single tone at 38MHz. It can be noted that the distortion caused by finite output impedance of the current sources, transient response, coupling, clock feedthrough, etc. is sufficiently low. In fact, the *SFDR* is better than 58dB in the worst case.

Both figures of merit *SNDR* and *SFDR* are based on a single tone input signal which concentrates the maximum power permitted by the system in a certain frequency. This is a pessimistic analysis because the distortion is directly proportional to the frequency and power input signal. A more realistic case consists in distributing the maximum power permitted by the converter by multiple tones, i.e., DMT signals. Fig.9(b) shows the output spectrum for an input DMT signal where 1536 tones are distributed from 4.3MHz to 34MHz suppressing 8 tones of each 128.

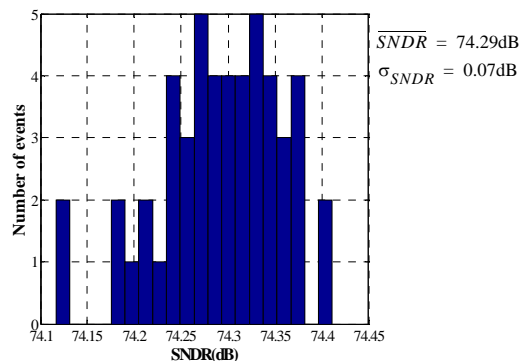


Fig. 8: Montecarlo analysis.



Finally, Table 2 summarizes the performance results. Experimental results will be presented on the symposium.

#### CONCLUSIONS

A segmented 8 + 4 bits CMOS current steering DAC with a *SFDR* better than 58.5dB up to 80MS/s and a *MTPR* higher than 59dB has been presented. It has been realized in 0.13 $\mu$ m CMOS, has an active area of 1.7 mm<sup>2</sup> and consumes 129mW for a 20mA full-swing output current. Systematic errors have been analysed and reduced by using an improved 2-D centroid switching scheme [10] and by a careful layout generation. The design has been computer-aided by a behavioural simulator which runs under MATLAB/SIMULINK.

#### ACKNOWLEDGMENTS

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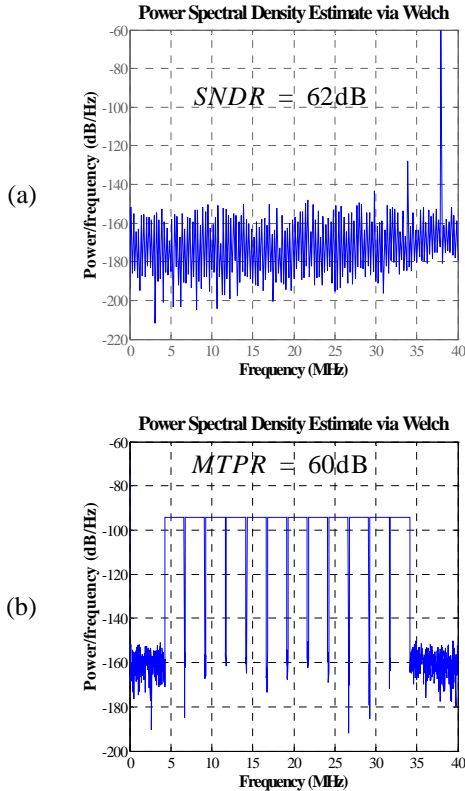


Fig. 9: Output spectra for (a) a single input tone at 38MHz and (b) a DMT test signal.

TABLE 2. Performance summary

Current Steering DAC 12bit@80MS/s	
Process	0.13 $\mu$ m CMOS
Resolution	12 bits
Differential Input Range	1 Vp-p
Power Supply	3.3V
Power consumption	129mW
Active area	1.7mm <sup>2</sup>
<i>MTPR</i>	> 59dB
<i>SFDR</i> (38MHz@80MS/s)	67dB
Output load	25 $\Omega$    20pF

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