A 12-bit CMOS Current Steering D/A Converter for Embedded Systems

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Abstract – **This paper describes the design of a 12-bit digital-to-analog converter for a wireline modem chip implemented in a 0.13μm digital CMOS technology. Transistor-level simulations from extracted layout at the nominal modem data rate of 80MS/s show an Spurious-Free Dynamic-Range (SFDR) better than 62dB at Nyquist rate under industrial operation conditions (-40 to 85º temperature range and ±10% supply variations) and for all technology process corners. Additionally, the converter achieves a Multi-Tone Power Ratio (MTPR) higher than 59dB for different Discrete MultiTone (DMT) test patterns consisting of 1536 carriers that fall in the Nyquist band. Simulation results at a higher data rate of 200MS/s are also shown in the paper. The converter dissipates less than 150mW from a mixed 3.3/1.2V supply and occupies less than 1.7mm^2.**

Keywords: **D/A converters, Digital-to-analog converters, Current-steering, Switching sequence.**

I. INTRODUCTION

Digital-to-Analog Converters (DACs) are essential components in applications such as video signal processing, digital signal synthesis, and broadband communications. Among several alternatives, current-steering DAC architectures have proven to be a suitable solution for these applications [1]-[3] because they can be implemented in pure digital CMOS technologies, with obvious integrability advantages, and are intrinsically faster and more linear than other solutions based on resistors or capacitors.

This paper presents an embeddable 12 bits resolution current steering DAC specifically designed for the analog front-end of a broadband wireline modem chip requiring a data converter rate of 80MS/s. The converter has been designed in a 0.13μm pure logic CMOS technology using thick oxide MOS devices for the analog part. At the nominal operating frequency of the modem, the DAC features high linearity under all industrial operation conditions and for all process corners, with a worst-case SFDR larger than 58dB from DC to 40MHz and a worst-case MTPR higher than 59dB for different DMT waveforms formed by 1536 frequency components that span the Nyquist band. Such values are more than 3dB above the targeted specifications to provide a safe integration margin. Further, when the converter is operated at 200MS/s, it achieves a worst-case Signal to Noise and Distortion Ratio (SNDR) at 80MHz higher than 55dB, thus revealing its potential use in other higher speed applications.

The paper is organized as follows. In Section II, the DAC architecture and its main design trade-offs are discussed. In Section III, the basic building blocks are presented. Layout issues are explained in Section IV. Finally, transistor-level simulations from extracted layout are shown in Section V.

II. D/A ARCHITECTURE

Fig.1 shows the block diagram of a generic segmented current-steering DAC, where an N-bit digital word is split into b Least Significant Bits (LSBs) which steer a binary-weighted current cell array, and t Most Significant Bits (MSBs) which are thermometer-wise decoded to steer a unary array of current cells. A latency equalizer is placed in the binary segment path to match the delay of the thermometer decoder. The current cells are switched on/off by means of switches which are synchronized and controlled by latches and driver circuits, respectively. These circuit elements compose the "swatch" array of Fig.1.

The segmentation level of the DAC is an important architectural choice which draws up a trade-off between static linearity (particularly affecting, the Differential Non-Linearity, DNL) and dynamic performance (glitch energy and SFDR) on the one hand, and area occupation and decoder complexity, on the other [2][4]. In the used technology, it has been found, with the aid of an in-house behavioural simulator [5], that the optimal segmentation is $t = 8$ and $b = 4$ for the targeted specifications.

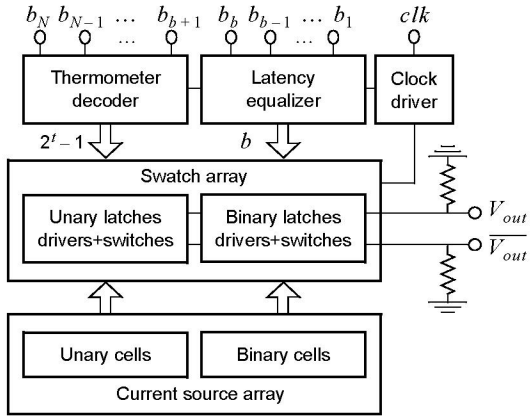


Fig. 1: Block diagram of a segmented current steering DAC.

In order to compensate for error sources such as thermal gradients, doping and oxide thickness variations, and edge effects two main techniques have been employed. First, each unary current source has been implemented as 16 units in parallel, divided into 4 groups (each consisting on 4 cells) and distributed in a double common-centroid topology. Second, an INL-bounded switching sequence [6] has been applied at each quadrant of the current source array to SNDR degradation due to linear and quadratic gradient errors.

In this design, the output of the DAC is differential so that common-mode distortion and noise are attenuated. Output currents are converted into voltages by means of two off-chip 25Ω grounded resistors. The DAC achieves 1Vpp differential output range through a full scale current, I_{FS}, of 20mA.

III. BUILDING BLOCKS DESIGN

A. Current sources and switches

Fig.2 shows the schematics of the current source (transistors M_{cs} and M_{cas}) together with the current steering switches (transistors M_{swp} and M_{swn}) – they compose a basic current cell of the DAC. Note that the current source uses PMOS transistors in order to increase the tolerance against substrate noise – essential for embedding applications. Sizing of the current cells has been tailored by two main objectives. On the one hand, matching errors between cells must be low enough so that the static performance of the converter is not degraded. On the other, the finite output impedance of the cell must be high enough so that the dynamic properties of the converter meet the targeted specifications.

The tolerable mismatch among current cells can be calculated from yield simulations. It can be found that to guarantee a 99.5% yield, the relative standard deviation of the current cells must satisfy $(\sigma_{i_{LSB}}/i_{LSB}) < 0.3\%$ [2]. Based on well-known mismatch statistical models, the minimum area of M_{cs} can be approximately calculated as,

$$(WL)_{min} = \left(A_\beta^2 + \frac{4A_{V_T}^2}{(V_{gs}-V_{th})_{cs}^2} \right) / (\sigma_{i_{LSB}}/i_{LSB})^2 \qquad (1)$$

where A_{V_T} and A_β are mismatch technology parameters and $(V_{gs}-V_{th})_{cs}$ is the gate overdrive voltage of M_{cs}. Another constraint on the size of M_{cs} is imposed by the full scale current as $i_{LSB} = I_{FS}/2^N$. Assuming a quadratic law for transistors in saturation, we have

$$i_{LSB} = \frac{1}{2}\mu_o C_{ox}\frac{W}{L}(V_{gs}-V_{th})_{cs}^2 \qquad (2)$$

On the other hand, the finite output impedance of the current cells has also a strong impact on parameters such as Integral Non-Linearity (INL), SNDR and SFDR bandwidth [7]. Fig.3 shows a representation of the achievable SNDR of the DAC converter in terms of the output impedance. As can be seen, to avoid distortion in excess, the output impedance must be higher than 5 MΩ in the Nyquist band. To this end, the current source uses a cascoded topology, and switches are forced in the saturation region when enabled. As will be shown, this is achieved by properly conditioning the activation signals of the switches.

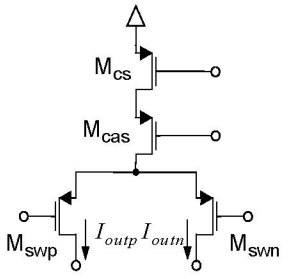


Fig. 2: Basic current cell topology.

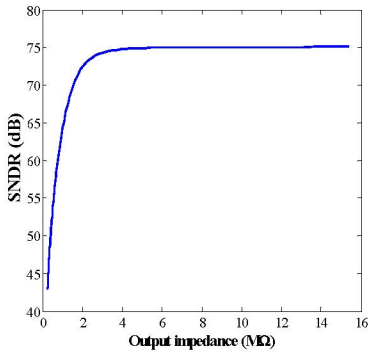


Fig. 3: Current cell sizing: SNDR versus output impedance.

Taking into account the above issues, the electrical-level sizing of the current cell was carried out considering, as additional constraints, glitch energy minimization and fast settling response issues.

B. Driver

Transistors M_{swp} and M_{swn} in Fig.2 are operating as switches with complementary activation gate signals. These signals, provided by a driver circuit, must be properly generated in order to minimize two important effects which can cause glitches at the output of the converter: (a) drain voltage variations of the current-source transistor and (b) coupling of the control signal through the gate to drain capacitance of the switches to the output. To this end, it must be prevented that both switch transistors are simultaneously in the off state. This can be done by forcing the two complementary signals which control the switch operation to have a non-symmetrical crossover. Fig.4(a) shows the circuit which carries out this function. It is a CMOS inverter with the lower supply voltage set at $V_{ref} = 0.9\text{V}$. Fig.4(b) displays the transient response of the driver circuit showing that the crossover point is well below half the supply voltages.

Fig. 5 shows the reference buffer circuit used to define on-chip the lower limit for the voltage swing of the switch drivers. A decoupling capacitor at the V_{ref} node has been used to reduce signal dependent fluctuations and, therefore, to limit the generation of harmonic components on the output signal.

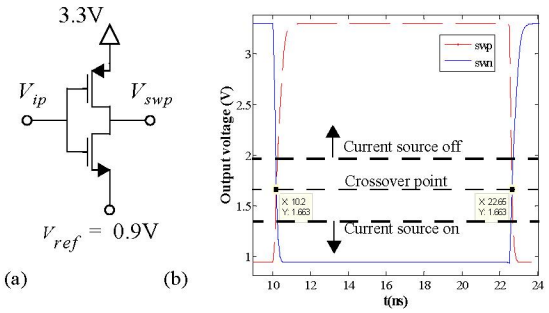


Fig. 4: Driver: (a) circuit implementation and (b) transient response.

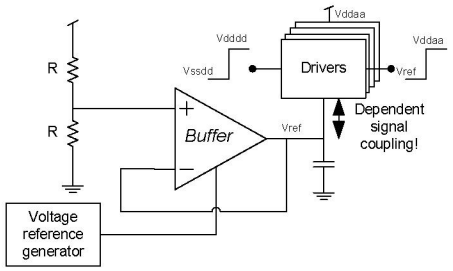


Fig. 5: Reference buffer to set the lower supply of the driver circuit.

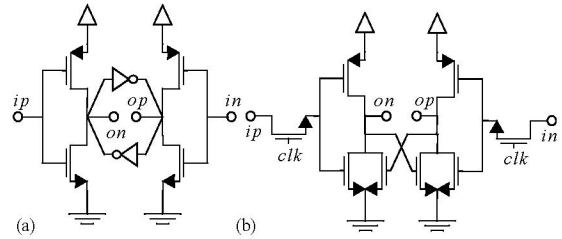


Fig. 6: Circuit implementation: (a) level shifter and (b) latch.

C. Level shifter, latch and digital circuitry

Fig.6(a) shows the level shifter schematic used for converting the digital signals processed by the decoder and the equalizer (see Fig.1) from 1.2 to 3.3V CMOS logic. They represent the input of the "swatch" array. Following the level shifter, two clocked latches are inserted before the driver circuit for synchronizing and shaping the digital waveforms. The first one is active-high and captures the output of the level shifter. The second one is active-low and provides its output to the driver. By that instant all outputs of the digital decoder (a combinational circuit) must be settled. The schematic of the latch circuit is shown in Fig.6(b).

Finally the thermometer decoder and the latency equalizer have been synthesized using commercial synthesis tools from a VHDL functional description based on the decoder presented in [3].

IV. LAYOUT ISSUES

The current steering DAC has been designed in a pure logic 1P-8M 0.13µm CMOS process. It occupies an active area of 1.78x0.96mm^2. Fig.7 shows it layout. The decoder has been placed on the top, far away and well shielded from the sensitive analog parts. The "swatch" array is below the decoder; in a separated array from the current sources to avoid coupling between the digital and analog parts. Two dummy rows and columns enclose the current source array to avoid edge effects. Routing between the current source and "swatch" arrays is done on top of transistors to save active area. Exhaustive use of substrate contacts, guard rings and on-chip decoupling capacitors have been also taken into account.

V. SIMULATION RESULTS

The performance of the DAC has been evaluated with both HSpice and Spectre and the results have been checked at all process corners under industrial operating conditions (-40 to 85º temperature range and ±10% supply variations).

Fig.8 has been obtained from electrical simulations of the extracted DAC layout, operated at the nominal modem data rate of 80MS/s. It illustrates the worst-case SNDR degradation against the input frequency and shows that the obtained resolution is higher that 58dB from DC to Nyquist frequency. On the other hand, Fig.9(a) plots the output spectrum for a single tone at 38MHz, showing an SFDR better than 62dB.

Both SNDR and SFDR evaluations are based on single tone input signals which concentrates the maximum allowed power in a given frequency. A more realistic situation in broadband applications consists on distributing the maximum power on several tones. Fig.9(b) shows the worst.case output spectrum for an input DMT signal where 1536 tones are distributed from

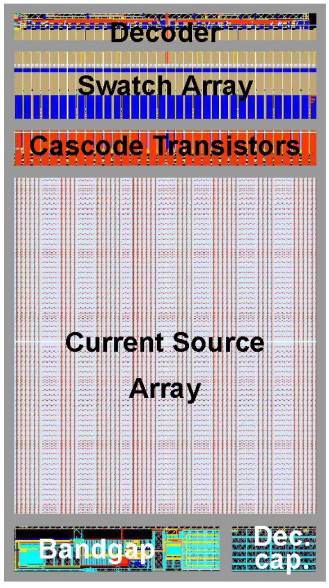


Fig. 7: DAC layout.

4.3MHz to 34MHz with 8 spectral notches each 128 tones. The MTPR is better than 59dB for all corners – similar results are obtained for other DMT patterns. Finally, Fig.10 shows the worst-case output spectrum for a single tone at 80MHz obtained at a sampling rate of 200MS/s, showing an SNDR higher than 55dB.

Table 1 summarizes the performance of the DAC. Experimental results will be presented in the Symposium.

CONCLUSIONS

A segmented 8+4 bits CMOS current steering DAC with a SFDR better than 58dB up to 80MS/s and a MTPR higher than 59dB has been presented. It has been realized in 0.13µm CMOS, has an active area of 1.7 mm^2 and consumes 149mW.

TABLE 1. Performance summary of the current-steering DAC

Process	0.13µm CMOS @ 3.3V
Resolution	12 bits
Sampling rate	80MS/s
Output Range (25Ω || 20pF load)	1Vp-p Differential
SFDR (15MHz@80MS/s)	58dB
SNDR (38MHz@80MS/s)	61.4dB
MTPR (1536 carriers)	> 59dB
Power consumption	149mW
Active area	1.7mm^2

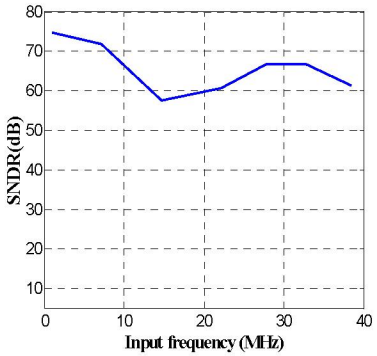
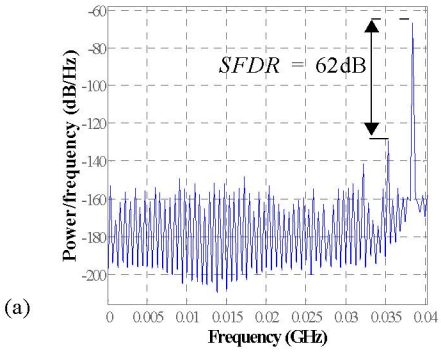
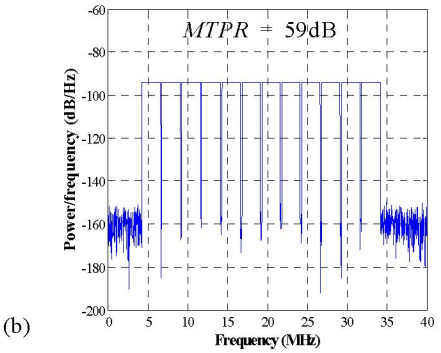


Fig. 8: SNDR against input frequency.



(a)



(b)

Fig. 9: Output spectra at 80MSA/s for (a) a single input tone at 38MHz and (b) a DMT test signal.

ACKNOWLEDGMENTS

This work has been supported by the MEDEA+ (A110-MIDAS) and TIC2003-02355 Projects.

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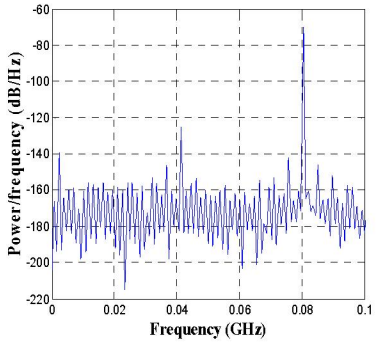

Fig. 10: Output spectra at 200MSA/s for a single input tone at 80MHz.