A 2.5MHz 55dB Switched-Current BandPass ΣΔ Modulator for AM Signal Conversion

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Abstract - We present a Switched-Current (SI) fourth-order bandpass ΣΔ modulator IC prototype. It uses fully-differential circuits in 0.8µm CMOS technology to obtain a Dynamic Range (DR) larger than 55dB at 2.5MHz center frequency with 30kHz bandwidth – in accordance to the requirements of AM digital receivers. The prototype incorporates a single-ended to fully-differential current-mode buffer for testing purposes. The power consumption of the whole prototype (modulator plus buffer) is 60mW from a 5V supply voltage.

1 Introduction

Prompted by the convenience to design mixed-signal chips using standard VLSI technologies, different authors have explored the application of switched-current (SI) circuits for analog-to-digital conversion [1][4]. Most of their effort have been focused on lowpass ΣΔ modulators (ΣΔM) for frequencies in the range of audio [1][2]. A few works have also explored the use of SI circuits for larger frequencies [3][4]. Particularly, [3] reports a 4th-order lowpass (ΣΔM) featuring 7.2bit@625kHz with power consumption of 40mW in a 0.8µm CMOS technology, while the higher frequency has been obtained using a Full-Nyquist converter that obtain 8bit@7.5MHz with 350mW, also in a 0.8µm CMOS technology [4]. These latter advances show promise for future application of SI techniques in the area of communications.

During the last few years bandpass ΣΔMs (BPΣΔM) have been demonstrated as basic building blocks for wireless Intermediate-Frequency (IF) communications [5]. A number of CMOS prototypes have been reported using switched-capacitor (SC) circuits [6][7]. However, very little has still been done on the design of this kind of oversampled modulators using SI circuits [8]. This paper presents a SI fourth-order BPΣΔM IC for converting AM signals. This circuit relies on the analysis of the major sources of errors which degrade the performance of SI cir-

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cuits to obtain 9bit resolution up to 1.25MHz IF and 8bit at 2.5MHz with a maximum sampling frequency of 10MHz, in CMOS 0.8μm technology. It uses fully-differential circuitry operating with 5V supply voltage and has a power consumption of 60mW – showing similar Power/Speed figures than others high-frequency SI converters [3][4].

2 Modulator Architecture

The modulator architecture has been obtained by applying a $z^{-1} \rightarrow -z^{-2}$ transformation to a 2nd-order lowpass modulator. Because of this transformation, which keeps the stability properties of the lowpass modulator, the integrators become resonators. There are several alternative structures to realize the resonator function using SI circuits. The structure shown in the inset of Fig.1 has been chosen because it keeps the poles in the unit circle upon changes due to mismatches of the resonator's feedback coefficients. Fig.1 shows the block diagram of the bandpass modulator, where the required delay in the feedback loop has been realized through two additional delay blocks. Assuming as customary for ΣΔ circuit design that the 1 bit quantizer can be modelled as an additional white noise source with effective gain of *k*, the output is given as,

$$Y(z) = z^{-2}X(z) + (1+z^{-2})^2 E(z) \tag{1}$$

where *X(z)* is the modulator input signal, *Y(z)* is the modulator output, and *E(z)* is the additional quantization noise source in the linear model. We see that the transfer function for the input is a double-delay; on the other hand, the transfer function for the quantization noise has two transmission zeroes at $f_s/4$ where f_s is the sampling frequency. This is the equivalent of the two zeroes at DC observed in the lowpass prototype. The scaling factors have been optimized to obtain similar dynamic range for both resonators, giving $A_{RES2}^{nom} = A_{DAC2}^{nom} = -A_{DAC1}^{nom} = 1$ and $A_{RES1}^{nom} = 1/2$.

3 Switched-Current Implementation of the modulator

Memory Cell and Integrator: The most basic linear block is the memory cell. We use a fully-differential second generation regulated-folded-cascode structure which increases the input conductance through the incorporation of a local feedback in the signal path, thus reducing the error due to finite input conductance, ε_g [9]. Fig.2 shows the schematic of the integrator including the common mode feedback circuit (CMFB) ($M_{16\text{-}24}$). It consists of two regulated-gate cascode [10] (RGC) groups. The local feedback stage (regulated-cascode stage) is made up of $M_{3\text{-}6}$; the memory transistors are $M_{1,2,1',2'}$; the supply current mirrors are $M_{9\text{-}15,15'}$. The steering switches are PMOS while the memory switches are NMOS; the latter include dummy devices for feedthrough attenuation. Because of the feedback, the memory cell exhibits a third-order dynamics with a single pole at $C_{gs_{1,2}}/g_{m_{1,2}}$ and a pair of complex conjugate poles whose values depend on the transconductances and the parasitic capacitances of $M_{3\text{-}6}$ and the steering switches. Two extra MOSFET connected to the memory nodes (see Fig.2) are used to create a dominant pole at $(C_{gs1,2} + C_H)/g_{m1,2}$ and, thus, to control the error due to incomplete settling, ε_s, by proper sizing of the memory transistor. These extra capacitances reduce also the common-mode charge-injection error, ε_q.

The memory cell has been designed using a transistor-level optimizer [11] to attain the specifications required for AM digital receivers and, at the same time, optimize the trade-off between speed and dynamic range, for 10MHz sampling frequency. The resulting bias currents are: I_{bias} = 106.3μA, I_{biasR} = 120μA; on the other hand, C_H =1.4pF (realized through a 36μm x 36μm transistor). The simulated values of the errors are ε_g=0.06%, ε_q=0.3%, ε_s=0.3% – low enough to achieve the targeted modulator resolution. On the other hand, the in-band integrated thermal noise is -78.9 dB below the D/A reference current (50μA) – in compliance to the intended SNR of the modulator (>8 bit).

1-bit Quantizer and D/A: The 1-bit quantizer is made up of a regenerative latch [12] and an RS flip-flop that maintains the output value during the acquisition phase -- the phase where the resonators are feedback. Layout-extracted simulations shows 4% hysteresis – not problematic because the power of the in-band noise remains virtually unchanged for hysteresis as large as ten percent of the full-scale converter input. The 1-bit D/A converter used in the modulator consists of a current source controlled by the comparator output.

Current Mode Buffer: We have incorporated a single-ended to fully-differential high-frequency current mode buffer at the front-end of the modulator. Fig. 3 shows the schematic of this circuit. This buffer is used to isolate the on-chip circuitry from the parasitic time constants at the chip input pads, thus allowing us to take full advantage of the speed capabilities of the current-mode circuitry. The condition $C_{PAD}R_{in} \ll 1/f_{input}$ is the basic specification in the design of the buffer, which is intended for 10MHz sampling frequency. In addition, its SNR must be in compliance to the intended SNR of the modulator (>8bit).

4 Experimental Results

Fig.4 shows the microphotograph of the modulator. It occupies 0.48mm^2 active area and consumes 60mW from a 5V power supply. For testing, the input is applied using the single-ended sinusoidal signal source HP3314A through an off-chip resistor (for V/I conversion) connected to the input pad and then to the on-chip current buffer. The output bit streams were captured with the HP82000 data acquisition equipment. Hanning-windowed 32768-point FFTs were performed on each of those bit streams using MATLAB. Fig.5(a) shows a measured modulator output spectrum for a -9dB input amplitude@2.5MHz signal frequency@10MHz sampling frequency. Fig.5(b) shows a measurement of the SNR figure vs. relative input amplitude for a single tone of 2.47MHz and an oversampling ratio of 167 (nominal value corresponding to a signal bandwidth of 30kHz). The measured DR is larger than 55dB(8.8bit), which is illustrated with a linear regression curve obtained processing the experimental SNR data. The SNR-peak is 48dB (7.8bit). Table 1 summarizes the modulator performance for different sampling frequencies and oversampling ratios. It shows DR > 55dB up to 10MHz sampling frequency – in accordance to the requirements of AM digital receivers.

Summarizing, the results in this paper demonstrate the possibility to design high-frequency SI circuits with around 9bit precision through proper control of the main errors which degrade the performance of this kind of circuits.

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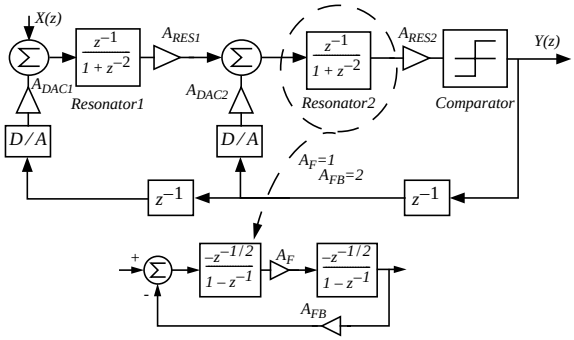


Fig. 1 Block Diagram of the Modulator.

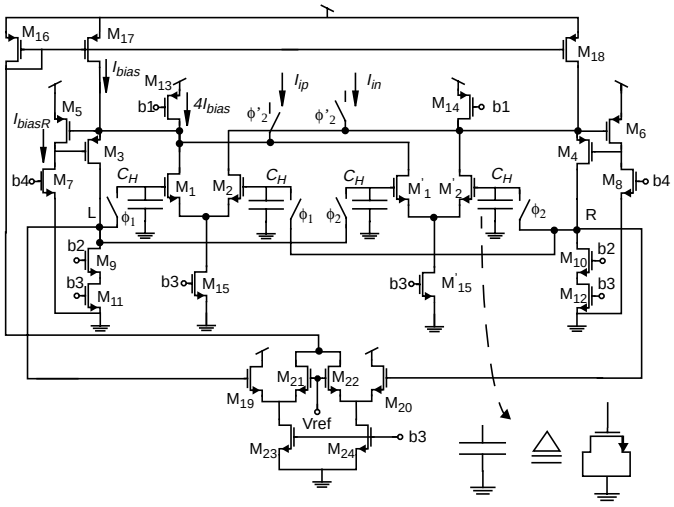


Fig. 2 Schematic of the Integrator.

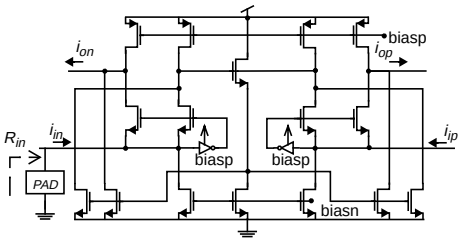


Fig. 3 Current Mode Buffer.

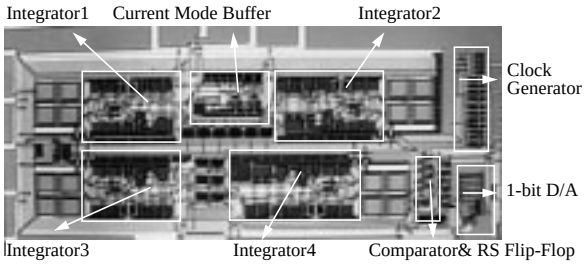
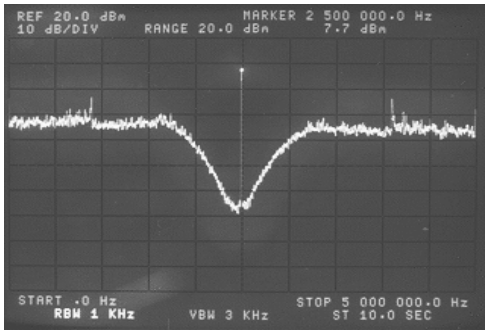
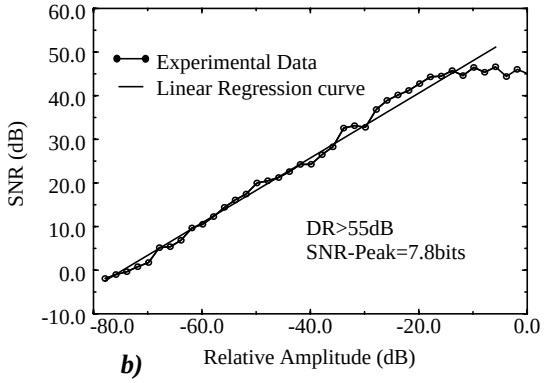


Fig. 4 Microphotograph of the Modulator.



a)



b)

Fig. 5 a) Measured output spectrum of the modulator for -9 dB@2.5MHz input single tone. b) Measured SNR for an input tone of 2.47MHz@*BW*=30kHz@10MHz clock frequency.

TABLE 1. Summarized modulator performance

	***BW*=30kHz**	***BW*=20kHz**	***BW*=15kHz**	***BW*=10kHz**
SNR-Peak (dB)	47	49	54	55
DR(dB)	55	58	64	64
IF Freq. (MHz)	2.47		1.23	
Sampling Frequency (MHz)	10		5	