Tools For Automated Design of ΣΔ Modulators

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Abstract

We present a set of CAD tools to design ΣΔ modulators. They use statistical optimization to calculate optimum specifications for the building blocks used in the modulators, and optimum sizes for the components in these blocks. Optimization procedures at the modulator level are equation-based, while procedures at the cell level are simulation-based. The toolset incorporates also an advanced ΣΔ behavioral simulator for monitoring and design space exploration. We include measurements taken from two silicon prototypes: 1) a 17bit@40kHz output rate fourth-order low-pass modulator; and 2) a 8bit@1.26MHz central freq@10kHz bandwidth band-pass modulator. The first uses SC fully-differential circuits in a 1.2μm CMOS double-metal double-poly technology. The second uses SI fully-differential circuits in a 0.8μm CMOS double-metal single-poly technology.

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I. INTRODUCTION

The performance of a ΣΔ converter IC is ultimately limited by its analog circuitry: the ΣΔ modulator front-end. Thus, efforts to enhance the performance or widen the application range of these converters concentrate mostly on the modulator and follow two parallel and largely correlated directions: exploration of high-order architectures and/or multibit quantizers and, pushing the specifications of analog cells used in the modulators at their performance edges [1][2][3]. The confrontation of these issues poses significant difficulties to IC designers. Some of the problems encountered are general of analog IC design: large number of specifications, complicated relationships between specifications and design parameters, involved analysis, critical specifications significantly sensitive to mismatch, etc. Others are specific to ΣΔ modulators; in particular, its accurate simulation is costly due to its highly non-linear dynamics and the necessity to use long time-series of data for evaluation purposes [5][6][7]. These difficulties render the design of ΣΔ modulator ICs a time- and resource-consuming process, and have prompted the development of tools which can help to increase designer productivity and, thus, reduce time-to-market and production cost of forthcoming generations of ΣΔ-based mixed-signal ASICs.

This chapter presents a set of CAD tools for computer-aided design of CMOS *switched-capacitor* (SC) and *switched-current* (SI) ΣΔ modulators for *low-pass* and *band-pass* applications. These tools use *optimization* at the modulator and cell levels, advanced *behavioral simulation* at the modulator level, and include the capability of fast design space exploration of modulator architectures. The tools are vertically integrated to support top-down design of ΣΔ modulators, from the high-level specifications to the sizes of the cells. Their use is demonstrated in the paper through two fully-differential silicon prototypes in CMOS technologies: a fourth-order two-stage SC ΣΔ modulator and a fourth-order band-pass SI ΣΔ modulator.

II. TOOL DIAGRAM

Fig. 1 shows the design flow of ΣΔ modulators. It comprises top-down *synthesis* tasks:

1. ***Topology selection,*** i.e., to identify the best suited modulator architecture for the required high-level converter specifications (signal baseband, resolution, etc.);
2. ***Modulator sizing***, i.e., to map these high-level specifications into specifications of the basic building blocks (such as gain-bandwidth product of the opamp, slew-rate, comparator hysteresis, etc.);
3. ***Analog cell selection***, i.e., to choose the cell schematics according to the specifications;
4. ***Cell sizing***, i.e., to map the cell specifications into values of their components;
5. ***Layout.***

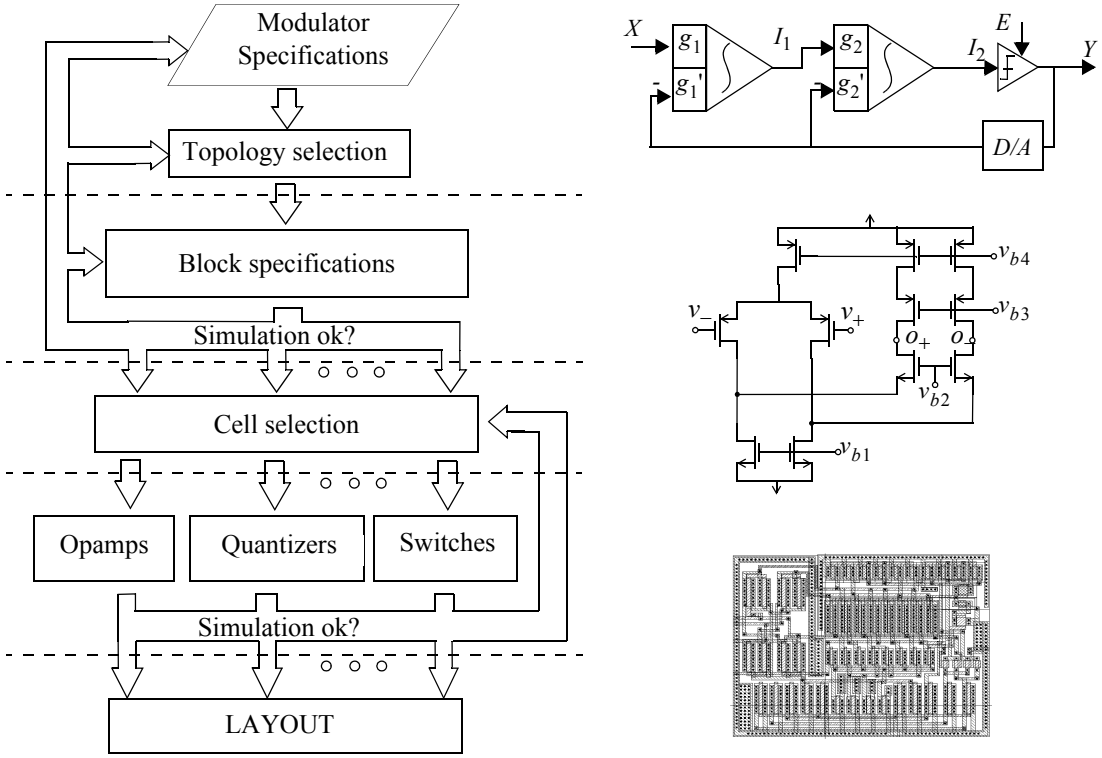


Fig. 1.Modulator design operation flow

These top-down tasks are complemented with bottom-up *analyses*:

6. ***Modulator simulation*** at the architectural level, to verify correctness of the results of high-level synthesis. Due to the large circuit complexity, and the need for long time series at the modulator output, this analysis is more conveniently handled through dedicated behavioral simulation.
7. ***Cell simulation****,* to verify synthesis at the *electrical* level using SPICE-like simulators [4].
8. ***Extracted layout simulation*** at electrical level -- very costly in CPU time and memory resources. Thus, it is typically used just to check connectivity and evaluate block performance degradation due to layout parasitics (not shown in Fig. 1).

The selection tasks (either modulators or cells) involve *knowledge* issues. The proposed tools include procedures to help designers in gaining insight about the operation of different modulator architectures, and hence guiding their selection. On the other hand, the sizing tasks involve principally *optimization* issues -- realized in our design framework through the use of *statistical* optimization techniques. Fig. 2 is a flow diagram of the top-down vertical integration of the set of tools described in this chapter [8].

III. DESIGN EQUATION DATABASE

These represent the behavior of typical modulator architectures realized with *switched-capacitor* (SC) and *switched-current* (SI) building blocks. The database has been conceived to be easily

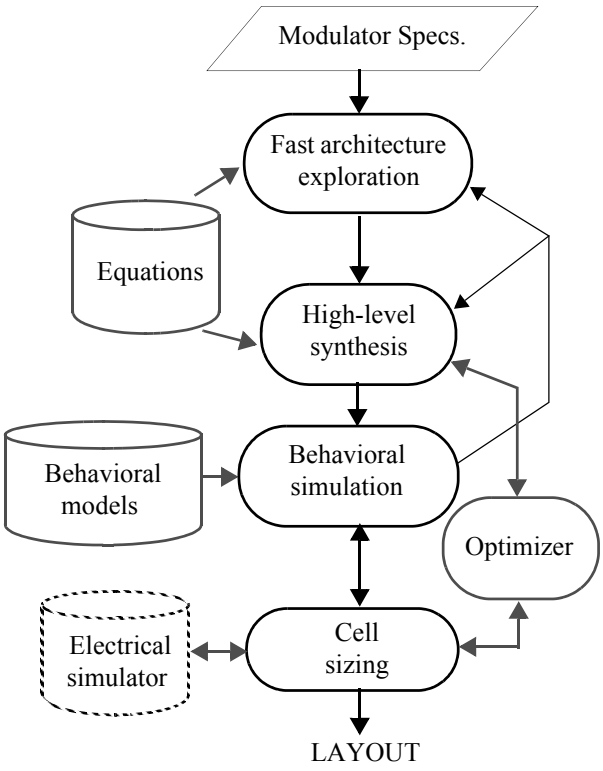


Fig. 2.Tool block diagram

extendible and includes *single-loop* as well as *cascaded* architectures, *low-pass* and *band-pass*, *single-bit* and *multi-bit*. Equations describing these architectures are classified in three categories:

- ***Architecture-related.*** These represent the *quantization noise* as a function of the non-idealities that affect its shaping. Their analytical expressions may be largely different for the different modulator architectures [8].
- ***Circuit-related***. These represent noise sources other than quantization: *thermal noise*, incomplete *settling*, harmonic *distortion*, etc [8].
- ***Fundamental limits.*** They cover trade-offs between power consumption, resolution, speed, etc., for the different topologies. They are used to guide modulator selection [1][11][13][15].

Table I summarizes the noise and distortion contributions covered in the two first categories above, together with the responsible building block. As an example, Table II shows the approximate expressions for the power of noise and harmonic distortion of a cascaded SC 2-2 architecture (see Fig. 10(a)[11][16]) .

IV. SIZING

Specifications contemplated for sizing include *constraints* on the performance parameters and design *objectives*. Their meaning is clarified considering for instance an opamp with the following

specifications: DC-gain > 70dB; gain-bandwidth product > 5MHz; phase margin > 60 degree; input equivalent noise < 3μV; with minimum power consumption and silicon area occupation. We call constraints to the four first specifications that include > or < symbols, and design objectives to the last two, whose goal is to maximize or minimize some magnitude.

TABLE I
NON-IDEALITIES CONSIDERED IN THE TOOL

Building Blocks		Non-idealities	Consequences
	Opamps	DC-gain, finite and non-linear	Increased quantization noise, harmonic distortion.
		SR, limited	Settling noise, harmonic distortion.
		GB, limited	Incomplete settling noise.
		O.S. limited	Overloading.
		Thermal Noise	White noise.
	Switches	ON-resistance, feed-through	Settling noise, white noise, harmonic distortion.
	Capacitors	Non-linear, mismatching	Increased quantization noise, harmonic distortion.
	Clock	Jitter	Jitter Noise.
	Comparators	Hysteresis, resolution time	Increased quantization noise.
	Quantizers	Non-linearity	Harmonic distortion.

TABLE II
APPROXIMATE ERROR POWER FOR A CASCADED ARCHITECTURE 2-2

Quantization noise	$\frac{\Delta^2}{12}\left\{\frac{4\pi^2}{3M^3}\mu^2+\frac{\delta_A^2\pi^4}{5M^5}+d_1^2\frac{\pi^8}{9M^9}\right\}$
Incomplete settling noise	$\frac{\Delta^2}{9M}\left(1+\frac{C_p}{C_1}\right)^2\varsigma^2\exp\left(-\frac{g_m}{C_{eq}}T_S\right)$
Thermal noise	$\left(1+\frac{C_{12}}{C_{11}}\right)\frac{kT}{4MC_{11}}+\left(1+\frac{C_{12}^2}{C_{11}^2}\right)\left(\frac{kT}{6MC_i}+\frac{kTg_mR_{on}}{2MC_i}\right)$
Non-linear capacitor distortion	$\frac{\alpha^2}{8}\left(\frac{\Delta}{2}\right)^4+\frac{\beta^2}{32}\left(\frac{\Delta}{2}\right)^6$
Non-linear opamp dc-gain distortion	$\frac{\lvert\alpha_1\rvert^2(1+k_1)^2k_2^4}{4A_0^2k_1^6}\left(\frac{\Delta}{2}\right)^4+\frac{\lvert\alpha_2\rvert^2(1+k_1)^2k_2^6}{8A_0^2k_1^8}\left(\frac{\Delta}{2}\right)^6$
Jitter noise	$\left(\frac{\Delta}{2}\right)^2\frac{(2\pi f_b\sigma_t)^2}{2M}$

Sizing itself is performed through a sequence of movements in the design space until a cost function reaches a minimum. The main related issues are *cost function* formulation, and the genera-

tion of *movements* and the *management* of the optimization procedure.

A. COST FUNCTION FORMULATION

The sizing of modulators and cells are formulated as *constrained* optimization problems,

$$\begin{aligned} &\text{minimize}[\Phi(\mathbf{x})] \quad \text{subject to} \\ &\phi_r(\mathbf{x}) \le 0 \;\; ; \;\; 1 \le r \le R \end{aligned} \tag{1}$$

where $\mathbf{x} = (x_1, x_2, \ldots, x_L)^T$ is the vector of design parameters, which defines a L-dimensional parameter space. From (1) an equivalent *unconstrained* problem is defined using different strategies for modulators and cells.

5. Cost function for modulator sizing

Calculated block specifications must fulfill the modulator specifications and, at the same time, be the best suited for implementation. For instance, the DC-gain and GBW of the opamps should be the lowest among the set of values which yield feasible modulators.

The modulator specifications are mapped onto a single constraint:

$$P_N(\mathbf{x}) - P_{N,\,max} \le 0 \tag{2}$$

where $P_N(\mathbf{x})$ is the total in-band output noise power at the modulator output, and $P_{N,\,max}$ is the maximum power that guarantees the modulator specifications: resolution, bandwidth and maximum input level. The cost function is given by:

$$\Psi(\mathbf{x}) = \begin{cases} -\sum_{j=1}^{N} K_j \log\left(\dfrac{x_j}{x_{j,\,norm}}\right) & if \;\; \mathbf{x} \in A \\ \log\left(\dfrac{P_N(\mathbf{x})}{P_{N,\,max}}\right) & if \;\; \mathbf{x} \notin A \end{cases} \tag{3}$$

where x_j represents the value of the j-th block specification. The sign of the weight parameters K_j, indicates if the objective must be maximized or minimized. On the other hand, the normalization factors,

$$x_{j,\,norm} = \begin{cases} x_{j,\,min} & if \;\; K_j > 0 \\ x_{j,\,max} & if \;\; K_j < 0 \end{cases} \tag{4}$$

are used to cope with large variations of the absolute values of different block specifications.

Logarithms in (3) renders the cost function smoother and thus, enable the trajectory to escape from local minima. The example of Fig. 3 illustrates the benefits of using logarithms. It corresponds to,

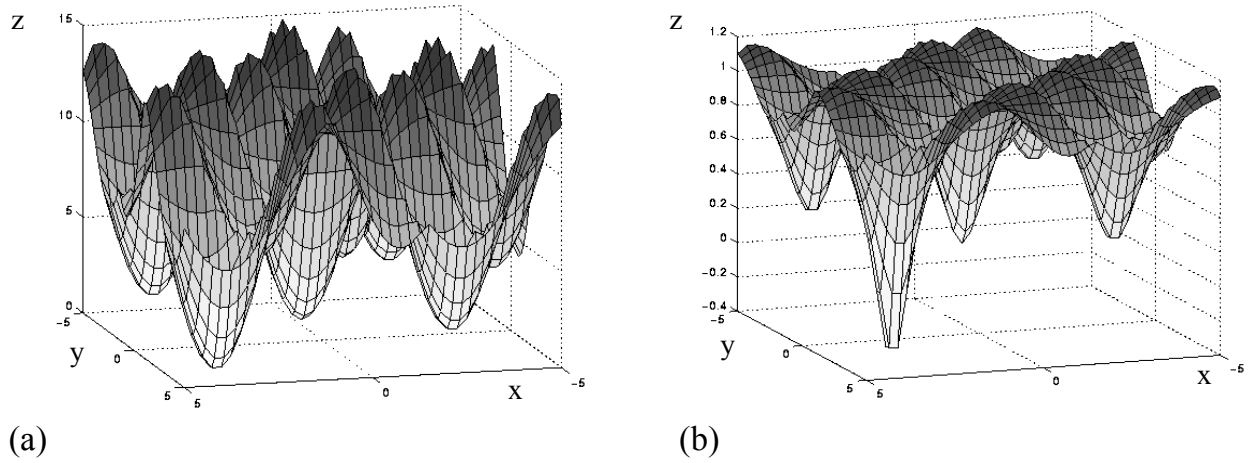


Fig. 3.Using logarithm to facilitate the search of the global minimum

$$f(x) = K \cdot min\left\{ -e^{-\xi \sum_{k=1}^{N} (x_k - d)^2} \prod_{k=1}^{N} \cos(x_k - d),\ -e^{-\xi \sum_{k=1}^{N} (x_k - d)^2} \prod_{k=1}^{N} \cos(x_k + d) + \gamma \right\} \tag{5}$$

where ζ, ξ, d and γ are constants. Fig. 3(a) depicts (5), which has the absolute minimum in $(x, y, z) = (4, 4, 0{,}5)$, and many local minima in its neighborhood. The values of the function at these minima are compressed into the interval [0.4, 0.5]. On the other hand, Fig. 3(b) depicts the result of taking the logarithm of (5), where the minima are more clearly separated. Functions like this are commonly found in modulator and cell sizing [8].

A. Cost function for cell sizing

Constraints related to cell sizing are classified in two groups:

- ***Strong restrictions****:* These are specifications whose fulfillment is considered essential by the designer; for instance, the phase margin of an opamp must be larger than 0 for stability. No relaxation of the specified value is allowed.
- ***Weak restrictions****:* These are the typical performance specifications required for analog building blocks, i.e. opamp DC-gain > 80dB. Unlike strong restrictions, weak restrictions allow some relaxation of their targets, making circuits which do not exactly meet the targets acceptable.

The costs function for cell sizing must reflect both types of constraints:

$$\begin{aligned} &\text{minimize} && y_{oi}(\mathbf{x}) && , 1 \le i \le P \\ &\text{subject to} && \begin{cases} y_{sj}(\mathbf{x}) \ge Y_{sj} \quad or \quad y_{sj}(\mathbf{x}) \le Y_{sj} & , 1 \le j \le Q \\ y_{wk}(\mathbf{x}) \ge Y_{wk} \quad or \quad y_{wk}(\mathbf{x}) \le Y_{wk} & , 1 \le k \le R \end{cases} \end{aligned} \tag{6}$$

where y_{oi} denotes the *i*-th design objective; y_{sj} y y_{wk} are constrained specifications (*w* and *s* denote *weak* and *strong* respectively) and Y_{sj} y Y_{wk} are the corresponding goals. The unconstrained cost function is defined as:

$$\Psi(\mathbf{x}) = \begin{cases} \Phi(y_{oi}) & if\ \mathbf{x} \in A \\ max[F_{sj}(y_{sj}), F_{wk}(y_{wk})] & if\ \mathbf{x} \notin A \end{cases} \tag{7}$$

where A denotes the acceptance regions, and where the partial cost functions are given by,

$$\Phi(y_{oi}) = -\sum_i w_i \log(|y_{oi}|) \qquad , F_{sj}(y_{sj}) = K_{sj}(y_{sj}, Y_{sj})$$
$$F_{wk}(y_{wk}) = -w_k \log\left(\frac{y_{wk}}{Y_{wk}}\right) \tag{8}$$

w_i is the weight associated to the *i*-th design objective, a real positive number (alternatively negative) if y_{oi} is positive (alternatively negative); for $K_{sj}(.)$ we have

$$K_{sj}(y_{sj}, Y_{sj}) = \begin{cases} -\infty & \text{if strong restriction holds} \\ \infty & \text{otherwise} \end{cases} \tag{9}$$

w_k is the weight associated to the *k*-th weak restriction -- a real positive number (alternatively negative) if the weak restriction is of $\geq$ type (alternatively $\leq$ type). These weights are used to give priority to some weak restrictions. There is no relation between the objectives and the weights of weak restrictions [18].

B. OPTIMIZATION ALGORITHM

Fig. 4 shows a block diagram of the operation flow of the proposed iteration procedure. The updating vector, $\Delta\mathbf{x}_n$, is *randomly* generated at each iteration. The value of the cost function is calculated at each new point of the parameter space, and compared with the previous one. The new point is accepted if the cost function has a lower value. It may also be accepted if the cost function increases, according to a *probability* function,

$$P = P_o e^{-(\Delta\Phi/T)} \tag{10}$$

depending on a control parameter, T (temperature). This probability of acceptance changes during the optimization process, being high at the beginning (for large T) and decreasing as the system cools (decreasing T). This is the well known Metropolis algorithm [17]. Our tool enhances the basic algorithms used for *cooling schedule* (mechanism to update T) and *design parameter updating* (mechanism to generate $\Delta\mathbf{x}_n$).

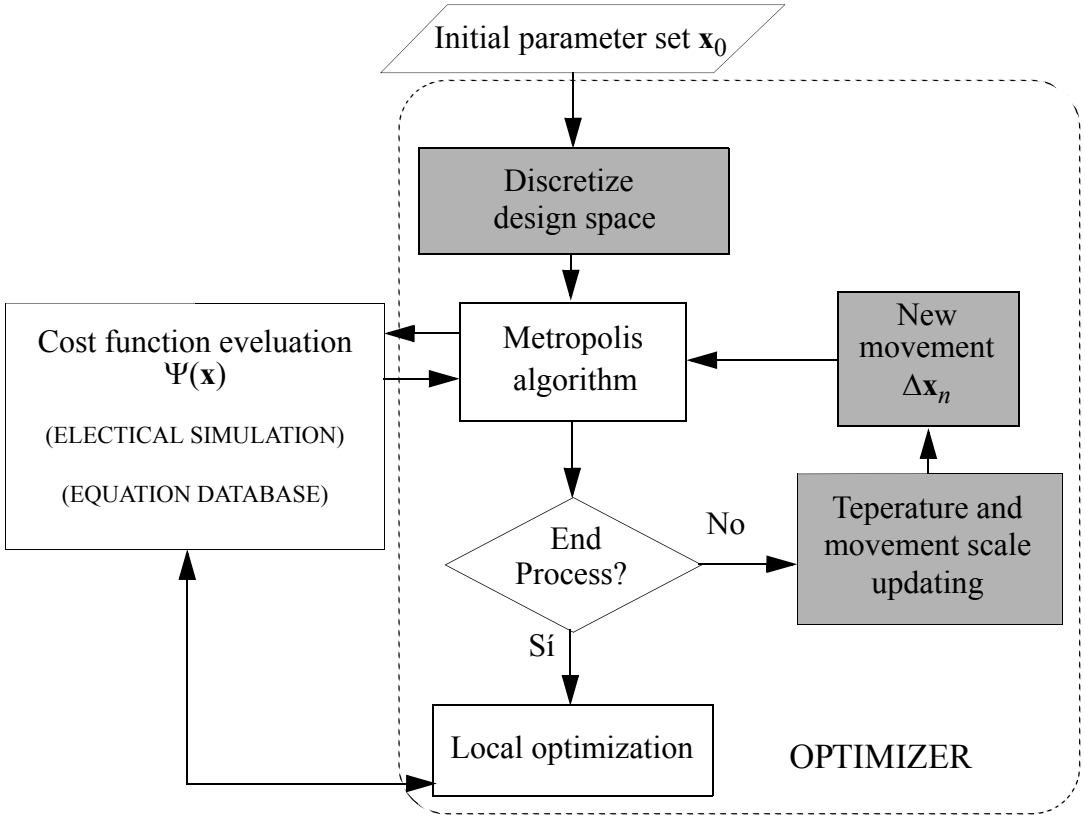


Fig. 4.Flow diagram of the proposed methodology

1. Cooling Schedule

In classical simulated annealing algorithm the cooling schedule is determined by four parameters: initial value of *T*, stop criterium, evolution law for *T,* and Markov chain length [17]. Our tool incorporates an algorithm based in the use of a composed temperature [8],

$$T = \alpha(\mathbf{x})T_o(n) \tag{11}$$

$\alpha(\mathbf{x})$ is employed to solve possible discontinuities of the cost function in the border of the acceptance region. On the other hand, $T_o(n)$ is a function of the iteration count and can vary *non-monotonically* with successive re-heatings and coolings. The tool incorporates an adaptive mechanism to automatically set the temperature and thus, keep a given *acceptance ratio*. Fig. 5 depicts the procedure. The instantaneous acceptance ratio $a[n]$ (one if the iteration has been accepted, zero if not) is low-pass filtered and the result is compared to the specified acceptance ratio $r_i[n]$ (commonly large at the beginning and decreasing with the iteration count). The difference between the ideal and actual acceptance ratio is integrated to obtain the new iteration temperature. The feedback loop forces the temperature to evolve such that $r[n]$ follows $r_i[n]$ -- depicted in Fig. 6. When compared with classical cooling schedules, the presence of spontaneous fast heatings and cooling has proven to be valuable to minimize complicated multi-minimum functions. In addition, the quality of the final result is only slightly dependent on the number of variables -- very convenient for analog sizing,

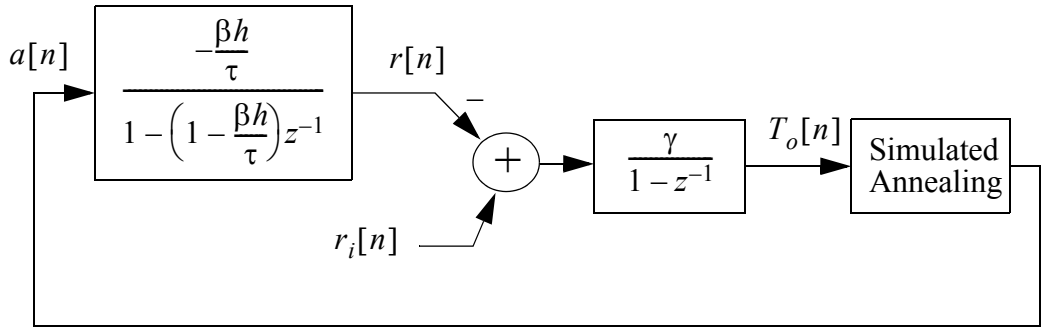


Fig. 5.Adaptive temperature flow diagram

where the number of design parameters is usually large.

2. Design parameter updating

Here the following heuristics are incorporated:

- Large amplitude movements of the design parameters are allowed at high *T*. On the contrary, acceptance probability decreases at low *T* and hence, only small movements are allowed.
- The possibility of defining logarithmic scales for independent variables with large variation range to ensure that their low range is not under-explored.
- Discretization of the design parameter space (see Fig.7). Only movements over vertices of the resulting multidimensional grid are allowed. If one vertex is revisited during the opti-

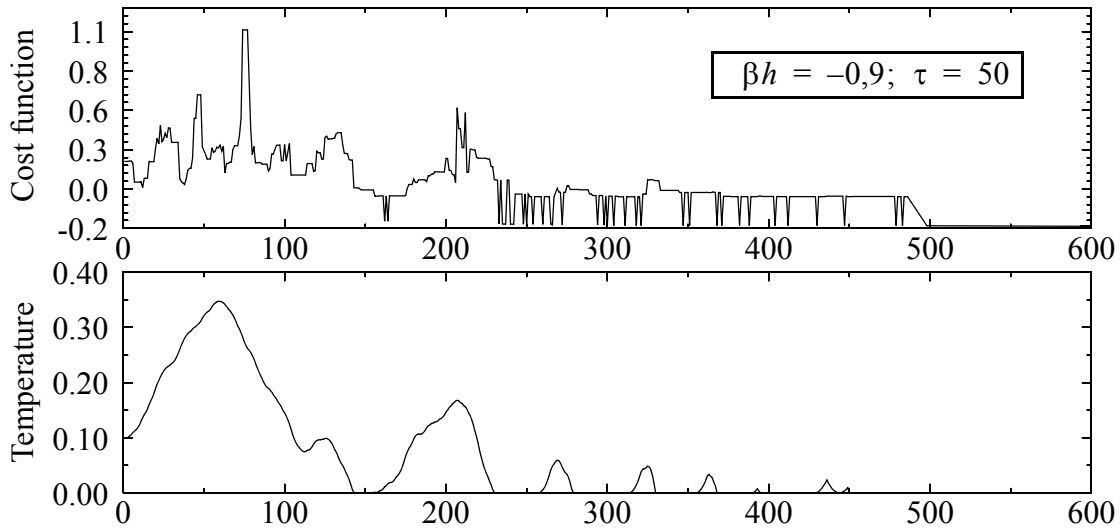


Fig. 6.Example of cost function, temperature and acceptance ratio evolution.

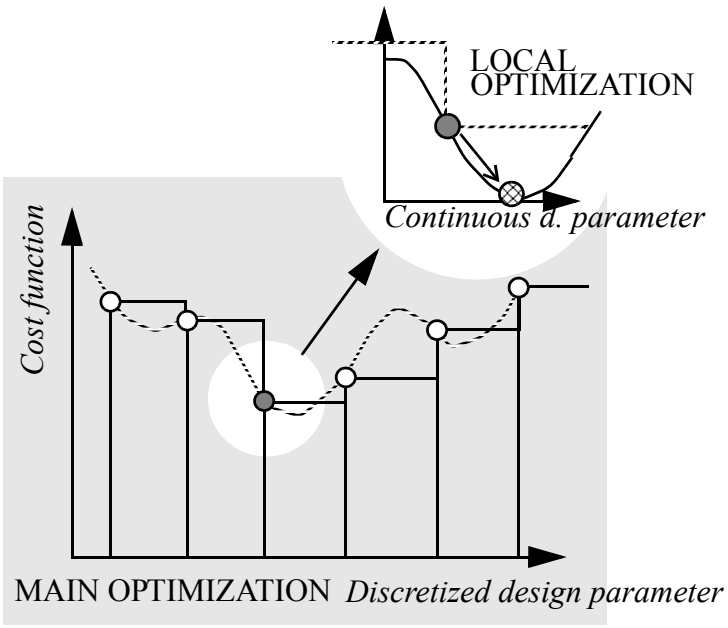


Fig. 7.Ilustrating the concept of discretized optimization

mization process the corresponding cost function evaluation need not be performed. When this optimization process ends, local optimization starts inside a multidimensional cube around the optimum vertex. During the local optimization it is possible to use a deterministic algorithm (Powell method) to fine tuning the design [9].

III. BEHAVIORAL SIMULATOR

The simulator incorporated to our tool, ASIDES, starts from an input netlist containing the modulator topology and a list of non-idealities to consider during simulation, and operates in time-domain using functional descriptions of the blocks. It generates a time series which is processed using a general-purpose DSP tool, for instance *MATLAB* [9] to provide:

- Information about the ***dynamic performance*** of the modulator, including the spectrum of the converter output, graphs of the signal-to-(noise + distortion) ratio (TSNR), etc.
- Information about its ***static performance***, through evaluation of integral non-linearity, offset, gain error, etc.
- ***MonteCarlo analysis***, taking into account fluctuations of both the integrator gains and the terminal specifications of the analog cells. These fluctuations can be indicated by the user or evaluated by the tool on the basis of technological parameters and layout-related variables, for instance the capacitor size and the partition used in their layout [10]. This capability is especially useful when cascade modulator architectures are considered because of their sensitivity to mismatching [11].
- ***Parameter sweep***, for design space exploration through visualization of the impact of crit-

ical design parameters on the modulator performance.

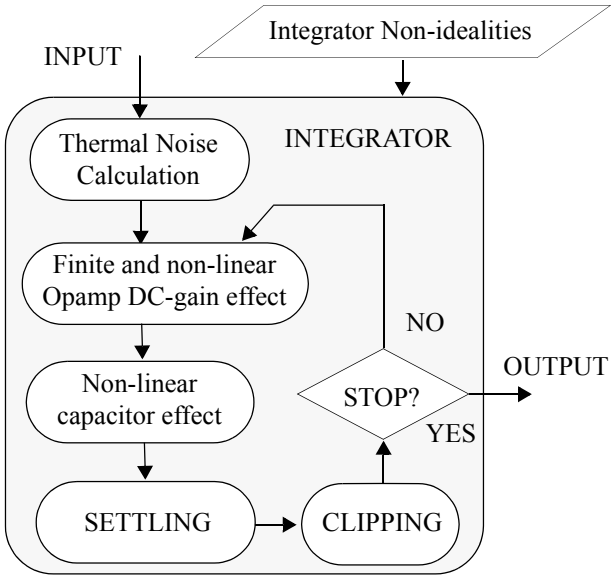
The catalog of building blocks in ASIDES includes *voltage sources, integrators, resonators, quantizers/comparators, adders, amplifiers, preamplifiers, delays, filters,* and generic *non-linear* blocks. Each is described through a dedicated routine in C-language. To obtain time series output, these routines are invoked according to the connection specified in the input netlist. Each block output is updated using its present input (and output) and a set of non-idealities related to the electrical implementation included in an associated block model.

Fig. 8(a) illustrates this operation flow for the integrator whose corresponding routine starts a loop that involves the following calculations:

- Thermal noise originated by the on-resistance of the switches and integrator opamps. The equivalent level of white noise is first calculated based on accurate analytical expressions for standard SC multi-branch integrators, and then added in time-domain to the integrator input using a random number generator [8].
- Non-linear scaling and leakage in the integrator due to finite and non-linear DC-gain of the opamps [8].
- Capacitor non-linearity, represented as a polynomial dependence of the capacitance value on the accumulated voltage [8].
- The value of the integrator output voltage is calculated at the end of the settling period. This calculation uses either a linear or non-linear expression of the settling depending on the integrator input, the slew-rate, the gain-bandwidth product and the phase margin of the opamp and the integrator gain [12][13].
- If the *output swing* of the integrator is surpassed, the output voltage is clipped to that value.

The iterative process shown in Fig. 8(a) is necessary due, on the one hand, to the interdependency between the opamp DC-gain and the integrator output and, on the other, to the relationship among the capacitor values and their accumulated voltages. However, two or three iterations are commonly sufficient to detect convergence and complete the simulation process. The remaining primitives considered in the behavioral simulator follow descriptions similar to that for the integrator.

Fig. 8(b) shows a typical input netlist; in this case for a fourth-order 2-2 cascade ΣΔ modulator [16]. The input is a pure tone with amplitude varying from -140dBV to 0dBV in 2dBV steps. The first and second stages are second-order modulators composed of two integrators and one comparator. All these elements are of real type and have associated models called "*im*" for the integrators and "*cm*" for the comparators. The cancellation logic, whose description is not completely printed, is formed using ideal delays and adders. The clock frequency is set to 35.2MHz with 1ns standard deviation jitter and the oversampling ratio is 64. Requested analyses include an FFT of the time series at the output node and the calculation of the signal-to-noise (SNR) curve at this node. They also include a MonteCarlo analysis of SNR with the integrator gains as random parameters. Those code lines that



(a)

```
# 2-2 Cascade SD Modulator #
##########################
Vin inp dc=0.0 ampl=(-140 0 2) freq=1.25k;

# First Stage -> 2nd-order mod.
Comp1 out1 (oi2) real cm;
I1 oi1 (inp,0*0.5 out1,0*0.5:2) real im;
I2 oi2 (oi1,0*0.5 out1,0*0.5:2) real im;

# Second Stage -> 2nd-order mod.
Comp2 out2 (oi4) real cm;
I3 oi3 (oi2,0*0.5 out2,0*0.5:2) real im;
I4 oi4 (oi3,0*0.5 out2,0*0.5:2) real im;

# Logic for noise cancelation #
Del3 14 (out1) full;
. . .
Ad4 out (21 15) ideal;
##########################
.clock freq=35.2X jitter=1n;
.oversamp 64;
.options fullydiff mismatch;

.output snr(out) monte=30;
.output fft(out);

# Models
.model im Integrator cunit=0.25p cfb=1p cpa=1.5p cnl=50u
   dcgain=70d dcgnl=20 ron=500 npwd=5n imax=800u
   gm=7m osp=3 osn=-3 pm=pmp;
.model cm Comparator vhigh=1.5 vlow=-1.5 hys=50m;
.param pmp= sweep (dec 10 100 100000);
```

(b)

Fig. 8.(a) Integrator operation flow. (b) Input netlist example.

start with "*.model*" in Fig. 8(b) are used to specify parameters associated with non-ideal features contemplated in the block models. Note that the opamp DC-gain is not given a numerical value, but specified through the parameter "*dcg*"; this is used to sweep a range of DC-gain values -- shown in the last command line in Fig. 8(b).

Fig. 9 depicts output provided by the simulator in the case of the netlist of Fig. 8(b), presenting three graphs corresponding to simulator outputs. The continuous trace in Fig. 9(a) shows the simulated output spectrum, while the dashed trace shows the corresponding ideal curve. Note the presence of harmonic distortion due to non-linearity of opamp DC-gain, and an unshaped noise floor around -120dBV mainly due to thermal noise. Fig. 9(b) shows the result of MonteCarlo analysis where all error sources other than mismatch have been disconnected to highlight the influence of the latter. It is of interest to compare the results of MonteCarlo simulation with a calculation of worst-case realized in a single instance of a corresponding equation contained in the equation database used for synthesis. Fig. 9(b) includes this calculated worst-case curve which coincides with the simulation results. Finally, Fig. 9(c) shows the SNR after decimation as a function of the opamp phase margin for -6dBV@5kHz input. Based on the information contained in this graphic one concludes that, for this case, a phase margin of 50^{o} suffices to reach maximum performance [8].

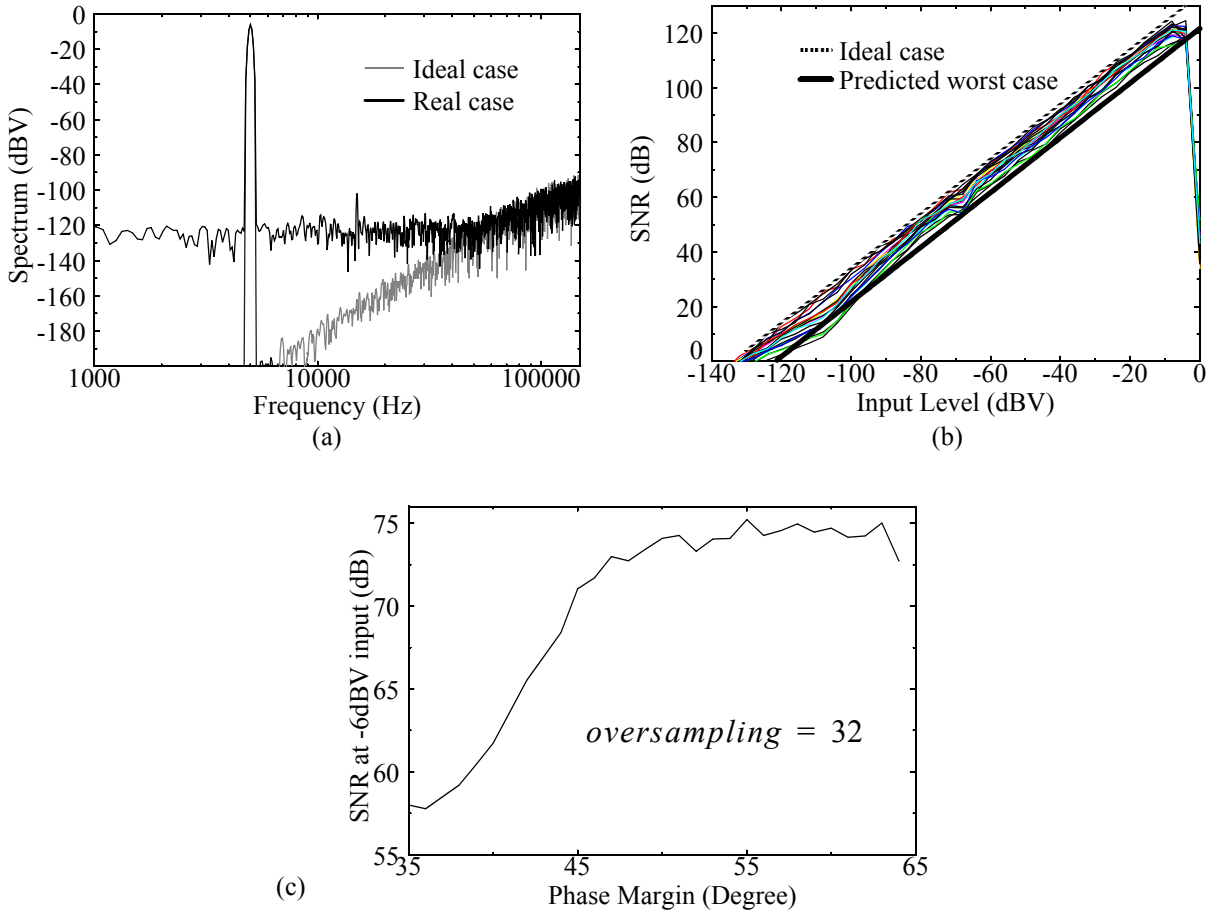


Fig. 9.Three simulator outputs: (a) Real and Ideal case output spectrum for a fourth-order 2-2 cascade ΣΔ modulator. (b) SNR vs. input amplitude including integrator gain mismatching. (c) SNR for -6dBV input vs. opamp phase margin.

IV. PRACTICAL RESULTS

The SC low-pass modulator of Fig. 10(a) has been designed to achieve 17bit@40kHz output rate, in a 1.2μm n-well double-poly double-metal CMOS technology [14]. On the other hand, the SI modulator of Fig. 10(b) has been designed for 8bit@+-5kHz bandwidth@1.26MHz central frequency, with a clock frequency of 5MHz in a 0.8μm n-well single-poly double-metal CMOS technology [21].

Table III displays the outcome of high-level synthesis for the SC structure. This is in the format provided by the high-level synthesis tool, which also summarizes the different noise contributions anticipated by the equations for the completed design -- displayed at the bottom in Table III. The associated statistical optimization procedures required 30,000 iterations for the SC modulator and 20,000 iterations for the SI modulator, and lasted 11.8s CPU time and 9s CPU time, respectively, on

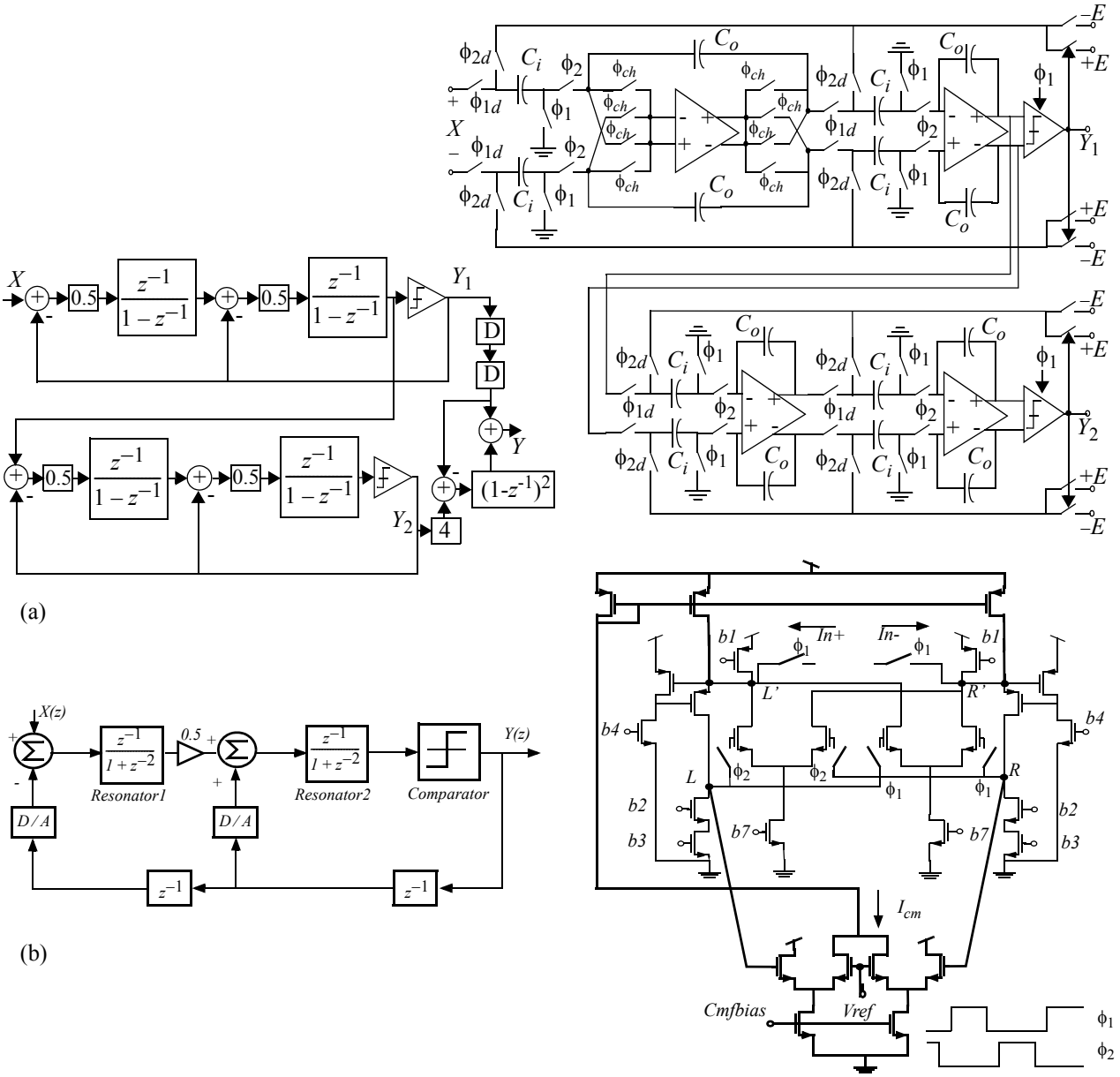


Fig. 10.(a) 4th-order two-stage SC ΣΔ modulator. (b) 4th-order SI band-pass ΣΔ modulator and fully-differential regulated folded-cascode SI integrator schematic

a 100MIPs workstation. These short CPU times are a positive consequence of using equations, and render the ability to explore design spaces through iterations of the optimum high-level synthesis procedure. For both architectures the sampling capacitor was fixed to a relatively small value to evaluate the ability of the procedure to obtain feasible designs in spite of a relatively large thermal noise contribution. In particular, the thermal noise contributed by a sampling capacitor of 1pF is at the very border of feasibility for the fourth-order SC modulator (see the bottom part of Table III). In this sense, the summary of noise contributions reported by the tool is of interest to guide design exploration if specifications are not met, and a new iteration of the high-level synthesis procedure is required.

Fig. 11 illustrates the use of the fast architecture exploration feature to evaluate the influence of two SI block errors in the noise transfer function (*NTF*) of the SI prototype: output-input conductance ratio error, ε_g; settling error ε_s; and the error due to changes in the feed-back loop gain in the resonator block.

TABLE III
HIGH-LEVEL SYNTHESIS TOOL OUTPUT

OPTIMIZED SPECS FOR:		**17bit@40kHz@±1.5V**
Modulator	Topology	Cascade 2-2
	Sampling frequency (MHz)	5.12
	Oversampling ratio	128
	Differential reference voltage *E* (V)	0.75
Integrators	Sampling capacitor C_i (pF)	1.0
	Feed-back capacitor C_o (pF)	2.0
	Unitary capacitance (pF)	>= 0.25
	MOS switch-ON resistance (kΩ)	<= 1.0
	Maximum clock jitter (ns)	<= 0.9
Opamps	DC-gain (dB)	>= 70.7
	DC-gain non-linearity (V^{-2})	<=20%
	GB (MHz)	>= 15.3
	Slew-rate (V/us)	>= 57.35
	Total output swing (V)	>= 6.0
	Input noise density (nV/sqrt(Hz))	<= 15.0
Comparators	Hysteresis (V)	<= 0.33
	Resolution time (ns)	<= 24.41
Technology	Cap Non-linearity (ppm/V)	<=50.0
RESOLUTION & NOISE POWER CONTRIBUTIONS		
Dynamic range:		**104dB (17bit)**
Quantization noise (dB)		-118.2
Thermal noise (dB)		-104.3
Incomplete settling noise (dB)		-177.7
Jitter noise (dB)		-111.2
Harmonic distortion (dB)		-117.7

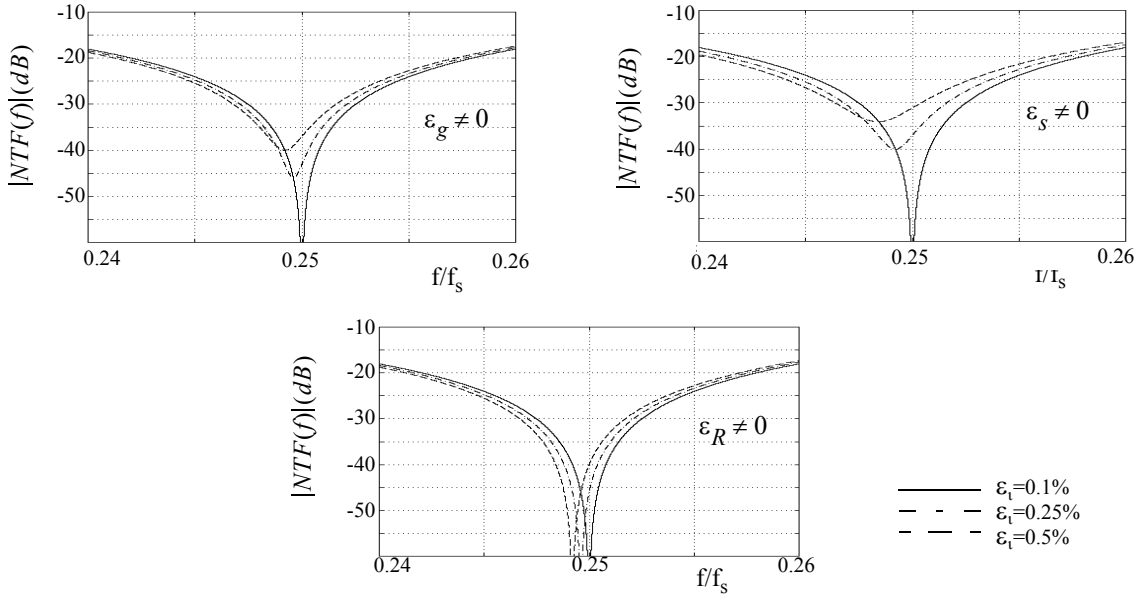


Fig. 11. Influence of non-idealities on NTF(z)

Fig. 12(a) presents the schematic of the opamp used for the SC topology: a folded-cascode fully-differential OTA with degenerated mirror common-mode feedback [19]. Fig. 10(b) shows the SI integrator used to implement the resonators in the SI prototype [21]. With regards to the comparator, since speed rather than hysteresis is the more demanding specification for both modulators, we used the regenerative latches: Fig. 12(b) for SC and Fig. 12(c) for SI.

The tool was used to automatically size the OTA, the SI integrator and the comparators to meet

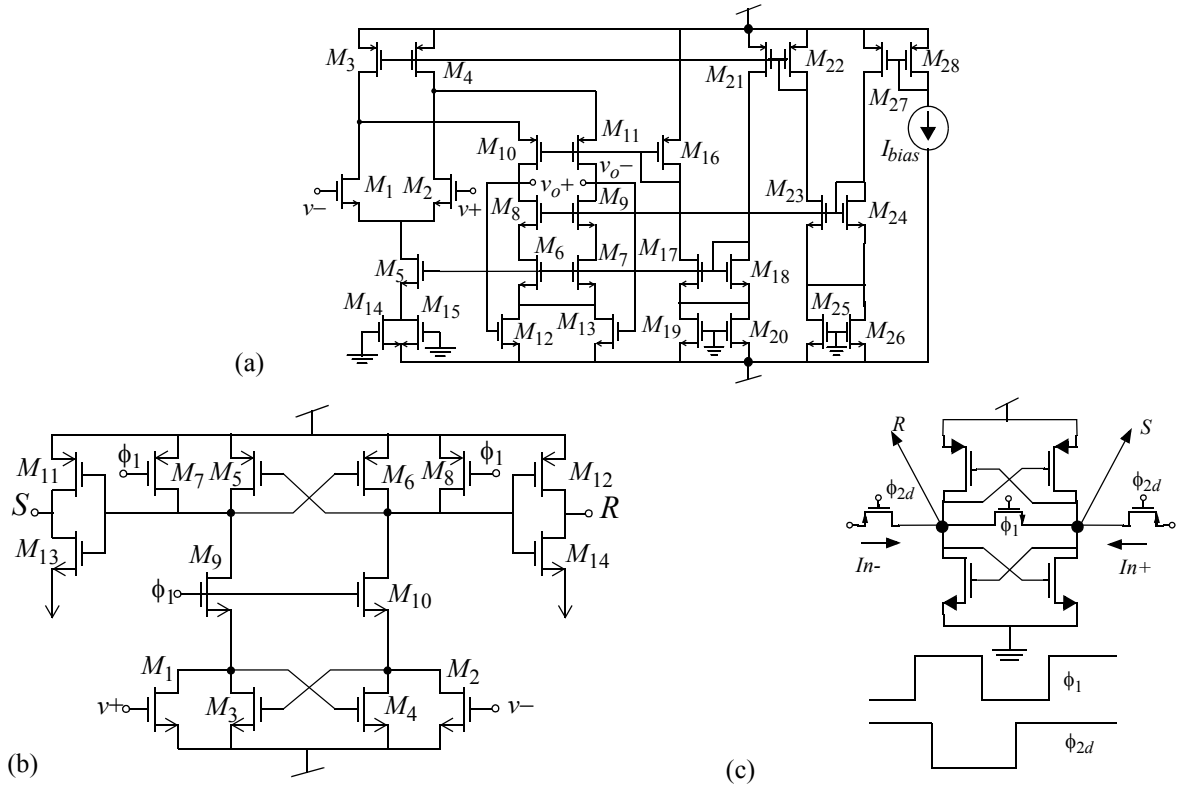


Fig. 12.(a) Folded-cascode OTA. (b) and (c) Regenerative latches

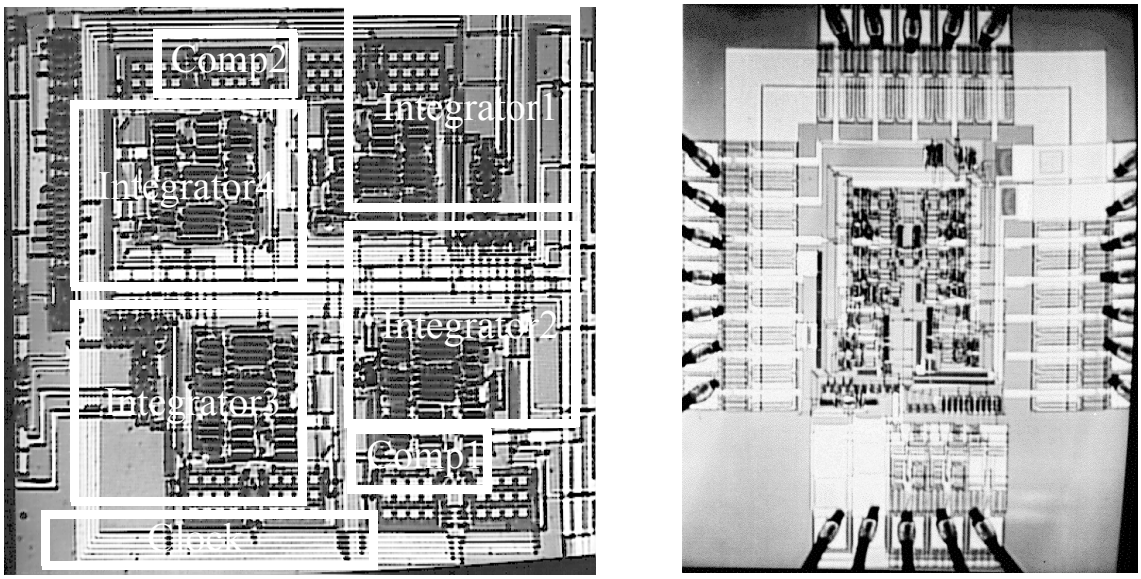
the specifications resulting from the high-level synthesis. The optimization process to obtain the sizes for the class-AB OTA required 45min CPU time, 35min for the SI integrator and 30min for the comparators. In all cases, the sizing started from scratch and no designer iteration was required. As an example, Table VI shows simulated and measured performances of the folded-cascode OTA

TABLE IV
SIMULATED AND MEASURED RESULTS FOR THE FOLDED-CASCODE OTA

	Specs	**Simulated**	**Measured**	**Units**
DC-gain	≥ 71	78.52	76.01	dB
GB (1pF)	≥ 16	34.88	–	MHz
GB(12pF, 1MΩ)		4.17	4.21	MHz
PM(1pF)	≥ 60	66.28	–	Deg.
PM(12pF, 1MΩ)		87.2	86.8	Deg.
Input white noise	≤ 15	13.53	–	nV/√Hz
SR	≥ 58	74.81	70.5	V/μs
OS	≥ ±3	± 3.2	± 3.0	V
Offset	–	–	3.35	mV
Power	minimize	1.95	1.93	mW

showing good concordance with the specifications.

Fig. 13(a) shows a die photograph of the complete SC prototype with 0.94mm^2 area and power consumption of 10mW@5V. A microphotograph of the SI prototype with 0.43mm^2 core area operating with 15mW@5V is shown in Fig. 13(b). To evaluate the performance of the two modulators, a test board was fabricated following the indications in [20] to reduce capacitive and inductive cou-

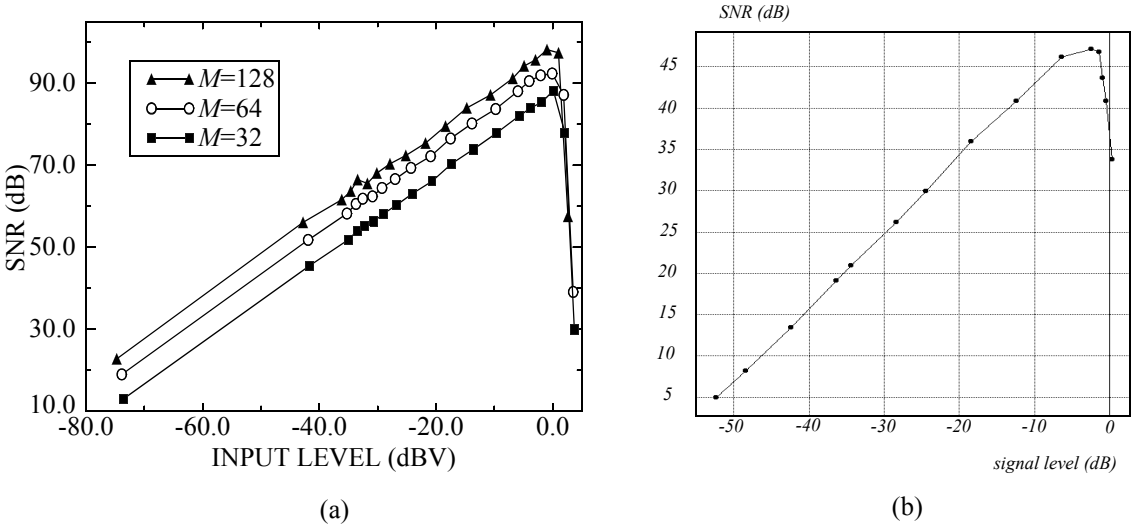


(a) (b)

Fig. 13.Microphotographs of the (a) SC prototype (1.2μm CMOS), and (b) SI prototype (0.8μm CMOS).

plings. The modulator input was provided using a high-quality differential sinusoidal signal source (less than -100dB THD) through a simple passive low-pass filter to prevent aliasing. The output series were acquired with an HP82000 unit and transferred to a workstation for processing. The cancellation logic of the fourth-order modulator, as well as the decimation digital filters, were implemented on a workstation using the same signal processor as used for simulations.

Fig. 14(a) presents the SNR of the fourth-order modulator as a function of the input level for



(a) (b)

Fig. 14.(a)SNR of the fourth-order prototype as a function of the input level for three values of the oversampling ratio; (b)SNR for the SI modulator.

three values of the oversampling ratio: 128 (nominal value), 64, and 32 which lead to 40, 80, and 160kHz digital output rate, respectively. Note that the modulator performance approaches the ideal as the oversampling ratio decreases, due to the fact that for low oversampling ratio the modulator is not thermal noise limited and thus, quantization noise dominates. The corresponding curve for the SI modulator with +-5kHz bandwidth arround the central frequency is given in Fig. 14(b). Fig.15(a) presents the baseband spectrum of the SC prototype obtained through an FFT of 65,536 consecutive output samples. The input was a -9dBV@4kHz sinewave sampled at 5.12MHz and compared to the output spectrum of its first stage, a second-order modulator. Differences between the two noise shaping functions are visible. However, the baseband of the fourth-order modulator is dominated by unshaped thermal noise. Our simulations show that this phenomena can be explained taking into account that the input noise power spectral density of the folded-cascode opamp was larger than expected. The output spectrum of the band-pass modulator for -6dBV@1.26MHz input tone is shown in Fig.15. Finally Table V summarizes the performance of both modulators.

TABLE V
PERFORMANCE OF THE FOURTH-ORDER ΣΔ MODULATOR

	SC Modulator			SI Modulator
Oversampling Ratio	128	64	32	165
Resolution	16.7	15.5	14.8	8

TABLE V
PERFORMANCE OF THE FOURTH-ORDER ΣΔ MODULATOR

	SC Modulator			SI Modulator
Oversampling Ratio	128	64	32	165
DR	102dB	95dB	91dB	50dB
SNR-peak	98.2dB	92.5dB	88.2dB	47dB
TSNR-peak	88dB	85dB	82dB	--
Noise Floor	-110dB			--
Max. Input	1V			10μA
Max. Sampling Freq.	5.12 MHz			5 MHz
Power (Average)	10 mW			15 mW
Area (without pads)	0.94 mm^2			0.46 mm^2

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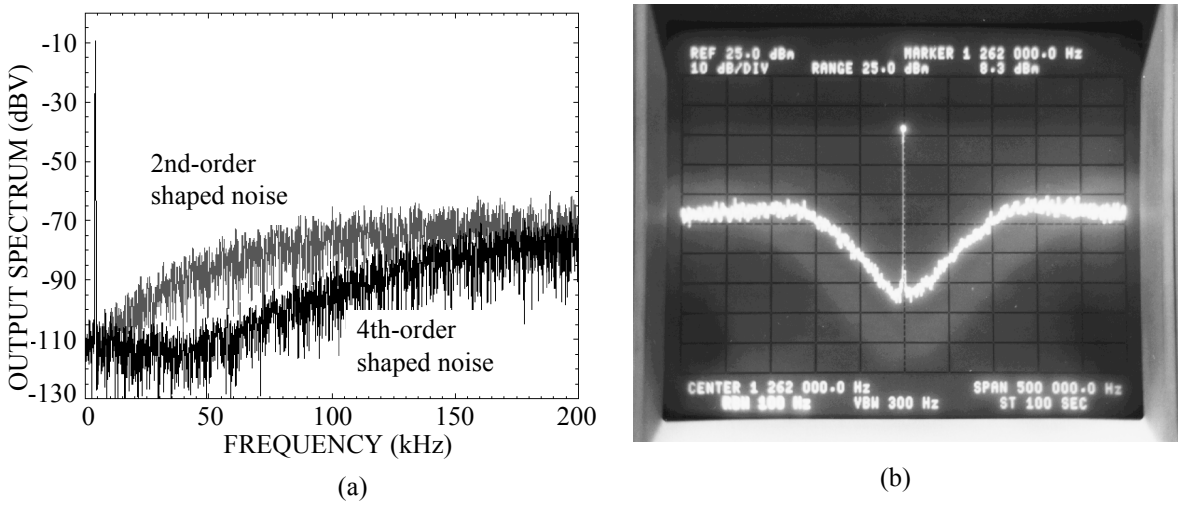

Fig. 15.Output spectrums: (a) Low-pass SC modulator, (b) Band-pass SI modulator

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