A 74dB Dynamic Range, 1.1-MHz Signal Band 4th-Order 2-1-1 Cascade Multi-Bit CMOS ΣΔ Modulator for ADSL

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Abstract - This paper explores the use of ΣΔ techniques for A/D conversion exceeding 1-MHz signal bandwidth. A cascade modulator architecture is proposed which combines single-bit and multi-bit quantization to obtain more than 12-b Dynamic Range (DR) with an oversampling ratio of only 16, and with neither calibration nor trimming required. Measurements from a 0.7μm CMOS prototype show 74dB DR in 1.1-MHz signal band at 35.7-MHz clock rate, with a power consumption of 55mW from a 5-V supply.

1 Introduction

Most of the previously reported CMOS or BiCMOS A/D converter exceeding 1-MHz signal band and 12-b or more resolution use pipeline or other Nyquist architectures [1]. However, some recent works [2][3][4][5] have demonstrated that oversampled converters, in particular those based in ΣΔ modulators (ΣΔM), can also be designed to operate in the proximity of this region of the speed - resolution plane, with the advantage of not requiring calibration or trimming techniques because of its intrinsic tolerance to circuit imperfections. Particularly, the modulator in the ADSL chip in [5] uses a 2-1-1 single-bit architecture to obtain 12b in 765-kHz signal band and a modulator power consumption of 210mW.

Because the quantization noise of a ΣΔM is inversely proportional to $(2^N - 1)^2$, where N is the number of bits of the internal conversion, using a multi-bit quantizer may increase the resolution in $3.32\log(2^N - 1)$ with respect to the single-bit case. On the other hand, because this improvement does not depend on the oversampling ratio, the use of multi-bit quantization allows us to combine high-resolution with large operation frequency. A major drawback of multi-bit quantization is due to the necessity of using extremely linear DAC in the feedback path. To overcome this problem several calibration techniques in the digital and the analog domain have been proposed [6][7][8]. As an alternative to these calibration methods, there exists the possibility of exploiting some architectural properties to attenuate the influence of the DAC non-linearity [2][9]. This paper combines single-bit and multi-bit quantization in a 2-1-1 cascade ΣΔM to obtain 12-b resolution for 1.1-MHz signal with only 16 oversampling ratio (*M*) and without calibration circuitry. This modulator achieves 40% larger signal band than the 2-1-1 single bit in [5], with similar resolution and about 80% reduction in the power consumption – thus demonstrating the viability and usefulness of multi-bit ΣΔMs for ADSL.

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2 Modulator Architecture

Fig.1 shows the block diagram of the modulator architecture. It is a fourth-order three-stage 2-1-1 cascade ΣΔM whose performance has been improved by including multi-bit quantization in the last stage (2-1-1mb). Ideally, after digital cancelation and observing the relationships of Table 1, the following is obtained for the Z-domain modulator output

$$Y(z) = z^{-4}X(z) + d_3(1-z^{-1})^4E_3(z) + d_3(1-z^{-1})^3E_D(z) \quad (1)$$

where $X(z)$, $E_3(z)$ and $E_D(z)$ are the Z-transforms of the input signal, last-stage quantization error and multi-bit DAC error, respectively. Note that the later is attenuated by a noise-shaping function of third order, which is one order higher than in other cascade multi-bit ΣΔMs [2][9] where the DAC errors are second-order shaped. Thus, the in-band noise power contribution of the D/A conversion error is inversely proportional to M^7. With this, the DAC linearity requirement becomes significantly relaxed, and a simple non-trimmed architecture can be used without calibration or digital correction techniques. This illustrated in Fig.2(a) where the signal-to-(noise + distortion) ratio (SNDR) of the 2-1-1 multi-bit ΣΔM with $M = 16$ is plotted as a function of the DAC non-linearity given in LSBs of 3bit. The advantages of the proposed architecture are highlighted by comparing its SNDR to those of a cascade 2-1 multi-bit [2] and a cascade 2-2 multi-bit [9]. Simulated data have been obtained using ASIDES [10]. Calculated data have been obtained assuming that the noise power of the DAC non-linearity, σ_D^2, is given by $\sigma_D^2 = (1/2)(INL|_{LSB})^2q^2$, where INL is the DAC integral non-linearity and q is the value of the LSB.

In practice, the integrator finite DC-gain and weight mismatches produce incomplete cancellation of the quantization noise generated in the first stage(s) of the cascade, thus degrading the SNDR at the modulator output. This imposes an upper limit to the useful resolution of the last-stage quantizer. Above this limits the benefits of finer quantization in the last stage are masked by the un-cancelled portion of the quantization noise of the previous stages. Fig.2(b) shows the half-scale SNDR obtained by behavioral simulation for a 2-1-1mb modulator as a function of the number of bits of the last quantizer. These simulations include typical levels of weight mismatching (0.2%) and finite DC-gain (60dB) of the integrators. According to these results, using quantizers with more than 3-b resolution does not make sense.

3 Switched-Capacitor Implementation

The 2-1-1 cascade multi-bit ΣΔM has been implemented using switched-capacitor circuits. The values of the integrator weights were optimized for maximum dynamic range and minimum integrator output swing and speed requirement giving $g_1 = g_1' = g_2' = g_3'' = g_4' = 0.25$, $g_2 = g_4 = 0.5$, $g_3 = 1$, $g_3' = 0.375$ and, consequently (see Table 1), $d_0 = -2$, $d_1 = 2$, $d_2 = 0$, $d_3 = 2$. Modulator timing consists in two non-overlapped phases and two slightly delayed versions of them. The specifications of the building blocks were calculated automatically using a modulator-level optimizer [10] to attain 12-b DR for 1.1-MHz signal band. Most significant results are M = 16; last quantizer resolution, N = 3; sampling capacitor and unitary capacitor = 0.5pF; integrator DC gain > 1000; opamp output current > 0.6mA; opamp transconductance > 4.2mA/V; switch on-resistance = 664Ω; DAC INL < 0.2LSB. Fig.3(a) shows the schematic of the fully-differential folded-cascode OTA used in the integrators. A dynamic, 4-capacitor CMFB net (not shown) was selected to improve the power consumption. Due to rather different loading conditions, two versions of the OTA were sized using a transistor-level optimizer [10]; one for the two first integrators and another for the last two. The small sensitivity of the 2-1-1mb ΣΔM to the last stage ADC and DAC allows us the use of the quite simple circuitry shown in Fig.3 (b): a 3-b flash converter where the comparators are simple regenerative latches (also sized using the tool in [10]); and a 3-b R-ladder DAC (R=307Ω).

4 Experimental results

Fig.4 shows a microphotograph of the modulator chip in a 0.7μm CMOS single-poly technology which occupies 1.3mm^2 and consumes 55mW from a 5-V power supply. The performance of the modulator was measured on a two-layer PCB with separated analog-digital planes, decoupling capacitor and terminated digital input/output. The input signal was provided by a high-quality differential signal generator. Data at the modulator output were acquired using a HP82000 unit (which also provided the clock and biasing voltages) and transferred to a workstation for digital filtering using MATLAB. Fig.5 shows the measured output spectrum after decimation (M = 16) for a -10-dBV, 126-kHz input tone at 35.7-MHz clock rate. The base band (1.1MHz) is dominated by unshaped, white noise and a small third-order harmonic (< -92dBV) is observed. Total in-band noise power is -71dB, which referred to the full-scale input (2V) leads to 74dB dynamic range. Fig.6 shows the measured SNDR as a function of the input level at 35.7-MHz clock rate and M = 16 (signal band = 1.1MHz). Premature overload is due to an improper strobing of the first comparators, which generate wrong outputs and force the third stage to enter in saturation for large modulator input. This problem has been solved in a new prototype not yet available. Fig.7 shows the in-band noise and distortion power as a function of the clock rate for M = 16. Note that up to 22-MHz clock rate the in-band noise power is around -77dB, equivalent to 80dB DR, which fully agrees with the result obtained by behavioral simulations. Beyond that frequency the performance decreases due mainly to the switching noise in the test set-up. We think that the measured performance of the modulator at the nominal clock rate can be further improved by lowering the biasing voltage of the digital part and using a multi-layer PCB.

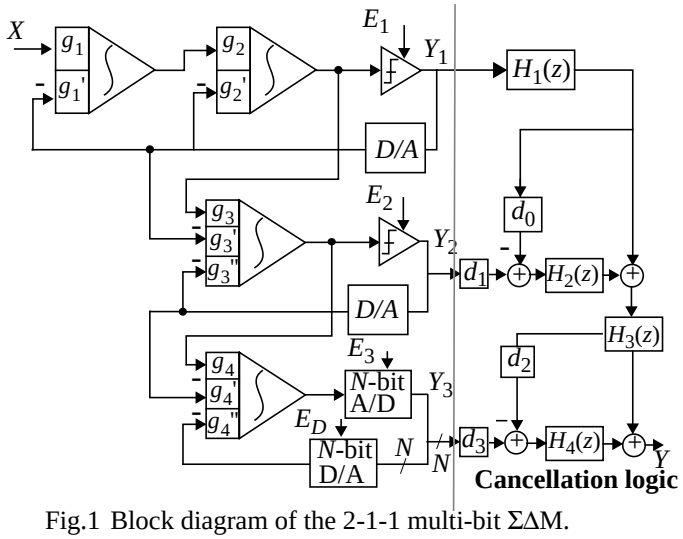


Fig.1 Block diagram of the 2-1-1 multi-bit ΣΔM.

Table 1: Coefficient relationships in Fig.1

Digital	Digital/Analog	Analog
$H_1(z)=z^{-1}$	$d_0=1-g_3'/(g_1g_2g_3)$	$g_1'=g_1$
$H_2(z)=(1-z^{-1})^2$	$d_1=g_3''/(g_1g_2g_3)$	$g_2'=2g_1'g_2$
$H_3(z)=z^{-1}$	$d_2=0$	$g_4'=g_3''g_4$
$H_4(z)=(1-z^{-1})^4$	$d_3=g_4''/(g_1g_2g_3g_4)$	

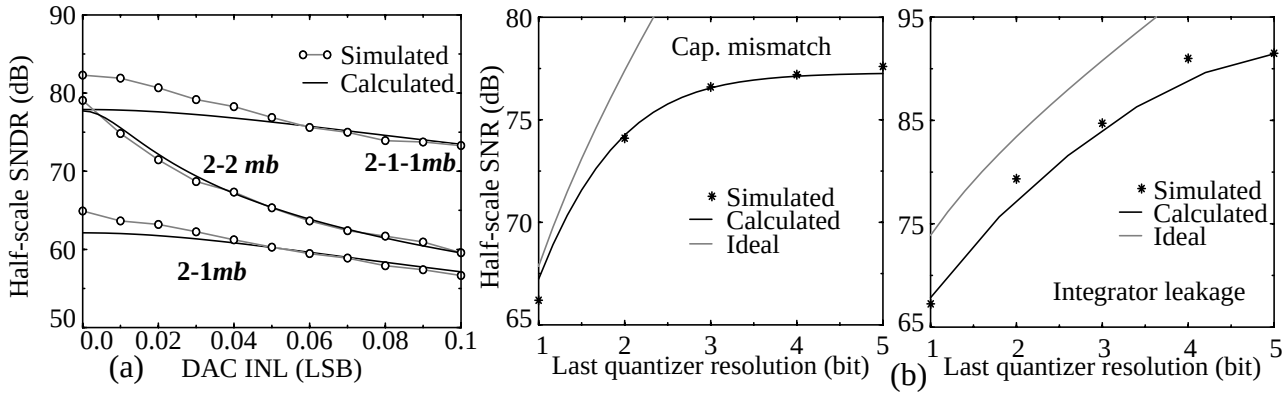
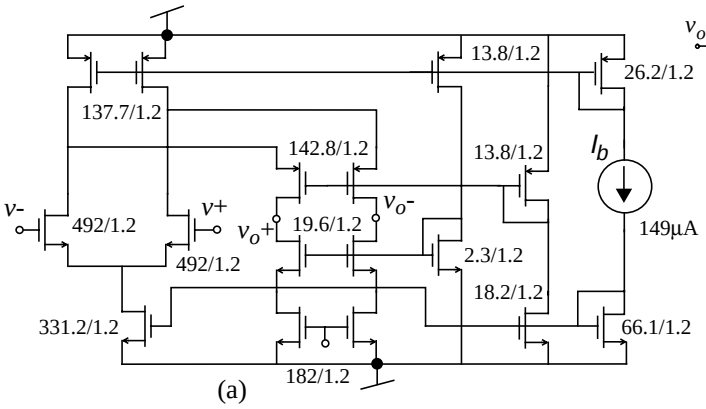


Fig.2 (a) SNDR vs. INL of the DAC; (b) SNDR vs. resolution in presence of capacitor mismatch and integrator leakage.



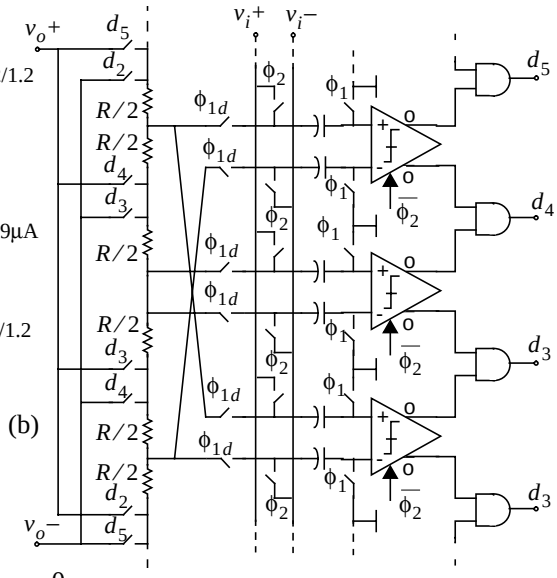


Fig.3 (a) Fully-differential folded-cascode OTA. Sizes for the first-stage amplifier are shown. (b) Three stages of the 3-b flash ADC and R-ladder DAC.

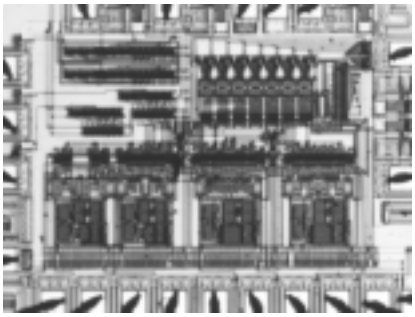


Fig.4 Microphotograph of the ΣΔM chip.

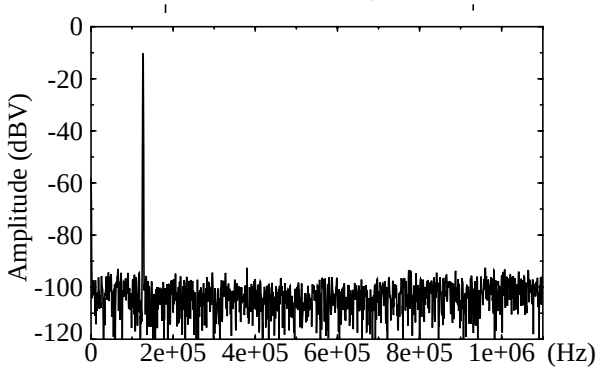


Fig.5 Measured output spectrum.

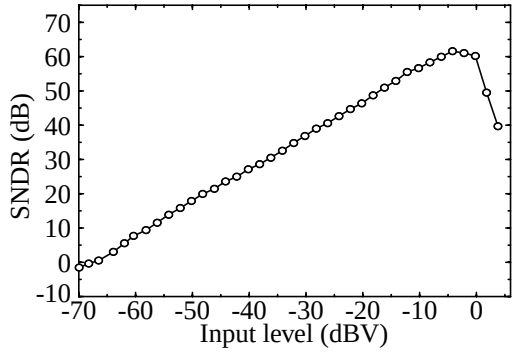


Fig.6 SNDR curve for M=16 and clock rate = 35.7MHz.

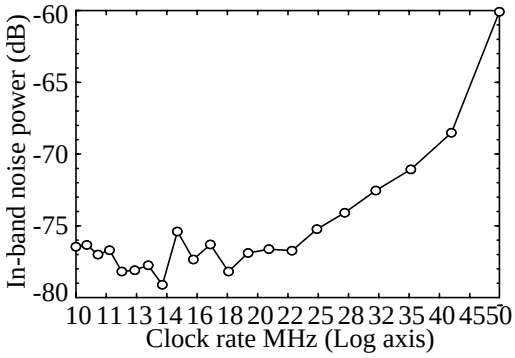


Fig.7 In-band noise (M=16) vs. clock rate.

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