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ELECTRON BEAM INDUCED DAMAGE ON PASSIVATED METAL OXIDE SEMICONDUCTOR DEVICES

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Abstract

Electron beam testing of integrated circuits (IC) is currently based on the electron beam induced conductivity in insulators to short the passivation layer and to enable a voltage measurement at covered conductor tracks. However, applying this technique to passivated MOS devices causes severe radiation damage, which was at first explained by primary electrons penetrating into the deep-lying gate oxide. Nondestructive electron beam testing was expected by using low electron energies that do not allow the primary electrons to reach into the gate oxide.

Therefore here the influence of nonpenetrating electron irradiation on the characteristics of passivated NMOS transistors has been studied. The experiments demonstrate that significant damage is caused even when primary electrons do not reach into the gate oxide. This can be explained by secondary X-rays, generated by the primary electrons in the upper layers, that then penetrate into the gate oxide. Radiation damage increases with irradiation dose, primary energy and with decreasing gate size. Though using the lowest primary electron energy possible to build up the necessary conductive channel, even low irradiation doses alter the devices drastically. Only by blanking off the high energy electron beam at gate oxide areas during the scan, i.e. by application of the window scan mode, is a nearly nondestructive testing of passivated MOS devices via the electron beam induced conductivity made possible. Another possibility to decrease radiation damage is the reduction of primary electron energy to about 1 keV. Then electron beam testing is no longer based on the physics of electron beam induced conductivity, but on the capacitive coupling voltage contrast.

KEY WORDS: Electron beam testing, radiation damage, voltage contrast, passivated metal oxide semiconductor circuits, capacitive coupling voltage contrast, electron beam induced conductivity, window scan mode.

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Introduction

Electron beam testing is mainly applied to nonpassivated devices to shorten the period of development of new very large scale integrated VLSI-circuits [14, 22]. For production inspection at the manufacturer or inspection of goods received at the user, as well as for an IC-internal testing of failures after an application of the device, electron beam testing of the passivated IC is necessary.

The application of existing electron beam test techniques [14] to passivated devices can be realized by using a high energy electron beam. Primary electrons, penetrating the passivation layer, generate electron-hole pairs in the energy dissipation range and thus a region of electron beam induced conductivity is formed in the insulator [18]. If the penetration depth of the primary electrons is at least as large as the passivation thickness, a conducting channel is formed to the covered conductor tracks through the passivation and a voltage measurement is thereby made possible [19]. The necessary energy for the primary electron beam was examined for different passivations [1, 19, 20] and voltage contrast measurements, using the electron beam induced conductivity in insulators, have been successfully realized [4, 20, 22].

When applying this technique to passivated bipolar devices, the necessary electron irradiation did not influence the performance of the bipolar device [4]. However, applying this technique to passivated MOS devices, drastic changes in device parameters were found [10]. The initial explanation for this irradiation damage was that the high energy primary electrons used for testing passivated devices also penetrate the gate oxide layer, where they generate electron-hole pairs. The subsequent trapping of positive holes then causes a change in the space charge. Furthermore, interface states at the gate oxide boundary may be affected. Both effects are responsible for the experimentally found altering of the device parameters [3]. According to this explanation, electron beam testing had been expected to be nondestructive only when primary electron did not penetrate the gate oxide layer [10].

In contrast to these ideas, electron irradiation experiments using low energies (to exclude a

penetration of primary electrons into the gate oxide), were found to cause also radiation damage [7, 15, 16], which, however, is some orders of magnitude less severe than that caused by penetrating electrons [9, 17]. These irradiation effects by nonpenetrating electrons that are useable for electron beam testing of passivated circuits will be investigated in this paper.

Three different ways for electron beam testing excluding a penetration of primary electrons into the gate oxide are taken into consideration: 1. by proper choice of the primary electron energy, which should be adjusted just high enough for the primary electrons to form the necessary conducting channel through the passivation layer to the conductor tracks (10keV for 1.1 µm SiO_2 [2, 20], 2. by application of the "window scan mode" [6], a technique that excludes the high energy electron irradiation of gate oxide regions by automatically switching off of the scanned electron beam with an electron beam blanking system [13], thus creating scan windows that include the gate oxide regions, and 3. by aid of the "capacitive coupling voltage contrast" [5, 8, 14, 21] that is seen at passivated devices when using low energy primary electrons of about 1keV. Irradiation effects caused to MOS-devices by application of each of these three techniques have been experimentally studied in order to find out how severe radiation damages are, to decide whether at least an approximately nondestructive electron beam testing is possible and to determine necessary restictions of electron irradiation for the different techniques.

Experimental

The experiments for evaluating electron beam induced damage on passivated MOS-devices were performed at integrated passivated NMOS transistors. The test structures used consist of several different transistors, the characteristics of which can be measured separately. This enables a simultaneous determination of irradiation effects at all transistors using identical irradidation parameters.

Table 1

The integrated passivated NMOS-transistors used in the electron irradiation experiments (+:symbol consists of type -Enhancement, Depletion, Not doped - gate width / gate length)

No.	symbol+	gate width W / µm	gate length L / µm	typical values of threshold voltage V_{th} / V
0	E 50/10	50	10	1.19
1	E 50/5	50	5	1.00
2	E 10/5	10	5	1.30
3	E 10/50	10	50	1.52
4	D 5/50	5	50	- 5.23
5	E 50/50	50	50	1.37
6	D 50/50	50	50	- 5.98
7	N 50/50	50	50	0.40

A survey of the transistors used in the irradiation experiments gives table 1. They have different dimensions of the polysilicon gate, length and width varying from 5 µm to 50 µm. For the same gate dimensions there are different transistor types, (depending on the doping), exhibiting different values of the threshold voltage.

Fig. 1 shows an SEM micrograph of an enhancement transistor E 50/10 with a polysilicon gate 50 µm wide and 10 µm long (No. 0 in Table 1). The schematic cross section of this transistor is given in fig. 2. The gate oxide was thermally grown on the p-silicon substrate and is 90 ± 5 nm thick. The height of the polysilicon gate is 0.5 µm ± 0.05 µm and the insulating reflow glass is 0.7 ± 0.1 µm thick. The aluminium conductor tracks are 1.0 ± 0.15 µm thick. All the devices are covered with a SiO_2-passivation layer of 1.1 µm ± 0.1 µm thickness.

During the electron irradiation, source, drain, gate and substrate of the transistor were held at ground potential. The electron beam was scanned over the part of the device including the gate oxides of the investigated transistors.

Three different primary electron energies were chosen : 10keV, 5keV and 1keV. The first energy E_{PE} = 10keV is already too low to enable a penetration of primary electrons into the gate oxide layer 2.3 µm deep. But it is just high enough to short the 1.1 µm thick passivation layer for realizing a voltage measurement at the aluminium conductor tracks via the electron beam induced conductivity in insulators. Using the last energy E_{PE} = 1keV the SiO_2 passivation does not charge up negatively; an electron beam testing via the capacitive coupling voltage contrast is possible.

Further irradiation experiments were performed by applying the window scan mode to the test structures. Using this technique the electron beam is switched off during the scan, creating scan windows, which include the gate oxide of the NMOS transistors. Thus, irradiation of gate oxide areas is excluded.

The application of the window scan mode is demonstrated in fig. 3. The gate of the lower transistor is within the scan window (black area), and therefore this gate, in contrast to the one of the upper transistor, is not irradiated during the experiment.

Varying the electron beam current, which was measured via a Faraday cup, the time of irradiation and the size of the scan area the electron irradiation doses ranged from $1.1 \cdot 10^{-7}$ As/cm^{-2} to $2.7 \cdot 10^{0}$ As/cm^{-2}. After each irradiation the characteristics of the transistor were measured: the drain source current I_{DS} as a function of the drain source voltage U_{DS} with the gate source voltage U_{GS} as parameter; and as a function of the gate source voltage U_{GS} with the drain source voltage U_{DS} as parameter. Because of the multitude of measurements for different transistors and after different electron irradiations, determination of the characteristics was automated. With the voltage given by D/A-converters and the current

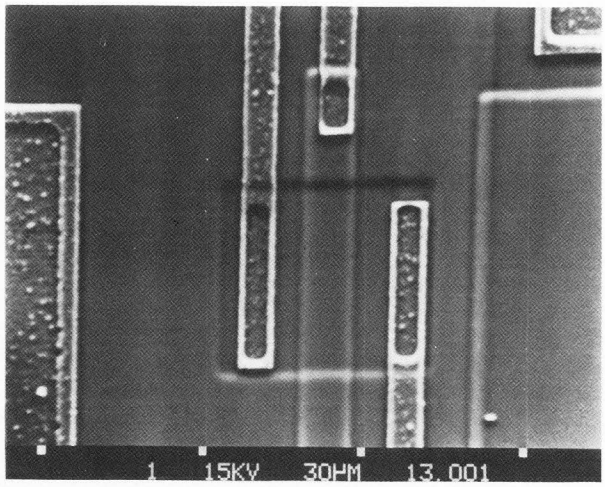

Fig. 1: SEM micrograph of an enhancement NMOS transistor, gate width: 50 µm, gate length: 10 µm (No. 0 in table 1).

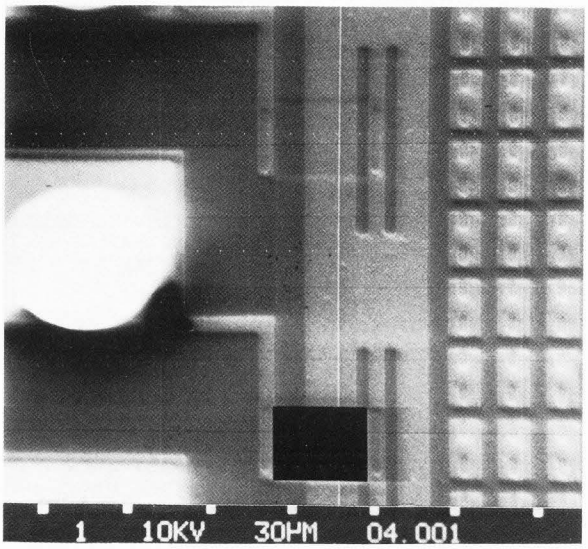

Fig. 3: SEM micrograph of two NMOS transistors; the 50 µm x 50 µm gate of the lower one is not irradiated by applying the window scan mode.

measured via an electrometer connected to a computer all characteristics could be measured and stored. Changes in the characteristics due to electron irradiation were examined afterwards. For example, as the drain source current I_{DS} is proportional to $(U_{GS}-V_{th})^2$, the threshold voltage V_{th} was determined by linear regression of the $(\sqrt{I_{DS}}=f(U_{GS}))$-characteristics. The measurements of the characteristics were performed with the test structure remaining in the specimen chamber of the electron beam test system [12], thus avoiding unintentional changes of the irradiation.

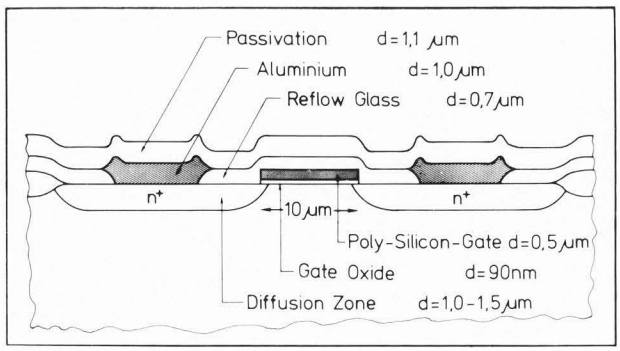

Fig. 2: Schematic cross section of the NMOS transistor of fig. 1.

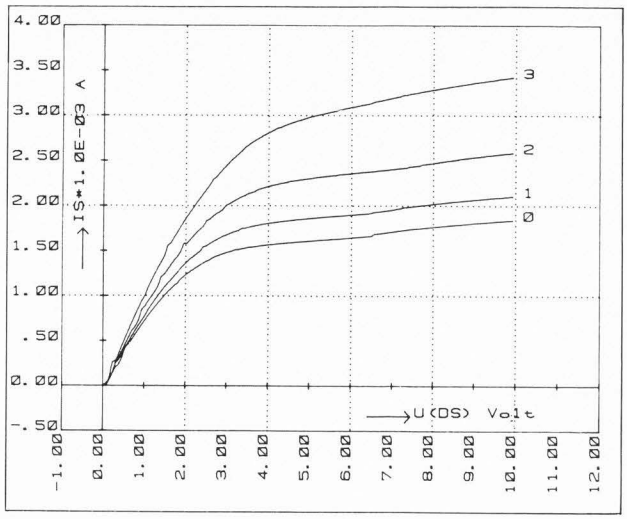

Fig. 4: Change in $(I_{DS}-U_{DS})$-characteristics of a NMOS transistor (E 50/5) due to different irradiation doses D of 10keV electrons: $D_0=0$ C/cm^2, $D_1=0.67\cdot10^{-4}$ C/cm^2, $D_2=3.7\cdot10^{-4}$ C/cm^2, $D_3=12.\cdot10^{-4}$ C/cm^2 ($U_{GS}=6$ V).

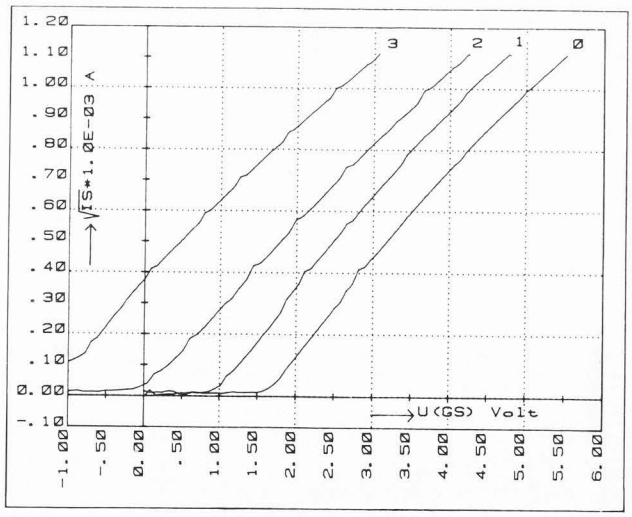

Fig. 5: Negative shift of $(\sqrt{I_{DS}}-U_{GS})$-characteristics of a NMOS transistor (E 50/5) due to different irradiation doses D of 10keV electrons: $D_0=0$ C/cm^2, $D_1=1.2\cdot10^{-4}$ C/cm^2, $D_2=3.7\cdot10^{-4}$ C/cm^2, $D_3=12.\cdot10^{-4}$ C/cm^2 ($U_{DS}=4$ V).

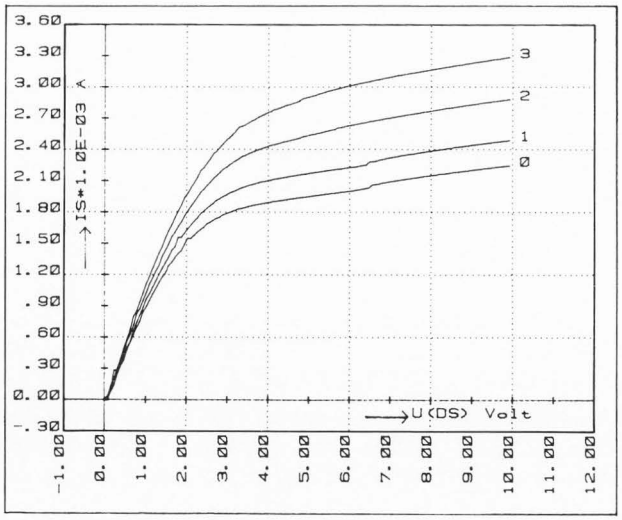

Fig. 6: Change in (I_{DS}-U_{DS})-characteristics of an NMOS transistor (E 50/5) due to different irradiation doses D of 1keV electrons: D_0=0 C/cm^2, D_1=0.54 C/cm^2, D_2=1.5 C/cm^2, D_3=2.7 C/cm^2(U_{GS}=6V).

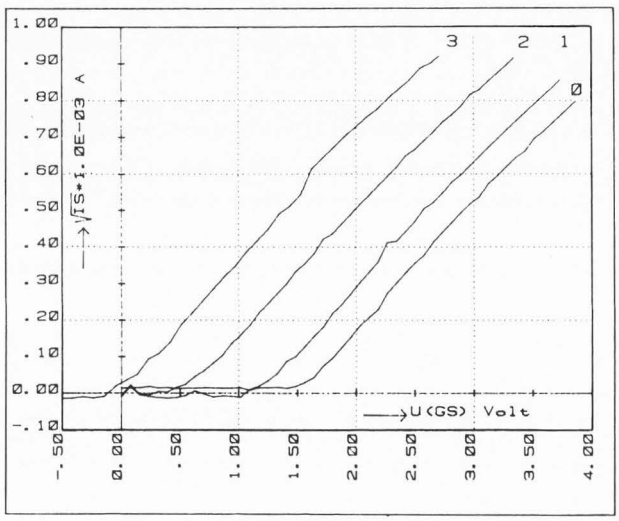

Fig. 7: Negative shift of ($\sqrt{I_{DS}}$-U_{GS})-characteristics of an NMOS transistor (E 50/5) due to different irradiation doses D of 1keV electrons, D_0=0 C/cm^2, D_1=0.54 C/cm^2, D_2=1.5 C/cm^2, D_3=2.7 C/cm^2 (U_{DS}=4V).

Results

The irradiation effects of 10keV primary electrons on an enhancement transistor E 50/5 are shown in fig. 4 and fig. 5. The changes in the (I_{DS}-U_{DS})-curve for a gate source voltage U_{GS}=6V and the negative shifts of the ($\sqrt{I_{DS}}$-U_{GS})-curve for a drain source voltage U_{DS}=4V are shown for four electron irradiation doses, respectively. With the curve index 0 to 3 referring to irradiation doses D=0, $0.67\cdot10^{-4}$C/cm^2, $3.7\cdot10^{-4}$C/cm^2 and $12\cdot10^{-4}$C/cm^2, it is found that the drain source current increases drastically due to the electron irradiation (fig.4).The saturation current has enlarged by a factor of about two and the slope in the saturation region has also risen. In fig. 5, a nearly parallel shift of the ($\sqrt{I_{DS}}$-U_{GS})-curve is shown for the irradiation doses D=0, $1.2\cdot10^{-4}$ C/cm^2, $3.7\cdot10^{-4}$ C/cm^2, and $12\cdot10^{-4}$ C/cm^2, referring to the curve indices 0 to 3. The electron irradiation leads to a negative shift of the threshold voltage V_{th}.

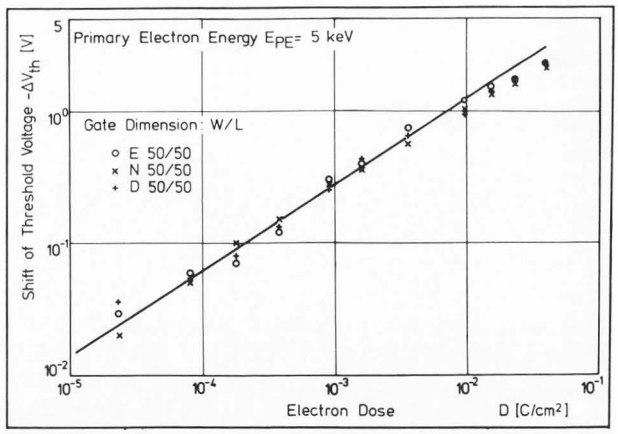

Fig. 8: Shift of threshold voltage as a function of electron irradiation dose for different types of NMOS transistors with equal gate dimensions.

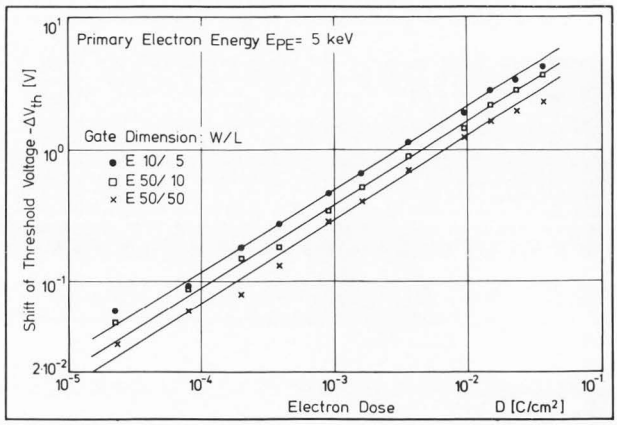

Fig. 9: Shifts of threshold voltage as a function of electron irradiation dose for enhancement NMOS transistors with different gate dimensions.

Similar results were found for irradiation with electrons of lower primary energies. This is demonstrated for 1keV primary electrons at the same transistor E 50/5 in fig. 6 and fig. 7. Fig.6 shows the same changes in the (I_{DS}-U_{DS})-curve for 1keV as found for 10keV shown in fig. 4; fig. 7 shows the same negative shift in the ($\sqrt{I_{DS}}$-U_{GS})-curve for 1keV as found for 10keV shown in fig. 5. However, the electron irradiation doses causing these effects are 0, 0.54, 1.5 and 2.7 C/cm^2 referring to the curve 0 to 3, respectively, which means that the doses for 1keV electrons are four orders of magnitude higher than for 10keV electrons.

The negative shifts of the threshold voltage increase with the irradiation dose and the primary electron energy. There also is a dependence on the

transistor irradiated: the threshold shift depends on the gate dimensions, but not on the type of transistor. The latter is demonstrated by fig. 8 for the irradiation with 5keV primary electrons. Using a logarithmic axis for the shift of threshold voltage $-\Delta V_{th}$, and the electron dose D all measured points are found on the same straight line for all of the three different types of transistors with a square gate 50/um x 50/um. Depending on the doping level, the threshold voltages of the unirradiated transistors are V_{th} (E 50/50)= 1.37V, V_{th} (D 50/50)= -5.98V and V_{th}(N 50/50)= 0.40V (see table 1). For all three types of NMOS transistors the same shift in the threshold voltage is found.

The relationship between the irradiation effects and the gate dimension is shown in fig. 9. For three enhancement transistors of different gate dimensions (E 10/5, E 50/10 and E 50/50) the negative shifts of threshold voltage are plotted as a function of the irradiation dose with 5keV primary electrons. All measured points are found on straight lines parallel to each other. The smaller the gate dimensions are, the higher the effect due to irradiation.

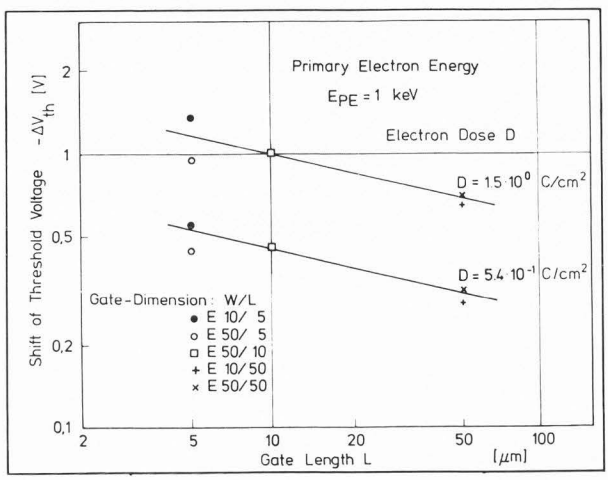

Fig. 10: Effect of the gate dimensions on the shifts of the threshold voltage for different irradiation doses with 1keV electrons.

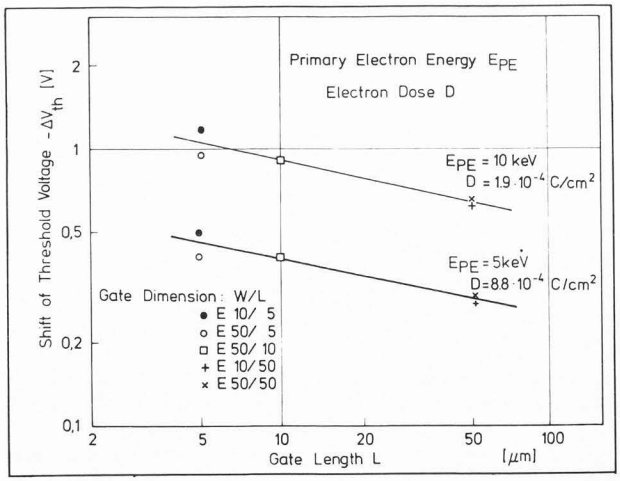

Fig. 11: Effect of gate dimensions on the shifts of the threshold voltage for different primary electron energies.

The effect of gate size on the sensitivity of NMOS transistors to electron irradiation is demonstrated in fig. 10 and fig. 11. The first one shows the shift of the threshold voltage as a function of the gate length for two electrons doses using a primary energy of 1keV. The five transistors exhibit the same dependence for both doses. With decreasing gate length the shifts of threshold voltage increase. There is also a tendency on the gate width. However, an opposite relationship is found, as the width is increased from 10/um to 50/um for a gate length of 5/um (E 10/5; E 50/5) and for a gate length of 50/um (E 10/50; E 50/50), respectively. For an explanation further experiments are necessary.

The same dependence on the gate dimensions, as shown in fig. 10 for 1keV primary electrons at different doses, is also found for other primary energies. As an example, in fig. 11 the shift in the threshold voltage as function of the gate length is shown for the primary energies of 10keV and 5keV, after irradiation with doses of $1.9 \cdot 10^{-4}$ C/cm^2 and $8.8 \cdot 10^{-4}$ C/cm^2, respectively. In spite of the lower dose the effect of 10keV electrons is higher, but the dependence of the shift in the threshold voltage on the gate dimensions is the same for both primary energies.

The shift in threshold voltage of the E 50/5 transistor after electron irradiation is shown in fig. 12 for three primary electron energies. As already seen by comparison of Figs. 4 and 5 with 6 and 7, low primary electron energies cause less radiation damage. The same shift of the threshold voltage, caused by irradiation using 10keV electrons, is found at about 20 times higher doses of 5keV electrons and about 10000 times higher doses of 1keV electrons. Since the experimentally determined straight lines are only shifted along the dose axis the dependence of the shift of the threshold voltage on the electron dose remains the same. By reducing the primary electron energy irradiation damage lessens over-proportionally.

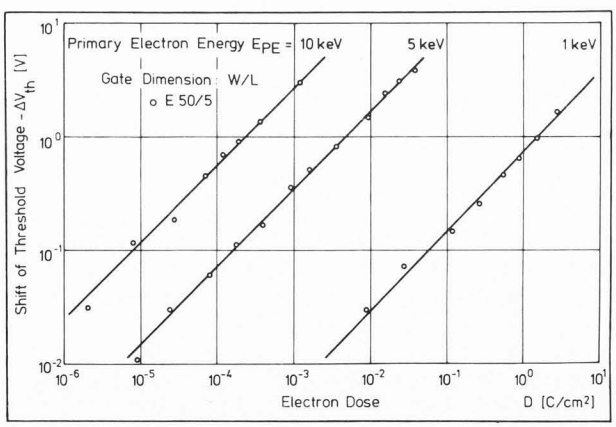

Fig.12: Shifts of threshold voltage of an NMOS transistor (E 50/5) as a function of electron irradiation dose for different primary electron energies.

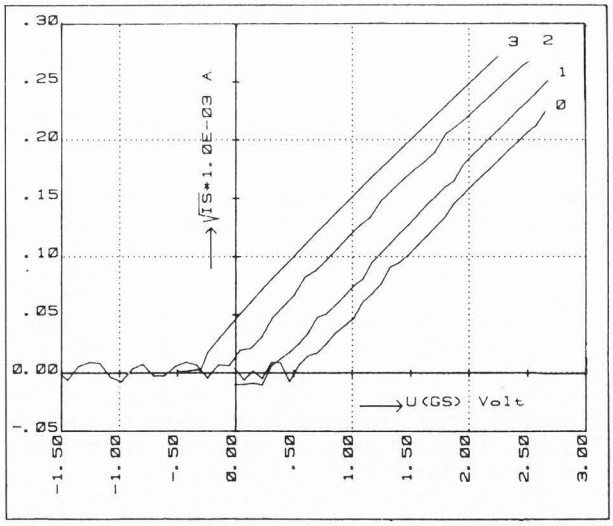

Fig. 13: Shift of $(\sqrt{I_{DS}}\text{-}U_{GS})$-characteristics of an NMOS transistor (E 50/50) due to different irradiation doses using the normal mode. D_0=0 C/cm^2, D_1=6.7·10^{-5} C/cm^2, D_2=1.9·10^{-4} C/cm^2, D_3=3.7·10^{-4} C/cm^2.

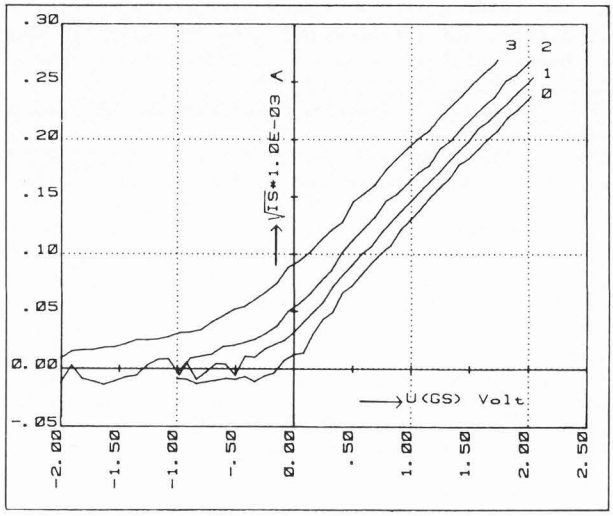

Fig. 14: Shift of $(\sqrt{I_{DS}}\text{-}U_{GS})$-characteristics of an NMOS transistor (N 50/50) due to different irradiation doses using the window scan mode. D_0=0 C/cm^2, D_1=1.1·10^{-2} C/cm^2, D_2=2.2·10^{-2} C/cm^2, D_3=4.4·10^{-2} C/cm^2.

Another possibility to minimize radiation damage, beside reduction of the primary electron energy, is the application of the window scan mode. This technique has already been demonstrated in fig. 3, where the gate of an N 50/50 transistor was within the scan window, and therefore not irradiated, whereas an E 50/50 transistor was totally exposed.

The results of such an irradiation experiment are shown in fig. 13 and fig. 14. Shifts in the $(\sqrt{I_{DS}}\text{-}U_{GS})$-curve are found in the normal mode (fig. 13) as well as in the window scan mode, but here only at doses about two orders of magnitude higher. However, beside the shift of the $(\sqrt{I_{DS}}\text{-}U_{GS})$-curve, an increase of leakage current is found (see I_{DS} for negative U_{GS} values). Furthermore, radiation damage depends on the size of the used scan window, as demonstrated in fig. 15. Here the shift of threshold voltage is shown as a function of irradiation dose. Using a scan window equal to the gate size, radiation damage is diminished by a factor of about 130, and using a scan window twice the size the factor increases to 600. These experiments show that the application of the window scan mode offers a possibility for both reducing radiation damage and using the electron beam induced conductivity for measurements at covered conductor tracks.

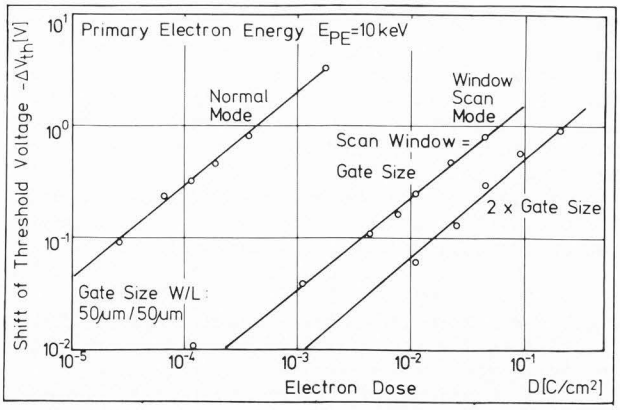

Fig. 15: Reduction of electron irradiation damage by application of the window scan mode.

Discussion

Electron irradiation causes significant radiation damage to passivated MOS devices, even when the primary electrons do not reach the gate oxide layer. The determined radiation damage, measured as negative shifts in the threshold voltage of NMOS transistors, depends on parameters of both the electron irradiation used and the MOS devices tested.

The shifts in threshold voltage increase with irradiation dose and primary energy, and they are more severe for smaller gate dimensions but independent of the transistor type, determined by the doping level. As the dependences of radiation damage on dose and on gate size are the same for different primary energies -(i.e., in fig. 12 and fig. 11 a change in the primary energy just results in a parallel shift of the graph along the voltage or dose axis, respectively)- it is believed that the same physical mechanism is responsible for the measured irradiation effects, even for those caused in the window scan mode (see fig. 15). Several mechanisms may be supposed:

- The commonly used electron dissipation range after Everhart and Hoff [2] does not take into account a very small but not vanishing amount of electrons beyond the nominal electron range, that may reach into the gate oxide layer and cause the irradiation effects as discussed in the initial model.
- On their way through the upper layers of the MOS device the primary electrons generate secondary radiation, for example secondary electrons, ions or X-rays. X-rays especially, having a long enough

range, can penetrate the gate oxide and thereby change the space charge and interface states [17]. - The electron irradiation can charge up the upper isolation layers and by this mechanism the charge balance of the MOS transistor may be affected.

However, as the experiments show the same dependences for the normal mode and for the window scan mode as well as for charging (E_{PE}=5 keV) and noncharging energies (E_{PE}=1 keV, 10 keV), the first and the last mechanism have to be excluded, respectively. The only mechanism, being able to explain what has been experimentally found, is the second mechanism of X-ray generation, which can be expected for all primary energies used. Furthermore X-rays can even penetrate from outside the gate area into the gate oxide layer, as necessary for comprehending the results in the window scan mode, with the gate area blanked out.

The irradiation experiments using 10 keV primary electron energy, the lowest energy possible to short the passivation layer for electron beam testing via the electron beam induced conducting channel, showed that electron doses above $10^{-4}C/cm^2$ give rise to severe radiation damage, i.e., as high voltage resolution calls for high electron beam currents of some 10^{-8} A, drastic changes of MOS transistor characteristics are caused even at low magnifications of about 100 in a few seconds of irradiation. The application of the window scan mode reduces radiation damage drastically by some orders of magnitude, depending on the size of the scan window, thus enabling a nearly nondestructive electron beam testing. Radiation effects are found for all primary energies used, even for such low energies as 1 keV. However, if the primary energy is just decreased from 10 keV to 1 keV, 10^4 times higher doses are acceptable, which means that electron beam testing of passivated MOS devices via the capacitive coupling voltage contrast using such low energies is approximately nondestructive.

Conclusions

Electron irradiation experiments of NMOS transistors demonstrated that electron beam induced damage is caused even when the energies are too low to enable the primary electrons to penetrate into the gate oxide layer, and even when the area of the gate oxide itself is not irradiated. These results can only be explained by secondary X-rays which are generated in a first interaction of the primary electrons in the upper layer and then penetrate into the gate oxide layer, where in a second interaction they affect the space charge and the interface states, resulting in the experimentally found changes of the MOS devices. The initial model, explaining radiation damage by ionisations in the gate oxide by penetrating primary electrons, therefore has to be enlarged for non-penetrating primary electrons by an additional interaction.

The experiments have shown that successful electron beam testing of passivated MOS devices via the conductive channel solely by proper choice of the primary electron energy, (even if a penetration of primary electrons into the gate oxide is avoided), has to be excluded because of severe radiation damage. A reduction of radiation damage is possible either by application of the window scan mode or by use of the capacitive coupling voltage contrast. The first technique requires sophisticated automated equipment to exclude irradiation of gate oxides by switching off the high energy electron beam during the scan [6]. The second technique simply uses a low energy electron beam of about 1 keV to reduce irradiation effects, but then only alternating IC-internal signals can be investigated [5, 8, 11, 21] . Both of the techniques offer the possibility of an approximately nondestructive electron beam testing of passivated MOS devices.

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Discussion with Reviewers

M. Miyoshi: Irradiation effects of MOS structures strongly depend on the property of gate oxide and the interface state density. What kind of gate oxide (method or characteristics) did you use in this experiments?
Authors: The gate oxide is thermally grown on the p-Si-substrate in a standard polisilicon gate NMOS process.

S.P. Shea: Is it possible to quantify, at least in a relative sense, your theory that X-ray generation by the primary electron beam is responsible for the damage to the devices which you have studied? Specifically, could you calculate the relative number of ionization events in the gate oxide due to X-rays, as a function of the energy and position of the electron beam?
Authors: Yes, it is possible to calculate the X-threshold voltage shifts, found in experiment, as a function of electron irradiation dose and primary electron energy. However, for nonpenetrating primary electrons and the mechanism via secondary X-rays these calculations are rather complex, as the generation of the X-rays by primary electrons of different energies, the penetration of different X-rays through the layers of the NMOS-transistor, the absorption of these X-rays in the gate oxide layer and the resulting threshold voltage shift due to the changed space charge have to be considered. Therefore, in this paper, we did no calculation, but discussed several mechanism possible, and by excluding the others, the mechanism via secondary X-rays is the only one that explains, what has been found in experiment. A rough estimation of this mechanism via secondary X-rays was already given by Nakamae et al (see ref.17).

H. Fujioka: What is the difference between your results on electron beam irradiation effects and the results obtained by Nakamae et al. (1981) and Miyoshi et al. (1982)?
M. Miyoshi: What is the difference between results of ref. 16 and ref. 17 and your results?
Authors: Nakamae et al. (ref. 17) described irradiation effects on a passivated NMOS transistor using primary electrons of 5keV - 18keV. They showed that there is radiation damage even when the Everhart and Hoff range of the electrons used is smaller than the distance between the gate oxide layer and the surface. They explained that this irradiation damage may be due to the effect of range straggling or secondary X-ray radiation. However, consequences for the different electron beam testing techniques at passivated MOS devices were not discussed.

In ref. 16 Miyoshi et al. discribed irradiation experiments using low primary energies of 1-3keV, but at nonpassivated NMOS and PMOS transistors. They also concluded that secondary X-rays may be responsible for this kind of radiation damage. Furthermore they found that radiation damage increases for smaller channel length.

In this paper irradiation effects are especially examined with regard to electron beam testing of passivated MOS devices. Therefore passivated NMOS transistors were irrediated under different conditions, which are typical for different ways of electron beam testing of passivated devices, i.e. for applying the electron beam induced conductivity, the window scan mode and the capacitive coupling voltage contrast. Thereby on the one hand the results of ref. 16 and 17 are confirmed and on the other hand the results are extended to lower energies for passivated devices and for the application of the window scan mode. Furthermore, the necessary restrictions of electron irradiation for different electron beam testing techniques are discussed.

S.P. Shea: Please, explain the kind of test discussed in the text and discribe how a voltage measurement is made.

Authors: Electron beam testing is based on the voltage contrast in the SEM. Those parts of the IC having a positive voltage appear dark in the secondary electron picture, those having a negative voltage appear bright. By application of a secondary electron spectrometer and a linearisation feed back this effect can be used for IC-internal quantitative voltage measurement. This is described in detail in ref. 14 and 23 (see below). The application of this technique is demonstrated in ref. 4, 20, 22.

However, when applying this technique not to nonpassivated but to passivated devices, the problem of charging of the passivation arises. In principle two ways are possible then : using a high primary electron energy to short the passivation (see ref. 1, 19, 20) or a low primary electron energy with an electron yield $\sigma > 1$ of the passivation, establishing the capacitive coupling voltage contrast (see ref. 5, 8, 11, 21).

Additional Reference

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