Scanning Electron Microscopy

Volume 1985
Number 1 *1985*

Article 6

9-6-1984

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SCANNING ELECTRON MICROSCOPY/1985/I (Pages 55-66)
SEM Inc., AMF O'Hare (Chicago), IL 60666 USA

0586-5581/85$1.00+.05

ADVANCES IN ELECTRON-BEAM-INDUCED-CURRENT ANALYSIS OF INTEGRATED CIRCUITS

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(Paper received March 18 1984, Completed manuscript received September 6 1984)

Abstract

Electron-beam-induced-current (EBIC) analysis of integrated circuits and of individual semiconductor devices has become an essential technique for semiconductor device characterization as well as for failure analysis and diagnostics. This tutorial is an update of the paper presented in SEM/1981/I on the same topic and discusses advances and new trends in the applications of EBIC in recent months. Examples of EBIC measurements on high density chips, ion-implanted junctions, and shallow diffusions in thin epitaxial layers are given. Time resolved EBIC (TREBIC) is also explained and new digital readout techniques, including computer-aided data analysis, are described as they refer to detailed analyses of depletion regions associated with P-N junctions.

KEY WORDS: Electron Beam Induced Current, EBIC, Integrated Circuits, Depletion Width, P-N Junction, Scanning Electron Microscope, Failure Analysis.

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Introduction

A familiarity with the previous paper [15] will be assumed in the presentation of this paper. EBIC analysis of semiconductor devices is becoming of greater interest as analyzers need to locate a particular electrical defect [5,14] and to characterize electrically and physically a particular transistor or junction [9]. Either of these needs can be met using high resolution electron beam techniques, and measurements of beam-induced currents often result in a solution to the analytical problem or to other physical analyses for a solution to a processing problem [11,12].

The electron beam/semiconductor interaction is important here, and let us consider some aspects of this interaction. The generation of free carriers within the semiconductor, the behavior of these carriers, and their subsequent collection (hence the often-used term "charge collection microscopy") ultimately lead to results that contain electrical information about the samples. When an electron beam of from 1 to 50 keV strikes a semiconductor material, the generated carriers, hole-electron pairs, diffuse randomly throughout the bulk material with a diffusion constant, D (D_n for electrons and D_p for holes). The minority carrier diffusion length, L, is written: $L = \sqrt{D\tau}$, where τ is the minority carrier lifetime. This lifetime is an important parameter when discussing semiconductor materials and devices. The lifetimes are in the range of 10^{-3} to 10^{-6} seconds for most semiconductors. During diffusion, recombination of oppositely charged carriers occurs usually at recombination centers in the crystal. The frequency of recombination depends on the capture cross section, s, of the center for the carrier, and the density of centers, N. The lifetime may then be written: $\tau = (sNv)^{-1}$, where v is the thermal velocity of the carrier. In N-type silicon the excess minority carriers, Δp, will have a recombination rate, R, of $\Delta p/\tau$. The steady state conditions for generation and recombination of carriers in a homogeneous sample may be written:

$$g - (1/q)\nabla \cdot J_p - \Delta p/\tau = (d\Delta p)/dt = 0 , \quad (1)$$

where g is the generation rate for electrons and holes. The carriers may be removed by drift motion or diffusion of flux J, and recombination rate is controlled by minority carrier recombination. The local rate of carrier pair generation may be written [7]:

$$g(r,z) = G(E_b I_b (1-f))/(E_{np})q \quad , \qquad (2)$$

where G is the distribution of carriers generated by an electron beam of energy, E_b, and current, I_b, perpendicular to the semiconductor surface and normalized to the electron range in the material, f is the fraction of the electron beam energy reflected by the sample, and E_{np} is the energy necessary to create a hole-electron pair in the material. Various workers [6] have computed Δp and have shown the relationship between L,s and g(z).

In a P-N junction of a Schottky barrier diode junction, there is a zone depleted of carriers, that is, a depletion region formed by oppositely charged sites on the two sides of the junction. The resulting field distribution is a maximum at the true electrical P-N junction and extends into the material on either side. If the material is very highly doped on one side of the junction approximating a step junction, the depletion width, W, of the junction may be written:

$$W = ((2\,\varepsilon_s/qN_d)(\emptyset + V_r))^{(1/2)} \quad , \qquad (3)$$

where ε_s is the product of the dielectric constant and the permittivity of free space and $\emptyset$ is the junction potential. The earlier paper [15] illustrated the relationship between W and the reverse bias, V_r, of a Schottky barrier diode as measured by EBIC. The depletion region and depletion width are important properties to the device physicist, since they determine the electrical properties of both active and passive devices in integrated circuits, such as transistor current gain, leakage currents, threshold voltages and switching times. A better value for the depletion width is obtained from the solution to the defining expression in its exact form, that is

$$W = ((2\varepsilon_s/qN_d)(\emptyset - (2kT/q)))^{(1/2)} \quad , \qquad (4)$$

N_d is used for P-type silicon, but N_a would be used for N-type silicon. This expression includes the "tail" portions of the depletion region where the true carrier distribution is accounted for. Values for W are obtained by capacitance measurements, where the capacitance per unit area, C, is defined by:

$$C = dQ/dV = d(qN_dW)/d((qN_d/2\varepsilon_s)W^2) \quad , \qquad (5)$$

and

$$C = ((q\varepsilon_s N_d)/2)^{(1/2)}(\emptyset \pm V-(2kT/q))^{-(1/2)}, \qquad (6)$$

It can be shown that [16]:

$$d(1/C^2)/dV = 2/(q\varepsilon_s N_d) = 2/(q\varepsilon_s NW) \quad , \qquad (7)$$

and capacitance/voltage curves can be used to obtain accurate depletion layer widths, within one Debye length (approximately 300 Å for silicon, $N = 10^{16}$ cm^{-3}). These measurements would be made on large area (area = 1×10^{-4} cm^2) devices, but for small devices (area = 1×10^{-7} cm^2), edge effects dominate, and capacitance measurements may not be used to determine W. EBIC measurements may be used to obtain depletion widths on small devices, and, also, variations in W over the area of a device may be determined by using EBIC techniques.

Time Resolved EBIC (TREBIC)

Recently, workers have reported measurements of Time Resolved EBIC [2,8] in which a pulsed electron beam is used. This technique measures the zero delay component of the junction transient response, thus minimizing the contributions of minority carrier diffusion to the collected current. An advantage is improved spatial resolution in the determination of junction depths from the top surface of the junction.

Figure 1 shows a comparison of an EBIC line scan made across the edge of a diffusion to a TREBIC line scan made at the same location [8]. The junction depth is 2.92 μm and the beam energy is 17 keV. The full width at half maximum of the EBIC scan is 5.0 μm and of the TREBIC scan is 3.5 μm. The sampling gate width used was 100 psec (see Fig. 2) for the TREBIC scan, while the experimental steady state curve was used for the EBIC trace. The lateral contributions of the diffusion process can be seen on the EBIC trace. Certain authors [2,8] describe a current gain as:

$$G(E_b) = ((1-f)E_b/E_{np})(S_B/S_A) \quad , \qquad (8)$$

where S_B and S_A are the signal amplitudes inside and outside the diffusion, respectively.

Experimentally, the TREBIC technique requires chopping the electron beam. This is accomplished in various ways, the most popular of which uses electrostatic plates that deflect the beam across a knife edge or across an aperture in the electron gun region. Another method [10] is to pulse the high voltage (grid voltage) at the Wehnelt grid of the electron gun. The former method can produce chopping times of less than 1 nsec, while the latter can produce chopping times of approximately 2 nsec. The output of the current amplifier measuring the beam-induced current is fed into a sampling head triggered by the pulse generator driving the beam chopper. A typical sampling duration is 100 psec., and the junction measured is usually reverse-biased to increase the signal. This reverse bias may prevent the use of TREBIC measurements on certain devices of interest.

Applications Of EBIC

EBIC measurements in failure analysis and device diagnostics fall into two groups. One type of analysis involves locating a defective device in a circuit or an array, locating a defect in a device or junction, or locating an irregularity in a junction [1]. These might lead to further analysis using other techniques. The other type of EBIC analysis involves measuring depletion widths, junction depths, channel lengths, or in some way utilizing the EBIC signal to characterize the device of interest [3]. Of these two types of EBIC analyses, the former seems to be in wider use for several reasons. The densities of devices in a circuit are typically thousands of devices, and there may be one or two defects in this large number. The few defects must be located and analyzed. An advantage to using EBIC for locating defects is that very often no sophisticated interpretation of the resulting EBIC micrograph is necessary to find a defect or irregularity. A simple comparison between a good circuit and a bad circuit viewed in the EBIC mode may be adequate, with little attention being given to resolution, generation current gain, scanning rates, beam voltage, etc. These latter concerns become important when making careful quantitative determinations regarding the EBIC signal and its relationship to a desired parameter.

Sample Preparation

Regardless of the type of EBIC analysis being performed, the sample must be prepared properly in order to achieve meaningful results. A deposited conductive coating may not be used. The coating would short together the electrical components of the sample being measured. Reliable electrical contact must be made to the circuit, device, or junction of interest. This may be accomplished before or after the specimen is placed in the vacuum system of a scanning electron microscope (SEM). Since a large portion of the sample may be dielectric (SiO_2, Al_2O_3, Cr_2O_3, Si_3N_4) or organic polymers, the secondary electron emission image may be altered due to charging except to the extent that the primary beam may be deflected or the junction may be altered in the area of the accumulated charge. This might be the case in a field effect transistor (FET) where the gate metal is left open. Both of these effects are possible, but should be reduced since operating beam voltages of less than 3 keV are not uncommon for EBIC studies.

Electrical contact is provided by probing or wire bonding as in the past. Some new capabilities involve incorporating a versatile probing capability inside the SEM chamber. Figure 3 shows one such system where two probes are mounted on motor driven stages such that the probes may contact any site on the sample once the sample is in the chamber. In this scheme, the area of interest on the chip is noted, and coordinates are assigned to all sites of interest (pads, devices, lines, diffusions, contacts). The sample is then placed in position for the EBIC measurement desired at the appropriate magnification. The probes are then sent under computer control to contact any site for the desired measurement. In this way, the specimen need not be moved and contact can be achieved outside the field of view of the SEM.

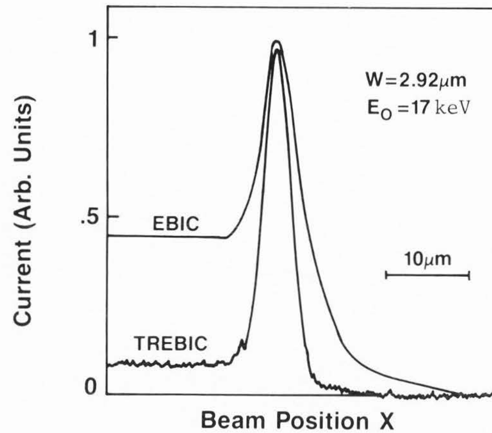


Figure 1. Comparison of a normal EBIC line scan with a TREBIC line scan across a P-N junction at the edge of a diffusion which is 2.92 μm deep. The beam energy is 17 keV.

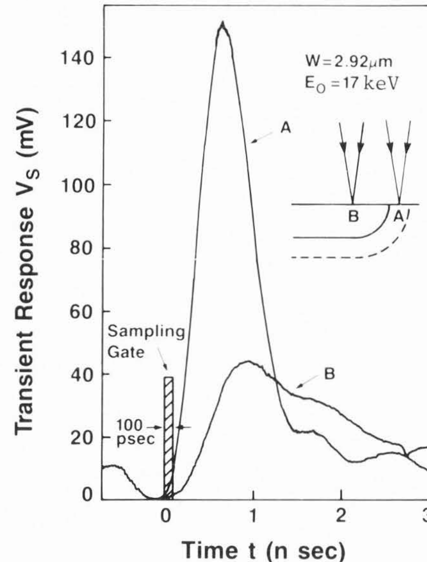


Figure 2. Transient EBIC signals collected from a diffusion with the electron beam at two different locations.

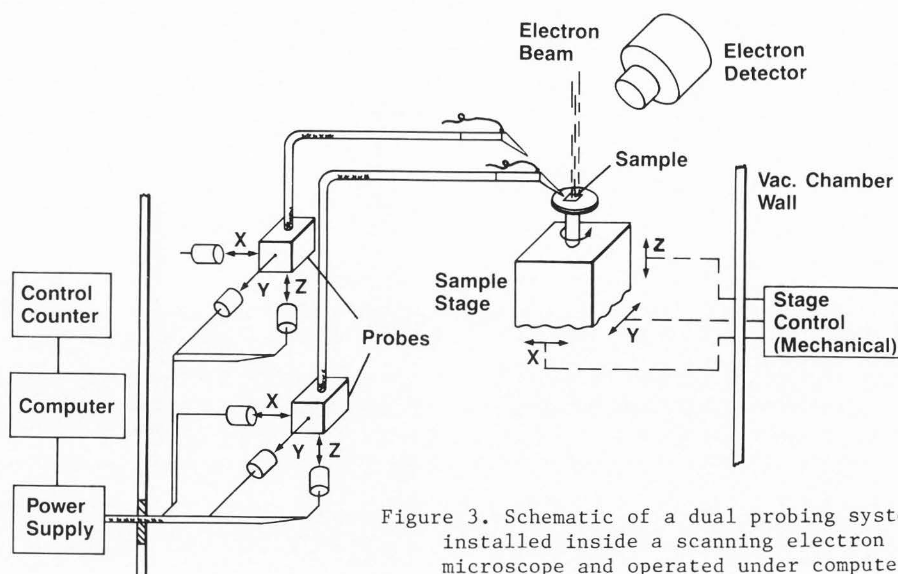


Figure 3. Schematic of a dual probing system installed inside a scanning electron microscope and operated under computer control.

Locating Defects By EBIC

Locating defects by EBIC includes locating a defective device in a large number of devices as well as locating a defect somewhere in a single device. In locating a defective device in a group or array of devices connected together, it is often unnecessary to anticipate the desired electrical result. An example of this is the location of a piped transistor (a pipe is a collector-to-emitter short through the base) in a group of transistors all of which are connected in parallel to the pads. Dominicucci and Karcher [4] demonstrated this analysis and found that the transistors with pipes appeared darker in an EBIC micrograph made by connecting all of the emitters in parallel to the input of the current amplifier and the substrate of the circuit to amplifier ground. Figure 4 shows a micrograph where the defective transistor is located. Notice that this technique does not locate the pipe or the cause for the pipe, but simply points out the piped transistor in a large number (320 in this case) of transistors. The electrical connection is shown schematically in Fig. 5. The EBIC signal from the piped transistor is dominated by the collector-to-isolation junction current since the pipe allows contact to the collector through a resistive path (R_{pipe}) instead of by back-to-back junctions as in the good transistor. The beam voltage for this measurement was 20 keV at a beam current of 10 nA.

An example of locating a defect in a single device is the analysis of Schottky barrier diodes (SBD) in our laboratory. In this work, the defective diode was a discrete device that had been isolated from the peripheral circuitry by laser isolation, and an individual diode could be connected in the scanning electron microscope (SEM) for EBIC measurements. The diode exhibited reverse leakage and a forward electrical characteristic of a localized parallel diode (see Fig. 6). A normal EBIC micrograph of a good diode, with the anode connected to the amplifier input and the cathode connected to ground, is shown in Fig. 7. The diode was a platinum silicide SBD with aluminum-copper metallurgy and the beam voltage was 10 keV. The secondary emission micrograph of the same good diode in Fig. 8 shows the bright copper-rich grains in the metallurgy. These grains reduce the beam penetration into the junction region, thus resulting in a decreased EBIC signal at each grain. Figure 9 shows the EBIC micrograph obtained with a 50 mV reverse bias applied to a defective diode supermiposed on the secondary emission micrograph. With the slight reverse bias applied, the highly localized increased field produces a much greater signal at the defect. Subsequent analysis of this and other similarly defective diodes revealed a localized discontinuity in the PtSi film at the EBIC defect site. This allowed contact between the silicon and elements of the other metallurgy (Cr, Al, or Cu). Figure 10 shows a series of EBIC micrographs of another defective diode taken at various reverse bias voltages. This defect is not as small as the former one, but it becomes apparent at lower bias. These micrographs are made using the EBIC current amplifier ac-coupled so that a dc bias may be applied across the device without affecting the grey level of the amplifier.

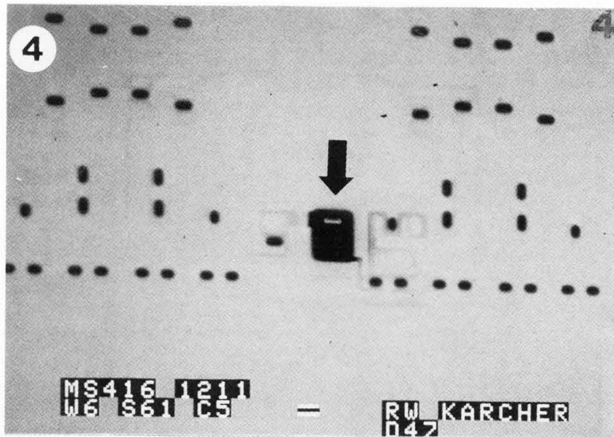


Figure 4. EBIC location of a piped transistor in a 320-transistor array connected in parallel. Bar = 10 μm. (Ref. 4.)

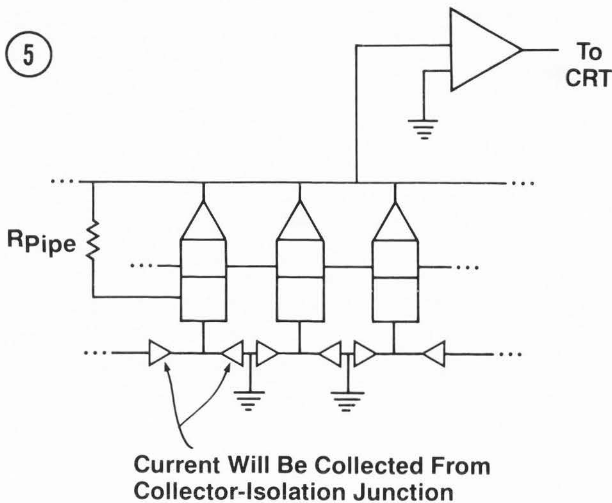


Figure 5. Electrical configuration of the 320-transistor array connected for EBIC location of piped transistor. (Ref. 4.)

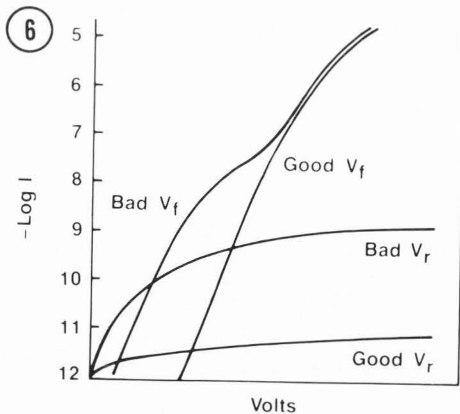
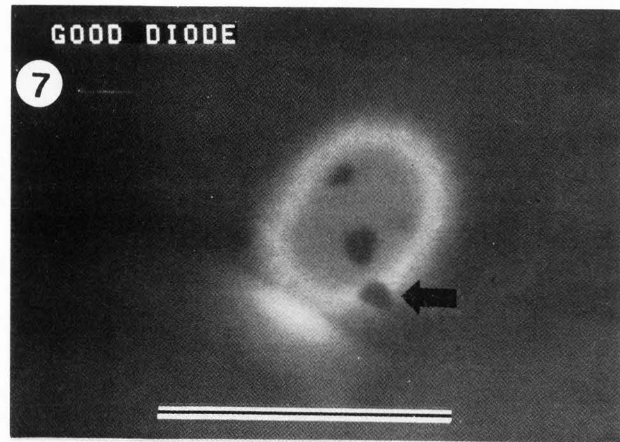
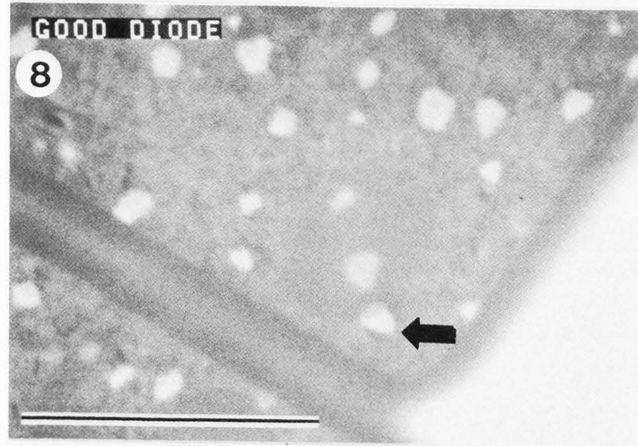


Figure 6. Electrical characteristics of a good and of a bad Schottky barrier diode.





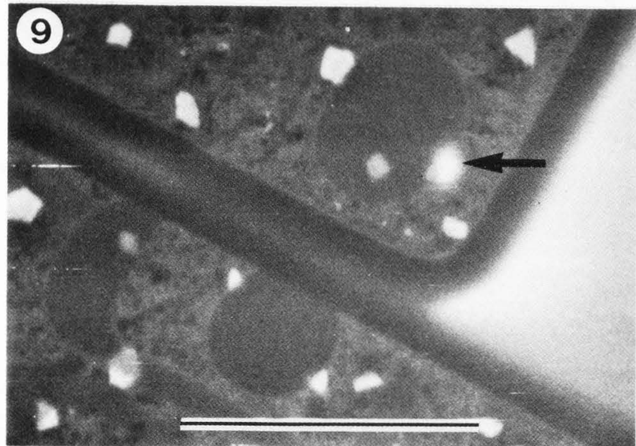


Figure 7. EBIC micrograph of a good SBD. Dark spots indicate copper-rich grains in the metallurgy. Beam voltage = 10 keV. Bar = 10 μm.

Figure 8. Emission-mode micrograph of a good diode. Bright spots are copper-rich grains in the metallurgy. Beam voltage = 10 keV. Bar = 10 μm.

Figure 9. EBIC signal from a defective SBD superimposed on the emission-mode micrograph. Bright spot (arrow) is electrical defect. Beam voltage = 10 keV. Bar = 10 μm.

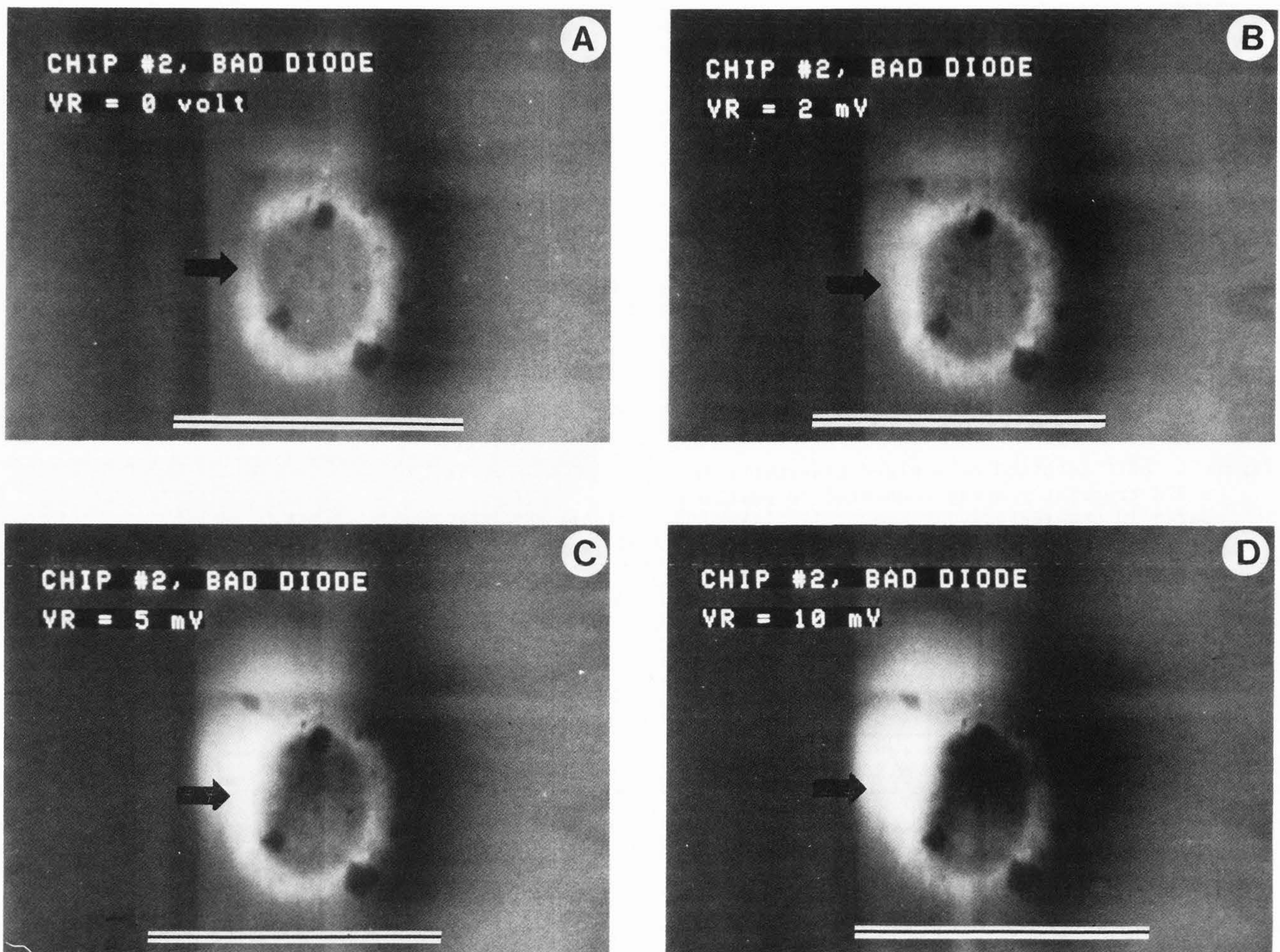


Figure 10. EBIC micrographs of a defective SBD at various reverse-bias voltages. Bar = 10 μm.

These examples of EBIC measurements have shown the importance of being able to find a particular transistor or region of a transistor that is causing an electrical failure. The explanation of the EBIC result is necessary in order to determine that the defect so detected is the cause of the device parameter observed.

Depletion Region Characterization By EBIC

The behavior of the carriers generated by the electron beam depends on the properties of the material in the immediate environment of the carriers generated. Thus, EBIC can be used to characterize these properties. Ion implantation of dopant into silicon is being used more and more for processing integrated circuits, and information règarding the resulting depletion regions associated with these implanted junctions is less easily derived apart from EBIC than for diffused junctions using diffusion theory. The ion implantion process utilizes a beam of high energy ions striking the silicon surface to penetrate the crystal and dope the silicon to the desired type and concentration. The resulting doping concentration profile may be determined for large areas using Secondary Ion Mass Spectroscopy (SIMS), but for small devices these profiles may be determined using EBIC. Figure 11 shows a sketch of the structure of some diodes that were examined using the EBIC technique. These devices were made by depositing polycrystalline silicon (N-type) on boron-doped silicon (P-type) with a boron doping of four different concentrations. The interest was to determine the junction depths for the different doses of BF_2 used to implant the boron.

The devices were each sectioned at 90° through the center of the diode contact. The diodes were 2 μm in diameter. The sectioned device was then mounted on a TO-5 integrated circuit header and wire bonded. Next, this header was placed inside a SEM equipped with an appropriate socket, aligned so that the beam was normal to the sectioned face, and turned so that a line scan could be made from the top of the diode to the bottom through the center of the sectioned diode. The EBIC current amplifier output was connected to a Tracor Northern NS-570 Digital Signal Averager. The beam voltage was 5.0 keV. The resulting EBIC line scans are shown in Fig. 12. The vertical scale is in relative units of current, and the vertical position (grey level) of each curve is adjustable. The horizontal position of each curve is non-critical, but the horizontal gain (magnification) is critical and calibrated with a standard known dimension in the SEM using the line scan mode of the same rate used for making the EBIC traces. These data were then stored in the NS-750 and transferred serially to an IBM 5110 computer. The computer allows data analysis, curve smoothing, diskette storage, and digital plotting. The curves in Fig. 12 were not smoothed, but are the accumulated data of eight line scans across each diode at precisely the same operating conditions.

The junction depth measurement requires the location of the polysilicon/silicon interface, or some other reference point from which to measure the junction depth. In this work, since no repeatable EBIC signal could be correlated to the interface, measurements were made from the leading edge of the EBIC peak exactly at one-half maximum height. This junction should have a non-symmetric depletion region, extending further into the lightly doped P-side than into the higher doped N-side (polysilicon side). The EBIC trace might have a nearly vertical initial rise, and the departure from this would be due to the spatial resolution of the excitation volume within the semiconductor bulk (see Fig. 13). Table 1 shows the results for the EBIC measurements on the four devices.

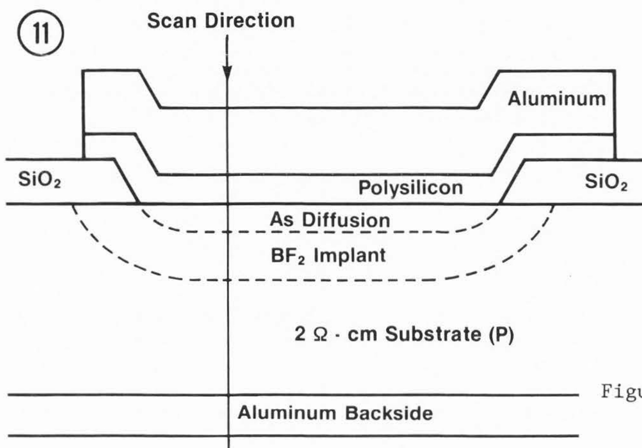


Figure 11. Schematic of an ion-implanted diode structure. Boron implant doses (BF_2) were varied for this experiment.

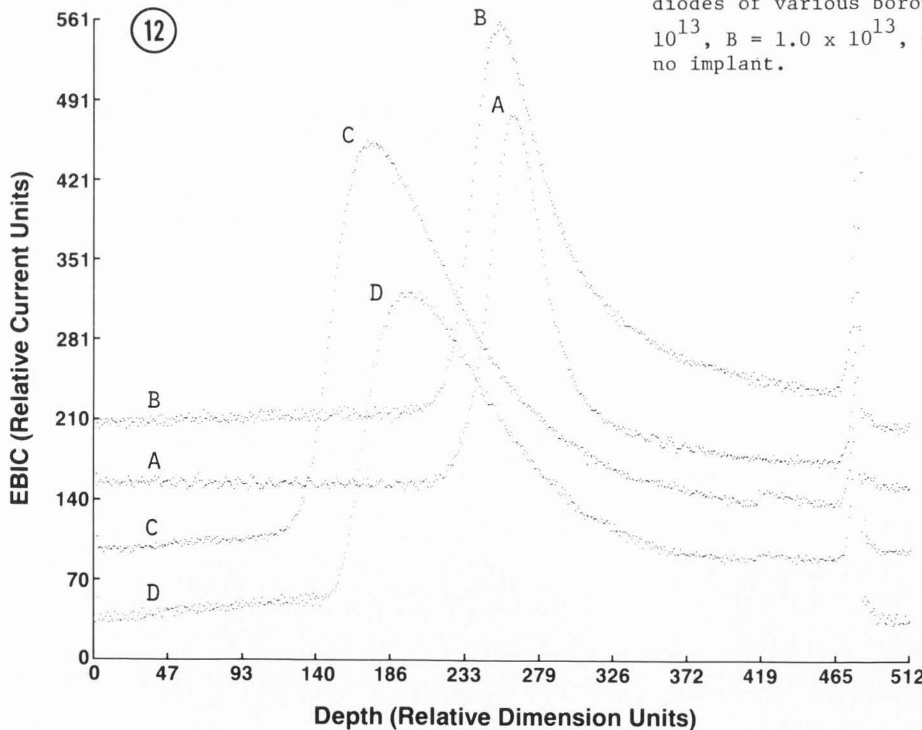


Figure 12. EBIC line scans across ion-implanted diodes of various boron doses. A = 1.5 x 10^{13}, B = 1.0 x 10^{13}, C = 5 x 10^{12}, and D = no implant.

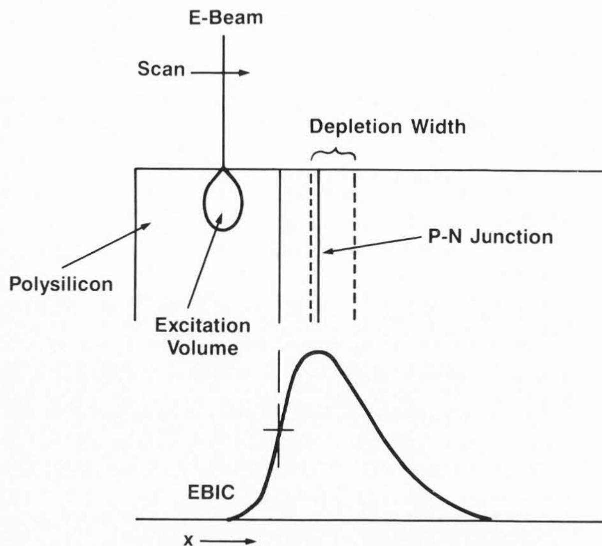


Figure 13. Relationship between electron beam, excitation volume, depletion region of a P-N junction, and resulting EBIC signal.

Table 1. Implant doses, reverse breakdown voltages, and junction depths for four ion-implanted diodes.

BF_2	Vb (100 nA) (Volts)	EBIC Junction Depth (Angstroms)
1.5×10^{13}	0.35	1940 (scan A)
1×10^{13}	0.6	2640 (scan B)
5×10^{12}	3.2	3370 (scan C)
0	5.5	3930 (scan D)

Zook [17] calculates the EBIC curve as a function of distance from the P-N junction for various shapes and sizes of excitation volume and concludes little dependence on the shape. Marten and Hildebrand [13] calculated the location of maximum EBIC signal for III-V compound P-N junctions and found the maximum to be determined mainly by minority carrier lifetime differences. The depletion regions associated with the samples they studied were typically 20 to 30 microns wide.

The measurements in the present work were made from the leading edge to the maximum of the EBIC peak. The beam voltage was 5.0 keV and the beam penetration depth was determined to be approximately 3000 Å. The initial rise slope was calculated for each curve normalized to maximum EBIC current and the slopes were the same. This supports the choice of the leading edge as the reference point for the junction depth measurements. The resulting four junction depths allow doping profiles similar to those sketched in Fig. 14. Further analysis will involve a structure large enough to perform SIMS measurements for correlation to the EBIC results.

FET Channel Length By EBIC

Attempts to measure the channel length of a field effect transistor (FET) usually involve a delineation of the junctions of the source and drain diffusions by some metallurgical means, such as bevel and stain or junction etch. These methods are inadequate for short channel devices on the order of one micron channel length. Some workers have attempted to delineate the junctions by EBIC measurements from the top surface of the FET, but these have led to ambiguity due to the topological irregularities affecting the EBIC signal very near the edge of the diffusion, as in a self-aligned gate. The solution to the difficulties is to section the device and measure the separation of the junctions on the device. The channel length of a FET determines the threshold voltage, i.e., the gate voltage that will turn on (or off) the device. This dimension is necessary for correlation of processing parameters to determine the ΔL, the relation between the final electrical channel length and the original mask dimension.

In order to make this EBIC measurement, the FET must be laid out such that all contacts are preserved when the transistor is sectioned through the center. This can be accomplished if all the contacts come into the device from one side of the device.

When the transistor is sectioned 90° or at a 19° bevel, the contacts can be wire bonded. Figure 15 shows the transistor characteristics of one such device that is sectioned at 90° in this way and still operating as a good FET. This device was placed in the SEM for EBIC measurements, and a line scan was made along the oxide/silicon interface between the source and drain just below the gate oxide. The gate was tied to ground in this measurement. For this device, and others whose channel lengths are in the 1 micron range, it is necessary to make two line scans and superimpose the two EBIC traces for measurements. Each scan is made on one junction while the other junction is shorted. This allows each individual P-N junction to be represented by the EBIC signal without interference from currents generated in the other junction. One set of EBIC scans is shown in Fig. 16. The electrical channel length for this device is the distance between the depletion regions for each junction.

Since the EBIC line scans showed the depletion regions to be symmetric in this section, the peak was taken to be the true P-N junction. The EBIC line scan was calibrated with a depletion width measurement by the capacitance technique outlined earlier for a large area diffusion in the same product. The value for W was found to be equal to the width of the EBIC peak at 0.85 of its maximum value. Thus, the electrical channel length for this device is the peak-to-peak distance minus one half of each depletion width, or

1.49 - (0.32 + 0.37) = 0.80 microns. This value gave good agreement with the ΔL measurements. The difference in the two depletion widths was not explained although three other identical devices and one similar device sectioned in the opposite direction gave the same results.

Summary

Electron beam induced current measurements can be used for failure analysis and device characterization. TREBIC offers a narrower signal in the line scan mode, but often this is not necessary to obtain good results. Computerization, probing in the SEM chamber, and digitizing of the data all offer advantages to the device analyst: however, we have found that one scanning electron microscope devoted to these electrical measurements on integrated circuits is necessary for timely results. Obtaining an EBIC micrograph or line scan may be easily demonstrated in most electron microscopes, but the refinement of techniques, data interpretation, and sample preparation are all necessary to make this powerful technique a reliable and routine failure analysis technique.

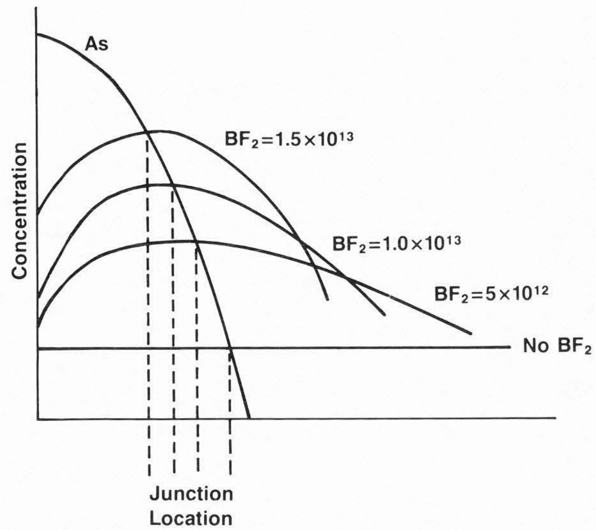


Figure 14. Approximate concentration profiles suggested from EBIC results on ion-implanted diodes.

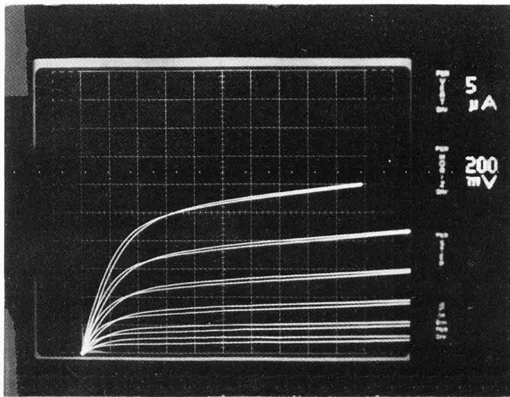


Figure 15. Curve-tracer electrical characteristics of FET sample inside SEM and sectioned with all elements operational. Gate voltages, from top to bottom, respectively, are -0.4, -0.5, -0.6, -0.7, -0.8, and -0.9 volts.

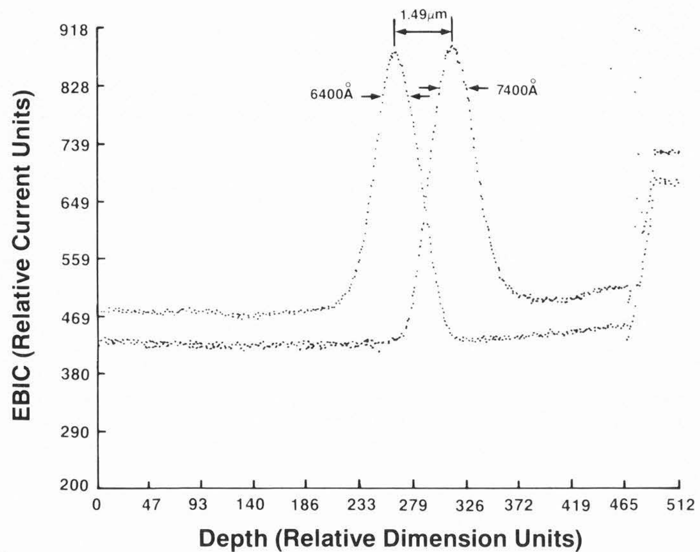


Figure 16. EBIC line scans from FET for making electrical channel length measurements. Channel length = 0.80 μm.

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Discussion with Reviewers

J.R. Beall: For equation (4), would you further describe what is meant by depletion region "tail"?

Author: Sze (ref 16, page 77) discusses obtaining a more accurate depletion layer width by considering the majority carrier contribution in addition to the impurity concentration. The depletion width, W, is essentially the same as for a two-sided abrupt junction, except that the built-in voltage or junction potential, ϕ, is replaced by ϕ - 2kT/q. This correction factor comes from what Sze calls the "majority carrier distribution tails," that is, electrons in the n side and holes in the p side. Each contributes a correction factor, kT/q, arising from the dipole moment of the "error" distribution, that is, the true carrier distribution minus the abrupt distribution.

J.R. Beall: What method was used to avoid coupling capacitor differentiation in Fig. 10?

Author: The input capacitance was 0.1 microfarads, and the line scan rate was 16.8 msec/line (horizontal) for recording the micrographs. Alteration of the EBIC signal trace was not observed until scan rates faster than 2.08 msec/line were used. The 16.8 msec/line would correspond to an electron beam scan rate of 1 mm/sec on the specimen at 5000 X. The input resistance remained very low during AC measurements, maintaining a time constant too fast for visible differentiation. The input resistance of the amplifier was 0.53 ohms.

J.R. Beall: In Fig. 12, how is the leading edge of the EBIC line scan related to the polysilicon/silicon interface?

Author: The leading edge of the EBIC signal, that is, the location where the signal just begins to be detected at the gain setting used for the entire scan, occurred in the polysilicon layer very near the interface. The aluminum/polysilicon interface, as observed in the emission mode, was very irregular. This is due to the rough surface of the polysilicon and possibly smearing of metal during sectioning. The polysilicon/silicon interface was not visible in the emission mode. We measured the thickness of the polysilicon over the oxide and projected a polysilicon/silicon interface by adding this thickness to the thickness of the metal. This produced only an approximate location of the interface higher up the leading edge at one-half maximum of the EBIC signal.

C. Donolato: Why did you plot the depths in Figs. 12 and 16 in relative dimensions rather than in microns?

Author: Relative units are used in these plots because the location of the peaks with respect to zero on the abscissa and with respect to zero on the ordinate are unimportant. Only the shapes of the curves and the dimensions of each individual curve are significant. Of course, in Fig. 16, the distance in the horizontal direction between the two curves is of significance.

C. Donolato: You state that the EBIC scans of Fig. 16 show the depletion regions to be symmetric, a rather uncommon feature. How is this property deduced from the scans of Fig. 16?

Author: The true depletion region of the junction is associated with the width of the EBIC peak near its maximum. When the shapes of

the EBIC curves of Fig. 13 were determined in this region, they were symmetric. This comparison is very easily done arithmetically in a computer. This is not to say that the depletion regions themselves are symmetric. A completely symmetric depletion region is unlikely, especially in these devices. The shapes of the EBIC curves in Fig. 12 are unsymmetric.

H.W. Marten: Please explain the dependence of TREBIC on reverse bias.
Author: Since TREBIC involves the measurement of the fast component of the EBIC signal in a very short time segment, the measured signal is very low, typically less than two orders of magnitude lower than the real-time EBIC current. Therefore, the junction being studied is usually reverse biased in order to increase the signal by increasing the electric field. Often this reverse bias, on the order of a few volts, may not be applied to a device without altering it or even, in the case of a sectioned device, destroying it. In other cases, where the device is an element of a circuit, the other elements of the circuit may prevent or affect the reverse bias being applied. We have found these requirements to be more difficult to overcome than the timing requirements in the measurement.
H.W. Marten: Are not the low beam voltages generally unsuitable for EBIC studies since complex modifications occur due to the small penetration depth, i.e., due to the close vicinity of the incident surface?
Author: Since much of our work has to do with sectioned devices, necessarily, in order to investigate vertical and horizontal parameters, the smallest diameter excitation volume is desirable. This can be achieved with low beam voltages in the 1 to 5 kV range. The penetration of the beam is still enough to produce a bulk effect rather than a strictly surface effect. In cases where penetration of passivation layers is of interest, higher beam voltages, with the accompanying larger excitation volume diameter, may be necessary. This sometimes causes complexity due to horizontal interactions among devices.
H.W. Marten: Since the EBIC traces were recorded close to the silicon-oxide interface, how could you calibrate them using the "bulk" space charge layer width obtained from C-V measurements?
Author: Certainly the (C-V)-determined width of the large horizontal junction will be different from the depletion width of the vertical junction near the silicon-oxide interface, but we are working on this. The approximation obtained in this way is the closest one we can get at the present time.
H.W. Marten: Please explain the offset of the EBIC traces (Fig. 16) within the n layer, which is not grounded.
Author: As the electron beam passes across this n region very near the silicon/oxide interface, it excites a small signal within the region from above the junction. This can be eliminated as the line of the scan is moved upward. We found that the signal from this region of the device, when it was on the order of 10% of the peak height, did not affect the channel length measurement. This is probably due to the relatively deep (3000Å) junctions. If the "bulk" region of the EBIC trace is much greater than 10%, a shift to longer channel lengths could result.
H.W. Marten: Which current amplifier was used, and what were the input resistance and capacitance?
Author: Several current amplifiers are used for different applications, but the one most often and most generally used is the Princeton Applied Research Model 114 with the Model 184 preamplifier. The input resistance of this amplifier is 0.53 ohms ("virtual ground"), and AC coupling is accomplished with 0.1 microfarads capacitance.
H.W. Marten: What beam currents did you use? Did you observe any dependence on EBIC on decreasing the beam current? Using low beam currents, did you try to locate electrical defects such as pipes?
Author: The typical beam currents used were $4.9E^{-}10$ A (5 kV). In general , the effect seen on the EBIC signal for slightly higher or lower currents was to increase or decrease the signal. Locating defects at very high currents was difficult, since the signal was altered and localized differences were smeared in the micrograph. We did not use beam currents lower than $3.53E^{-}11$ A. We located pipes whose EBIC image was on the order of 3000Å using beam currents on the order of 4.9×10^{-10} A.
H.W. Marten: Did you observe any dependence of the mesured FET channel length on the beam voltage? Did you estimate or eliminate possible displacements of the EBIC maxima from the respective pn-junctions? What are the quantitative error limits for the measured channel lenghth?
Author: Channel length measurements on 90-degree sections have been made using beam voltages from 3 to 10 kV. The higher voltages result in shorter channel lengths. This could be due to the effect of the large excitation volume affecting areas of the junction other than the vertical portion that intersects the surface. We found the channel lengths measured using 5 kV to be in agreement with the electrical threshold voltage techniques, and we estimate the accuracy of this technique to be within 300Å.

A. Bernds & S. Gorlich: Do you have any suggestions about the kind of defect in Fig. 10?
Author: Associated with the defect in Fig. 9, subsequent SEM analysis of the anode area after partial etching of the metallurgy revealed a copper-rich grain possibly penetrating the platinum silicide and perhaps making contact with the silicon. The defect in Fig. 10 was some sort of edge effect, less localized, and less clearly defined, but there was an irregularity at the nitride-defined edge at the defect location. We did not conclude what this particular defect was, other than that it was related to the contact edge.

A. Bernds & S. Gorlich: How did you calculate the rise slopes of the EBIC curves in Fig. 12?
Author: Since the point-by-point data is stored in the computer, a slope was calculated from five adjacent data points at three different locations on the curve. Although we have curve-smoothing functions and straight-line-fitting functions in our computer capabilities, we did not use them in this calculation. Since the structures of the devices were the same above the ion implant region, we concluded that identical slopes indicated the same location beneath the polysilicon. This is an approximation since the polysilicon/silicon interface was not visible after sectioning nor delineated by etching.

J.R. Beall: In "Applications of EBIC" you say, "very often no sophisticated interpretation... to find a defect or irregularity." Two factors that are very important in interpreting EBIC data are a good understanding of the EBIC generation and collection process and familiarity with the device construction. I agree finding an anomaly may be easy but understanding it's significance requires greater knowledge of the EBIC process and device construction.
Author: Thank you for your comment.