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CROSS-SECTIONAL ANALYSIS OF SILICON METAL OXIDE SEMICONDUCTOR DEVICES USING THE SCANNING ELECTRON MICROSCOPE

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Abstract

A technique has been developed which enables one to cross-section specific devices or features for examination with the scanning electron microscope (SEM). This method is used for investigation of all facets of microelectronic circuit manufacture from research and development to failure analysis of the finished product.

Selective etching is used to provide contrast to each processed layer. Etch type and sequence, used for delineation, are important to understand since they may add artifacts to the cross-section, leading to erroneous analysis conclusions. The etchant and etch conditions used will be dictated by the information needed from a particular sample.

Etching systems based on $HF-HNO_3-H_2O$ are used with metal oxide semiconductor (MOS) technologies. In addition, buffered silicon dioxide etches are also used especially to delineate silicon dioxide layers.

Cross-sectional analysis enables measurement of processing parameters such as junction depth, channel length, layer thickness and length, layer composition and step coverage.

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Introduction

Device and processing technologies are continuously shrinking in the microelectronics industry. Modern devices use processing parameters of less than $3\mu m$ routinely while future devices will use processes designed for 1 to $2\mu m$ technologies. Cross-sectional analysis of such devices using the scanning electron microscope (SEM) is useful in product development and failure analysis. Considering this, a micropolishing technique was developed which will enable one to cross-section a specific area or device without encapsulation or an apparatus specially built for cross-sectioning or cleaving. This technique will be discussed in this paper.

In addition, the effect of selective etches, which are used to enhance the contrast of the layers of the sample, needs to be understood. Different etch types will be discussed as well as the effect of varying the sequence of etching and lighting conditions during etching. Comparisons of different etches are presented with considerations for interpreting the cross-section after preparation.

Technique

The micropolishing technique developed consists of two stages of polishing, using common laboratory materials without encapsulation. Earlier methods have relied on encapsulation[1,7,8] of the sample or special apparatus[3,4,5,7,8], to polish or cleave the sample.

Encapsulating the sample to be polished obscures the view of the sample making specific area or device analysis difficult. Any surface analysis after encapsulation is nearly impossible; increased specimen charging and long preparation time are two additional disadvantages of encapsulation.

This technique uses an X-ACTO (X-ACTO, Long Island, N.Y.) knife to hold the sample. The sample, which may be an individual die or a small piece of wafer, is placed in the position where the knife blade is normally held, as shown in Figure 1. This holds the sample well and does little damage to the portion the chuck is gripping.

The sample itself should be no larger than

1.3 cm on a side with the side to be polished opposite the holder (the bottom edge in Figure 1). If a specific area or device is to be cross-sectioned it should be photographically documented with an optical microscope for easy location during polishing and to insure that the holder is not covering the area of interest.

After documentation the first stage of polishing is started. The sample is placed on a polishing wheel with 600 grit sandpaper. The sample is oriented as shown in Figure 2 with the angle between the sample back and the grinding wheel, θ, being about 45°. The circuit side of the sample is facing up in Figure 2 with the direction of wheel spin being right to left. The sample is polished in this manner until the polished edge is within 50μm of the desired area of interest. Periodically, observation of the sample using the optical microscope should be done so that one does not rough polish through the area of interest. Figure 3 shows the polished edge after rough polishing -- note the beveled edge.

The second step is the final polish where the section is brought to the area of interest. The sample is held again at an angle, θ, of 45° between the back of the sample and the polishing wheel as shown in Figure 4. In this step the direction of the polishing wheel spin is away from the circuit face (i.e., right to left in Figure 4). The sample is held such that the direction of spin is into the back of the sample. The fine polish uses a felt cloth on the polishing wheel and a slurry of 0.05μm alumina in deionized (DI) water. The final polish, which polishes from the back of the sample toward the circuit face, utilizes the nap of the felt cloth to cause a desired rounding effect at the polished edge. As the nap contacts the back of the sample, it is compressed to the wheel. Then, as the nap passes under the polished edge of the sample, the nap relaxes to its original position. This gives the polished edge a surface normal to the circuit surface as denoted by the arrow in Figure 5. This is the step at which the specific area of interest is sectioned. Periodic examination under the optical microscope is needed so that one does not polish completely through this area. For very small areas of interest examination in the SEM is often needed during the polishing process.

When the section has reached the area of interest, the polished edge is rinsed with DI water and with methanol, then is blown dry with dry nitrogen to await further processing for SEM observation.

Technique Considerations

The angle of tilt, θ, during polishing determines the bevel angle and to an extent the polished rate and smoothness of the polished edge. An angle of about 45° has been found by experience to be optimal. At this angle the polished edge is normal to the circuit surface as was seen in Figure 3. If the tilt angle, θ, becomes too small (<30°) various layers on the processed sample will be damaged. Artifacts such as cracks in oxide layers and the substrate material are often observed when the tilt angle becomes too

Table 1: Measured Lengths for Various Angles in Figures 6 and 8 ($\ell' = \ell/\cos\alpha$).

$\alpha = 0°$	$\ell' = \ell$
$\alpha = 5°$	$\ell' = 1.004\ell$
$\alpha = 10°$	$\ell' = 1.015\ell$
$\alpha = 15°$	$\ell' = 1.035\ell$
$\alpha = 18°$	$\ell' = 1.051\ell$
$\alpha = 20°$	$\ell' = 1.064\ell$
$\alpha = 25°$	$\ell' = 1.103\ell$

small. Conversely, if the tilt angle, θ, exceeds 60° the top passivation and metal layers become rounded by the nap of the polishing cloth.

If the polished edge is not normal to the circuit surface there will be an error in measurement of vertical parameters as shown in Figure 6. In this figure the electron beam direction is from the right, perpendicular to the circuit surface normal. If ℓ is the desired measurement and the angle γ is the angle of the polished surface to the normal then the measured value will be:

$$\ell' = \ell/\cos\gamma \qquad (1)$$

Table 1 shows the value of ℓ' in ℓ for different angles. Notice that for an error of 5% an angle of 18° can be tolerated. For an error of 10% an angle of 25° can be tolerated.

Horizontal measurements will also suffer an error if the attitude angle, ϕ, is not 0°. The attitude angle is the angle between the polished edge and a line parallel with the edge of the structure upon which a horizontal measurement is to be made. For instance, if the channel length of a metal oxide semiconductor (MOS) transistor was to be measured, the attitude would be the angle between the polished edge and the edge of the gate region. This angle is controlled by the placement of the die on the polishing wheel as shown in Figure 7. Figure 8 shows this in schematic form where ℓ is the desired measurement and ϕ is the attitude angle. This view is from the surface of the circuit; the electron beam, during observation in the SEM, would be directed from the bottom of the figure. The measured value, ℓ', is $\ell/\cos\phi$, as in the earlier example. Table 1 corresponds to this example. This angle is usually small, especially in <100> material since the lattice planes of the silicon substrate are usually aligned parallel to device features.

If a specific area is to be cross-sectioned it is helpful if the area is marked in order to facilitate optical observation during polishing. Among methods used to mark an area are small laser blasts or scratches produced by tungsten probe tips used for microprobing of circuits.

The cleanliness of the felt cloth used for the final polish is also important. The surface of the felt cloth should be cleaned with DI water before polishing; a build up of polishing slurry should be avoided during polishing. If the felt cloth is not clean, residue from prior polishes will accumulate onto the sample, obscuring features.
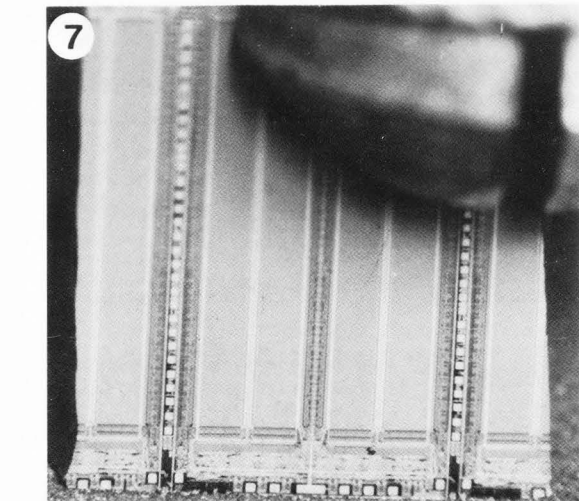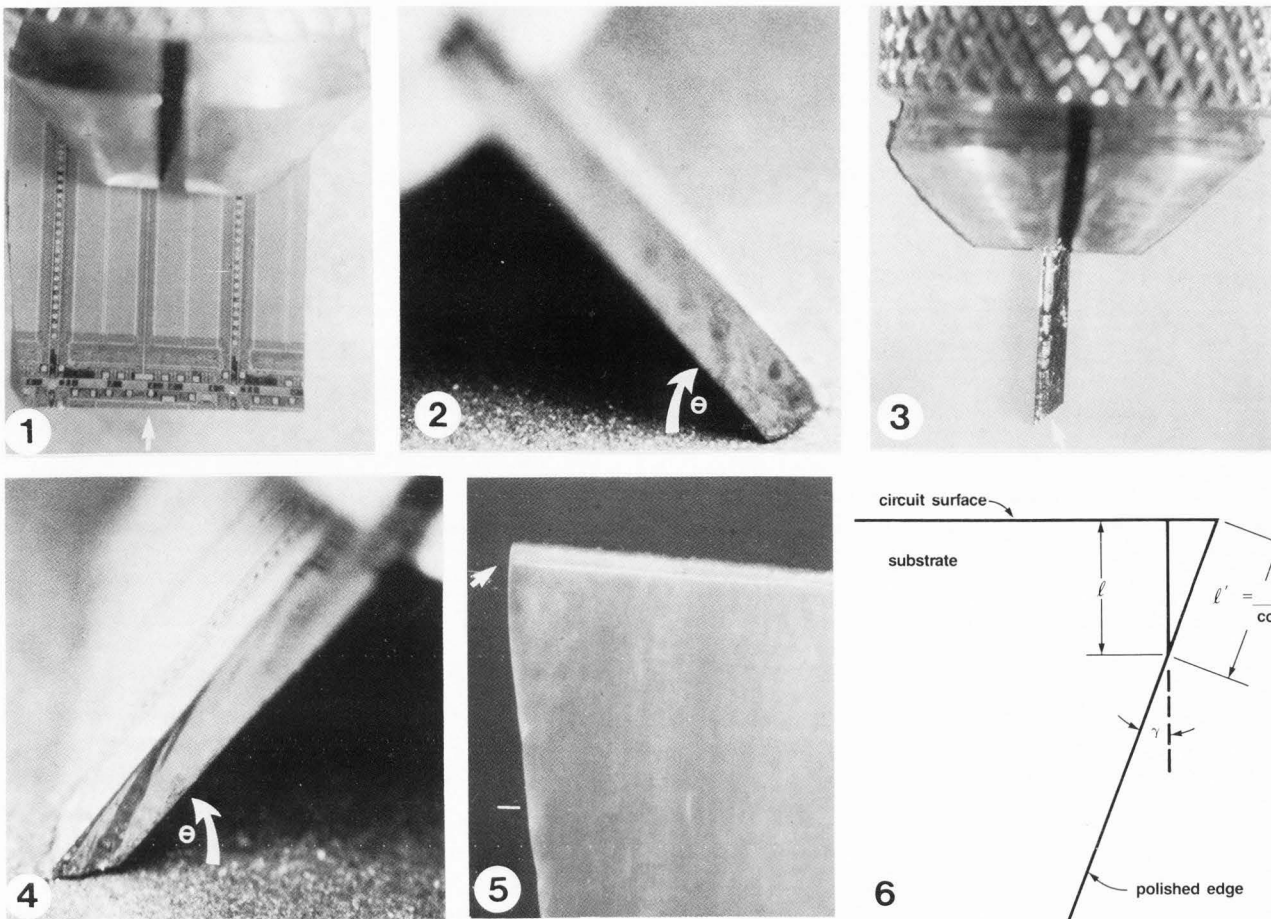
circuit surface

substrate

$$\ell' = \frac{\ell}{\cos\gamma}$$

γ

polished edge

Figure 1: Sample position in holder, arrow indicates edge to be polished.

Figure 2: Orientation of sample during the first stage of polish. The angle of tilt, θ, is denoted. The direction of spin of the polishing wheel is right to left.

Figure 3: Polished edge after the first stage of polish. Arrow indicates the beveled edge after the first stage of polish.

Figure 4: Orientation of the sample during the fine polish. The angle of tilt, θ, is denoted. The direction of spin of the polishing wheel is right to left.

Figure 5: Normal polish face at the circuit surface (arrow). The line marker is 10.0μm.

Figure 6: Error in vertical measurement due to non-normal face. The measured value is ℓ', the desired measurement is ℓ and γ is the angle from the normal.
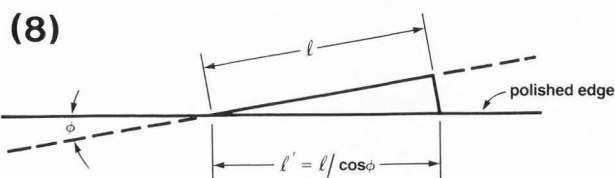
Figure 7: Front view of sample during polish. The attitude, φ, is controlled at this step.

(8)

ℓ

polished edge

ϕ

$\ell' = \ell / \cos\phi$

Figure 8: Error in horizontal measurements due to non-zero attitude angle. The measured value is ℓ', the desired measurement is ℓ and φ is the attitude angle.

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Structure Delineation

In order to study the various structures of the polished sample, chemical etching must be utilized in order to delineate the structures. Various etches have been discussed in the literature[2,5,9,10] many using an HF-HNO3-H2O based system. We have found that three etches will provide data in the majority of our studies. The etches are: 20/1 (20 parts HNO3 and 1 part HF by volume), KOH (saturated solution of KOH pellets (85% KOH) in DI water) and common oxide (CO) (7 parts HF and 1 part NH4F by volume).

The 20/1 etch is used to delineate junctions and doped polysilicon traces. Twenty to one (20/1) will also slowly etch silicon dioxide, especially when the oxide is doped with phosphorus. KOH etches aluminum alloy metal systems, delineating aluminum layers but not significantly etching silicon dioxide, polysilicon or delineating junctions. Common oxide etches at a controlled rate of about 3000Å per minute at room temperature (25°C) when the oxide is doped with 4% (wt.) phosphorus. Common oxide etch is used when oxide layers need to be delineated without etching polysilicon or delineating junctions.

An etch commonly used is two seconds 20/1, followed by six seconds KOH at room temperature in room light. After application, the sample is rinsed in DI water, followed by methanol and dried with dry nitrogen. The sample should be rinsed well after etching; any etchant left on the sample face will continue to etch, in time destroying the sample. In order to avoid this type of degradation the sample should be etched just prior to insertion in the SEM.

The etch sequence described above delineates junctions, oxide, polysilicon and aluminum layers as shown in Figure 9. The aluminum layer is still visible with this technique enabling one to study this layer. This is an advantage over methods[4] which completely etch back the aluminum leaving a void at that location.

Since etch rates for silicon oxides are dependent on chemical composition (e.g. phosphorous concentration) and to a lesser extent, density and stress[6], different types of oxide may be differentiated with this etch sequence. This is shown by the microsection in Figure 9. In general, thermally grown oxides will be brighter than deposited oxides; oxides with a greater phosphorous concentration will appear darker since they have a higher etch rate and are recessed from the polished surface.

Common oxide etch is used instead of 20/1 etch when an oxide thickness must be measured, especially that of a gate oxide. In Figure 9 the gate oxide is bright and appears to be thicker than its actual thickness. Since the polysilicon gate and the substrate under the gate have been etched back at a greater rate than the gate oxide, the gate oxide is protruding from the surface, forming a ledge. This will create two effects: 1) the gate oxide will be bright, appearing thicker than it is, due to secondary electron emission from the top and bottom as well as the side of the oxide; 2) in extreme cases, the gate oxide will appear rippled or curved due to inadequate support since the surrounding polysilicon gate and substrate have been recessed.
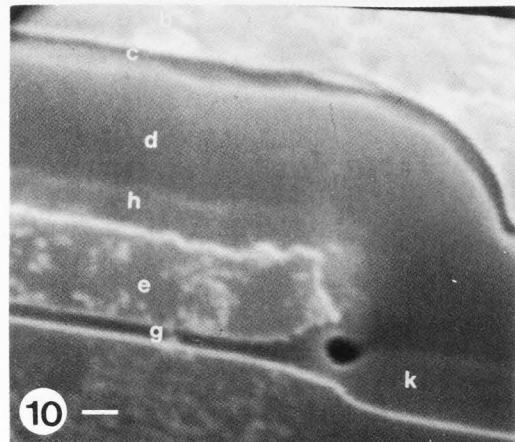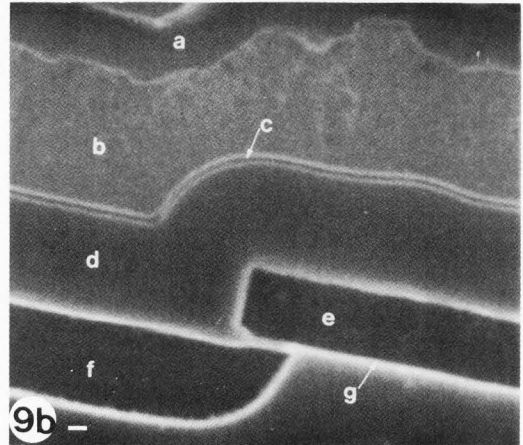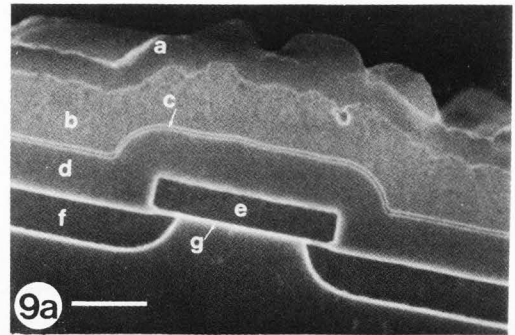
Figure 9: (a) View of an MOS transitor in cross-section. (b) Higher view. Layers are denoted as listed in Table 2. Bar = (a) 1.0μm, (b) 0.1μm.
Figure 10: View of an MOS transistor in a cross-section using fifteen seconds common oxide etch. Layers are denoted as listed in Table 2. Bar = 0.1μm.

Table 2: Layer Designations for Micrographs

a. top passivation
b. aluminum layer
c. phosphorous stabilization layer (PSG)
d. hotwall SiO_2
e. polysilicon
f. n^+ regions
g. gate oxide
h. thermal oxide (polysilicon)
k. thermal oxide (substrate)

These effects are enhanced if the sample is over-etched with 20/1 etch.

For more accurate gate oxide measurements fifteen seconds of common oxide etch instead of 20/1 etch should be used. This will etch the oxide layers without etching the polysilicon or the substrate. In this case the gate oxide is recessed, completely supported by surrounding layers. An example is shown in Figure 10.

Common oxide etch is also useful to distinguish individual oxide layers and to differentiate between oxide and non-oxide dielectric and passivation layers.

Etch Considerations

Sequence of etches performed, length of time etched and lighting conditions will influence the final product.

To understand the influence of an etch sequence one must look at the effect of each individual etch. In Figure 11 a simple structure has been drawn schematically to investigate etching effects. The figure shows a series of profiles of a cross-section with the polished edge being the right edge of each profile; during SEM observation the electron beam would be entering from the right side. The structure, as shown in view 'a' before any etching, is an aluminum to diffusion contact. The layers involved are a top passivation layer of 4% phosphorous doped silox (SiO_2), a layer of aluminum alloy, an n^+ substrate region and the lightly doped substrate itself. Views 'b', 'c' and 'd' are the structure after KOH only, 20/1 only and common oxide etches, respectively. In view 'b', only the aluminum layer is affected by the etch while in view 'c' the n^+ region and the top passivation are etched with the aluminum layer intact. With 20/1 etch, 4% phosphorous doped oxide will etch very little, not affecting thickness measurements. In the next view ('d'), though, common oxide etch is used which significantly etches this layer of oxide.

View 'f' is the commonly used etch (two seconds 20/1 and six seconds KOH) and view 'e' is that etch sequence reversed. As covered earlier, KOH recesses the metal and 20/1 recesses the n^+ region. In view 'e', if the metal is recessed first, the n^+ area below the aluminum will be recessed greater than where the aluminum is not contacting the substrate. This area is etched faster because the 20/1 etch is acting on the n^+ area not only from the side but also from the top due to the recessed aluminum. The dark area below the contact area may lead to incorrect conclusions during study. The opposite sequence, in view 'f', leads to consistent n^+ delineation. The view does show excessive recessing of the metal at the contact; if aluminum thickness measurements are to be made, the measurement should be made from the top of the metal to the substrate edge. Figures 12 and 13 show the etch sequences for views 'e' and 'f' respectively.

In the next figure, Figure 14, the delineation of an MOS transistor gate structure is shown in profile. The structure is like that in Figures 9 and 10, discussed earlier. In addition to the layers present in Figure 11 we also have a Phosphorous Stabilization Glass (PSG) layer, a thin layer of 10% (wt.) phosphorous doped glass; hotwall SiO_2, a silicon dioxide layer with no phosphorous doping; and a thermal oxide layer grown from the underlying polysilicon layer. The polysilicon layer is doped n^+. Under the polysilicon is the thermally grown gate oxide.

In view 'b' only the aluminum layer is recessed by the KOH etch, no other layer is affected. In view 'c', a two second 20/1 etch slightly etches the top passivation and recesses the doped polysilicon layer. The PSG layer is etched back more than the top passivation layer since it has a higher concentration of phosphorous. Three layers, the hotwall SiO_2, thermal oxide and gate oxide, are not significantly affected by the 20/1 etch since there is no phosphorus in these layers. With a 20/1 etch, as noted earlier, the gate oxide protrudes as a ledge from the sample between the recessed polysilicon and the underlying substrate.

In views 'e' and 'f' the KOH, 20/1 etching sequence is studied. With both sequences the polysilicon layer and the substrate are recessed with the gate oxide protruding. In this example, note the effect of the etch sequence on the aluminum and top passivation. In either case, layer thickness measurements are not affected.

In view 'd' the preferred etch for gate oxide thickness measurements is shown. A fifteen second common oxide etch will recess the gate oxide and the PSG layer. The top passivation oxide layer will be recessed and reduced in thickness by common oxide etch. If top passivation oxide measurements are required for such a section when using common oxide etch, a masking layer of gold should be evaporated onto the circuit surface prior to the etch to protect the top passivation surface.

Verification of the two preceding examples can be done by etching a sample and observing the polished edge at a grazing angle by rotating the sample without changing the tilt angle greatly. Examples of an aluminum to substrate contact and gate structure etched with two seconds 20/1 - six seconds KOH (Figure 15) and fifteen seconds common oxide (Figure 16) are shown. Notice in Figure 15 that the junctions are delineated and the polysilicon and aluminum layers are recessed; the gate oxide is protruded. In Figure 16 the top passivation is recessed and, to a lesser extent, so is the hotwall SiO_2 and the gate oxide layer. There is no junction delineation and no recessing of the polysilicon and aluminum layers. With either etching sequence none of the structure layers is recessed excessively so that surface (i.e., at the cross-section surface) information of each layer is available. Other etch sequences reported in the literature[5],[10] severely recess various layers, reducing available data.

Diffusion or implant regions that are deeply driven or lightly doped will not delineate well with the two second 20/1 etch discussed earlier. In order to delineate such a structure, etching in 20/1 for a longer time will often delineate the lightly doped areas at the expense of over-etching other layers of the sample.
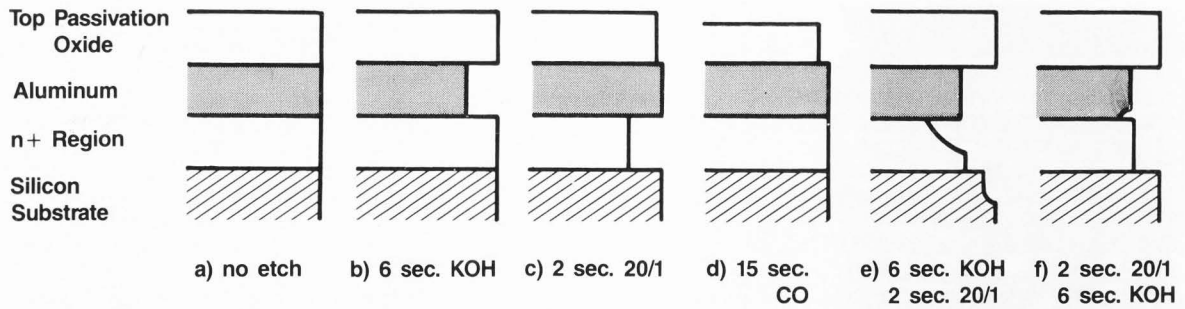
If the lightly doped region is not

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Figure 11: Schematic profile of an aluminum to substrate cross-section exposed to various etches.
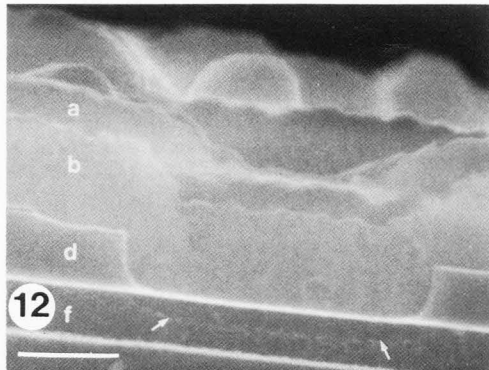

Figure 12: Aluminum to substrate contact cross-section with six seconds KOH and two seconds 20/1 etch. Recessed area in the n^+ region directly below the contact is denoted by the arrows, all other layers are denoted as listed in Table 2. The line marker is 1.0µm.
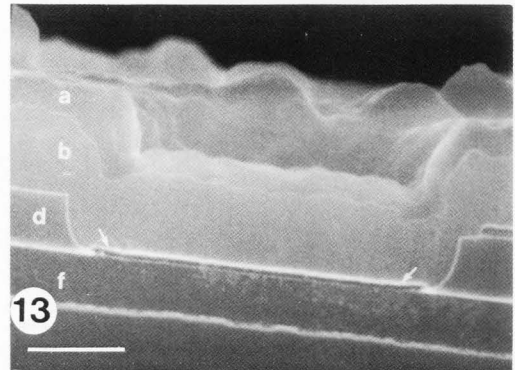
Figure 13: Aluminum to substrate contact cross-section with two seconds 20/1 and six seconds KOH etch. Recessed area in the aluminum layer is denoted by the arrows, all other layers are denoted as listed in Table 2. The line marker is 1.0µm.
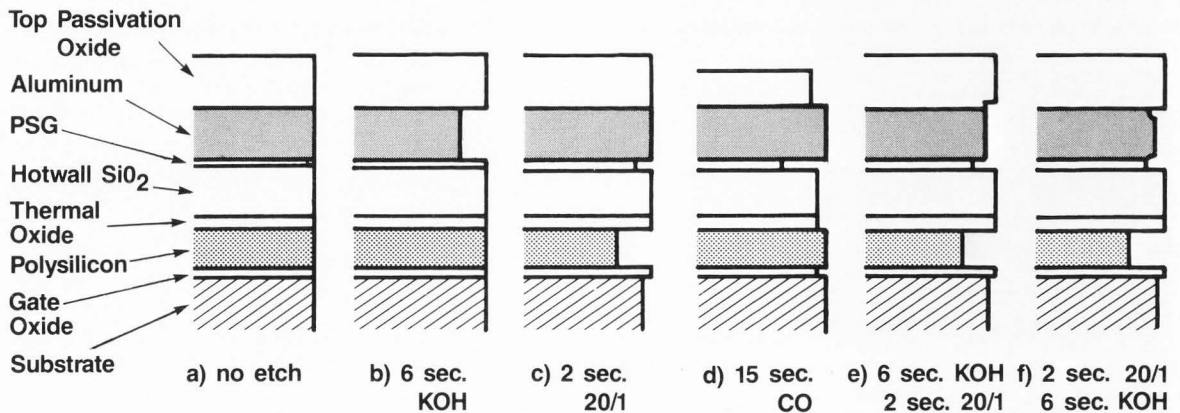

Figure 14: Schematic profile of an MOS transistor gate structure exposed to various etches.

delineated after an extended etch, etching with 20/1 under intense light will delineate the region. Other layers of the structure will be overetched. Frequently the doped region is still difficult to observe; rotating the sample, as in Figures 15 and 16, will permit improved examination of the region.

Examples

Random Single Bit Failures

The microsectioning technique was used to isolate a random single bit failure on the 64K Dynamic Random Access Memory (DRAM). A possible failure mechanism was a random masking error during an early processing step which partially masked an ion implant in the failing memory cell. In order to test the hypothesis, the failing bit, one of 65,536 bits, needed to be cross-sectioned in order to study the ion implant process. A failing die was selected, the failing bit was located and marked by a series of laser blasts that formed a crosshair with the failing cell at the center of the crosshair. With the crosshair, locating the specific cell was easier during the polishing stages.
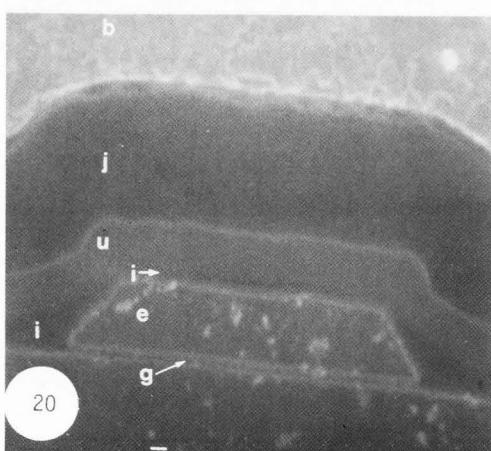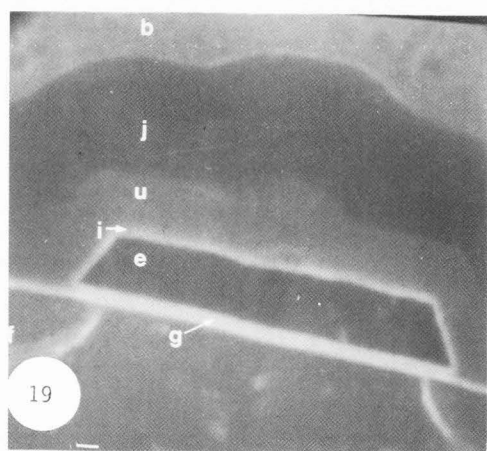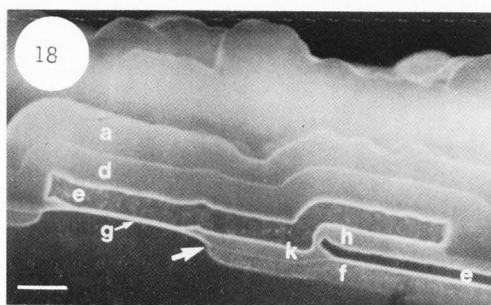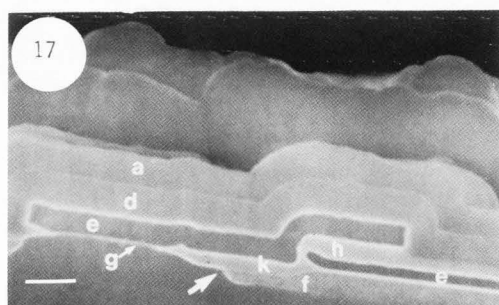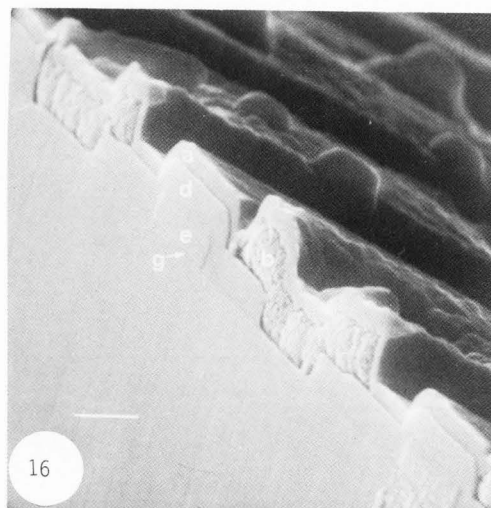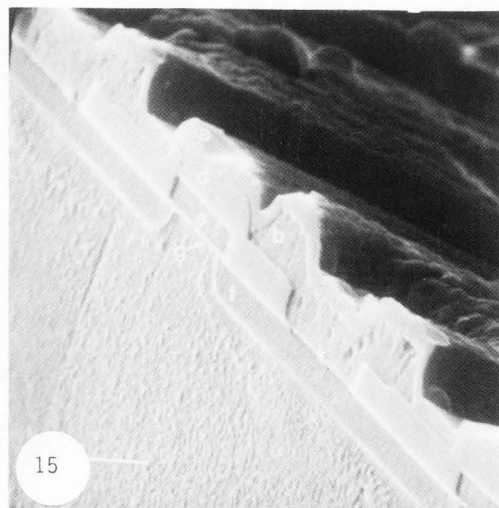
Figure 15: Grazing angle view of an MOS transistor and aluminum to substrate contact cross-section after a two second 20/1 and six second KOH etch. The layers are denoted as listed in Table 2, the bar = 1.0µm. A thin layer of gold has been evaporated onto the polished surface after sample etching.
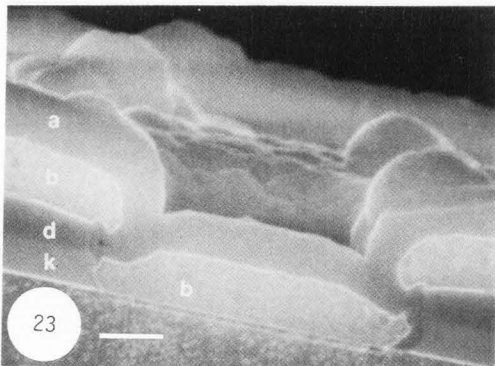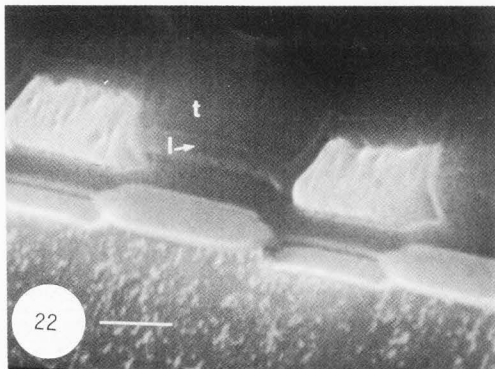
Figure 16: Grazing angle view of an MOS transistor and aluminum to substrate contact cross-section after a fifteen second common oxide etch. The layers are denoted as listed in Table 2, the bar = 1.0µm. A thin layer of gold has been evaporated on the polished surface after sample etching.

Figure 17: Cross-section of the failing bit. The affected implant region is designated with the arrow. The layers are denoted as listed in Table 2, the bar = 1.0µm.

Figure 18: Cross-section of a functional bit. The layers are denoted as listed in Table 2, the bar = 1.0µm. Arrow indicates location of properly located implant.

Figure 19: Cross-section view of multi-oxide layer device etched with two seconds 20/1 and six seconds KOH etches. The layers are denoted as listed in Table 2 except: i) initial 8% P doped oxide; u) undoped deposited oxide; j) 8% P doped oxide. The bar = 0.1µm.

Figure 20: Cross-section view of multi-oxide layer device etched with fifteen seconds common oxide etch. The layers are denoted as listed in Table 2 and Figure 19. The bar = 0.1µm.

Figure 24: Cross-section sequence of aluminum step coverage over a poly II-poly I step. The layers are denoted as listed in Table 2 except p1 is poly I and p2 is poly II. The line marker is 1.0µm in each view.

Figure 21: Cross-section view of two layer top passivation etched with two seconds 20/1 and fifteen seconds common oxide etches. The top layer is designated t and the bottom layer is ℓ, the line marker is 1.0µm.
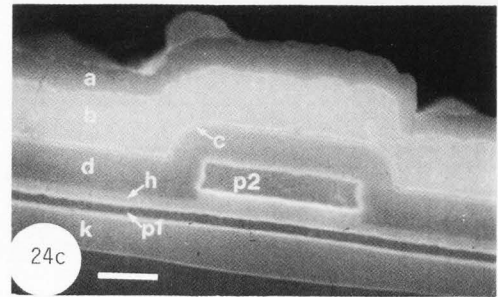
Figure 22: Grazing angle view of two layer top passivation cross-section etched with two seconds 20/1 and fifteen seconds common oxide etches. The layers are denoted as listed in Figure 21, the line marker is 1.0µm.

Figure 23: Cross-section of an open aluminum to substrate contact. The layers are denoted as listed in Table 2. The line marker is 1.0µm.

Figure 17 shows the cross-section obtained from the failing bit and Figure 18 is a control bit which was functional. A comparison of the two bits show that the implant on the right side of the transfer gate (arrow in Figures 17 and 18) is removed from the edge of the gate on the failing bit while the control bit has the implant near the edge of the gate. This was expected if the hypothesis proposed was correct.

Oxide Layer Location

A process was studied where a layer of oxide with 8% (wt.) phosphorous was deposited over the polysilicon layer. An additional layer of undoped oxide was then deposited, followed by another layer of 8% (wt.) phosphorous doped oxide.

A sample was cross-sectioned and the oxide layers were studied at a polysilicon step. Figure 19 shows a cross-sectional view when etched with two seconds 20/1 and six seconds KOH. The initial phosphorous doped layer cannot be seen well near the polysilicon layer since both layers are recessed. Since that etch sequence did not work well, the sample was repolished and

etched with common oxide. With this sample pre-
paration the oxide layers are better differenti-
ated as shown in Figure 20.

Thus, by choosing the appropriate etch to
affect the oxide layers in question, the problem
at hand was solved in a timely manner.

Layer Structure

During investigation of different top pas-
sivation layer types, the layer type and structure
for a certain device needed to be determined.
The device was cross-sectioned and etched with
two seconds 20/1 and fifteen seconds common oxide
etch. Observation of the cross-section with the
electron beam normal to the surface indicated
there were two layers, as shown in Figure 21.
The relative thickness can be determined from the
micrograph but one cannot tell which layer is re-
cessed greater. By rotating the sample slightly,
as was done in Figures 15 and 16, one can make
a better judgement as shown in Figure 22. The top
layer is recessed greater than the thinner bottom
layer. It was concluded that the top layer was a
phosphorous doped oxide and the bottom layer was
an undoped oxide or a silicon nitride.

Further analysis using energy dispersive
spectrometry (EDS) and secondary ion mass spec-
trometry (SIMS) confirmed that the top layer is
4% (wt.) phosphorous doped oxide and the bottom
layer is an undoped oxide.

Step Coverage

Step coverage of the aluminum (or other
process layers) at various steps and contacts is
a very important parameter. Step coverage is
dependent not only on the metal system used but
also on the underlying topography. During mea-
surement of contact step coverage, the step cov-
erage must be measured at the center of the con-
tact; using the method outlined earlier will
guarantee a cross-section through the middle of a
contact. With the conventional cleave and stain,
microsectioning a specific contact in the middle
is hit and miss at best. An example of a cross-
section for step coverage measurement at a speci-
fic contact is Figure 23 showing an open aluminum
line at a diffusion contact. This contact was
not covered by the top passivation layer while
all other contacts on the die were protected.
During normal fabrication processes this particu-
lar contact was exposed to additional etching
which thinned the metal layer at the contact
oxide step. The passivation layer present in
Figure 23 was deposited just prior to micro-
polishing to protect the aluminum layer during
polishing. Thus, using the technique outlined
here, a specific contact was easily microsec-
tioned for step coverage measurements and study.

The effect of topology and complicated steps
can be studied as shown in the sequence of Figure
24. The feature studied is an aluminum step over
a polysilicon layer (poly II) which steps over
another polysilicon layer below it (poly I) run-
ning perpendicular to poly II. Running parallel
to poly I and above poly II is the aluminum layer
which must cover the poly II-poly I step. In
Figure 24a we see poly II before it encounters
poly I. In Figure 24b poly II is in transition,
making the step up onto poly I. The area below the
poly II level is the edge of the actual poly II
step over poly I. In Figure 24c poly II is situ-
ated over poly I which is now visible. With this

series of cross-sections one can see that ade-
quate metal coverage is maintained. The width
of the aluminum line in this example is less than
4μm. Since the three sections shown in the above
example were performed on the same metal trace,
sectioning resolution of nearly 1μm is demon-
strated.

Summary

A technique for cross-sectional analysis of
a specific area has been presented. The technique,
using commonly available laboratory materials,
requires no encapsulation or apparatus specially
built for cross-sectioning or cleaving. Two
stages of polishing are used: a rough polish to
get near the area of interest and a final polish
to obtain the specific area cross-section. Sample
preparation is minimal, which makes this technique
rapid.

The tilt and attitude angles of the micro-
section will affect measurements performed on the
microsection. It was shown that for an angle of
18° an error of 5% will exist. Actual polishing
experience shows that the attitude and tilt angles
are less than 18° in most situations.

Structure delineation using 20/1, KOH and
common oxide etches was studied. Etch type and
order will change the final cross-section. The
information needed will dictate what etch type
will be used. In general, two seconds 20/1
followed by six seconds KOH works well; for gate
oxide measurements fifteen seconds of common
oxide etch is preferred.

Recession of layers by each etch was studied
and verified by observation of etched samples
rotated to a grazing angle with respect to the
electron beam.

Examples of cross-sections produced by the
technique and experiments where different etching
sequences were required were presented. This in-
cluded cross-sectioning a specific bit in a 64K
DRAM and aluminum step coverage at a specific
contact and step.

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Discussion With Reviewers

J.R. Beall: Are all cross-sections coated for SEM examination?
S. Joens: After you have completed your sample preparation, are the samples coated for conductivity before SEM examination?
Authors: No, samples are not coated before examination with the SEM. All sections in this paper are uncoated except for Figures 15 and 16. Coating is only used if absolutely necessary to reduce charging and improve resolution. Coating can obscure small features and eliminate contrast mechanisms.

S. Joens: At what accuracy can you control your rate of final polish? How small of an area of interest can you polish through?
J. Devaney: Can you section a particular-small $\cong 2\mu m$ area on a single die?
Authors: Yes, sections have been performed on a particular structure with a diameter of less than 1μm. In addition, as many as eleven sections have been performed through a particular aluminum line 3.5μm wide at a specific location. In the text, Figures 24a, 24b and 24c are three sections within a distance of less than 4μm on a single die sample.

J. Devaney: Do you make your etches fresh each time and what is their shelf life?

J.R.Beall: Are the reported etch times shelf life dependent?
Authors: No, etches are not made up fresh each time. Etches are prepared in small enough quantities (<30ml) such that the stock is depleted before degradation occurs. KOH may be stocked for up to a year. Acid mixtures, such as 20/1, kept in plastic bottles should be replaced monthly.

J.R. Beall: Are the reported etch times process dependent?
Authors: Yes, etch times are affected by the process. Etch times given in the text are typical for the samples produced in-house. The etch time will depend on dopant levels and density of the processed layers.

J. Reimer: What is the approximate total time for sectioning and etching a sample as shown in Figure 18?
Authors: Figure 18 is not a microsection through a specific memory cell. Since the memory cell structure is repeated, the rough grind and polish could be performed and then inspected under a high magnification light microscope to verify that a memory cell structure has been microsectioned. This would result in a sectioning and etching time of less than ten minutes. When a specific location is prepared, as in Figure 17, the preparation time is longer. Since a specific, one of a kind, area is to be sectioned one must be careful and make more frequent high magnification inspections using the light microscope. The section performed in Figure 17 through a specific memory cell was prepared in less than one hour. The distance remaining from the edge of the rough grind to the desired structure is another determining factor in the amount of time required for sample preparation.

J. Reimer: You mention that you polish a sample by holding it at an angle, θ, of 45° (Figure 4). Also, with your references 4,5 you imply that you are not using a special apparatus to polish a sample. Please comment on how you maintain holding a sample in place during polishing at a 45° angle without using some kind of fixture for control.
J.R. Beall: How is realignment accomplished when a cross-section is interrupted, inspected and then continued? What type of support is used to hold the chuck during grinding and polishing?
Authors: No special apparatus or fixture is used to hold the sample (and X-ACTO holder) in place during polish, it is simply held with the hand. This provides adequate control of placement for realignment of the sample after inspection. The angle, θ, of 45° is a recommended angle and can vary somewhat since the nap of the polishing wheel is inducing the normal polished edge of the sample. Only when the angle θ becomes too small (≅30°) or too large (≅60°) are artifacts introduced.

J. Devaney: What speed do you use on your polishing wheels?
Authors: Polishing wheel speeds are variable, normally 800 RPM is used.

J.R. Beall: What are the typical beam voltage and current used?

Authors: The typical beam voltage is 20kV with a beam current of about 4×10^{-11} A.

J. Devaney: Do your etches also attack the die surface, damaging its structure?

Authors: Yes, the die surface is attacked by the etch as discussed in the etch considerations section and shown in Figure 11, view 'd'. For most studies this is insignificant and does not damage the structure. In those cases where it may affect the data the surface may be protected by a layer of gold. The layer of gold may be selectively deposited only on the circuit surface but not the polished edge by facing the polished edge away from the basket filament during gold evaporation. Another method of protecting the surface is applying a thin layer of clear fingernail polish before sectioning and removing the fingernail polish, after sectioning, using methanol.

Simon Thomas: One has to be extremely cautious in measuring gate oxide thickness (typically now $\cong 200$Å) using cross-sectioning/SEM. In view of the limited resolution ($\cong 60$-100Å) in commercial SEM's and the presence of two "ridges" on either side of the oxide, the oxide thickness measurement is subject to significant error (Figures 9a, 10, 19 and 20). What is the accuracy and precision in the gate oxide thickness measurement from the authors' experience?

Authors: Yes, we agree that there is significant error in gate oxide measurements using the SEM. TEM cross-section is probably a superior method though sample preparation is much slower and very tedious. The discussion of the gate oxide measurement in the text was for thicker oxides and was to emphasize artifacts introduced during sample delineation.

S. Thomas: In Figure 10 please comment on the void (dark spot) in the oxide, close to the poly edge. How much of it is genuine and how much is accentuated by the HF etching?

Authors: The void is located at the intersection of four types of oxide, coverage may not be complete at this point. The void, though, is greatly exaggerated by the HF etch.

S. Joens: When polishing a sample for metal characterization, do you have difficulty with metal smearing? If so, how do you prevent this from occurring?

Authors: Yes, metal will smear if there is not a protective layer over the metal. In most cases there will be a layer of top passivation over the metal, often a layer may be added prior to polish as was done in the example of Figure 23. We have also experimented with using clear fingernail polish as a protective layer; further development is being done currently. Even with a protective layer, the metal may smear slightly but any evidence of smearing will be removed during delineation with KOH.

J. Reimer: In Figure 24c, aluminum covers the right side of P2 step at less than 50% of the nominal aluminum thickness value. While you consider this adequate, what is the minimum acceptable percent step coverage for the device shown?

Authors: Minimum acceptable step coverage specification is proprietary information.

J. Reimer: Please explain what further processing caused the open aluminum at the contact step shown in Figure 23 and why the aluminum was not protected by passivation glass at the contact step area of that particular contact only?

Authors: The particular contact in Figure 23 was the only contact on the die that was located within the top passivation bond pad opening. The further processing that caused the open aluminum at the contact step was part of the normal fabrication procedure which is proprietary information. Sample preparation did not cause the open aluminum.

S. Thomas: On comparison with Figure 10, the common oxide etching did not delineate the layers in Figure 20 too well, especially considering the very high phosphorous content in the PSG. Comments?

Authors: Yes, the contrast between the layers in Figure 20 is not as good as in Figure 10. The sample in Figure 20 was processed in a different manner than the sample in Figure 10.

S. Thomas: Please explain the irregular line present on the substrate below the transfer gate (but not under the capacitor) in Figure 17 but not in Figure 18.

Authors: The line in question is present on both samples but, because of the contrast of Figure 18, the line is not visible. The line is an artifact of the recession of the substrate below the field and gate oxide but is not apparent in the capacitor because of the implant directly below the gate oxide.

Reviewer 6: You mention that when one severely recesses various layers (especially the aluminum layer) during sample preparation that data is lost. Could you please give some examples?

Authors: Yes, an immediate example is the examination of multi-layered systems (e.g. a refractory metal layer overlaying poly) where the etchant used recesses all the layers involved such that only a void is left where the multi-layer system was. The structure, thickness and uniformity of the layers could not be studied. Also, aluminum doped with silicon is used extensively as a metallization layer. Silicon precipitates will form in the aluminum during normal processing. By using the correct etch and only recessing the aluminum slightly the position, size and linear density of the precipitate may be studied. This data would be lost if the metallization layer was severely recessed.