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ION BEAM INDUCED CHARGE MICROSCOPY OF INTEGRATED CIRCUITS

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Abstract

The ion beam induced charge (IBIC) microscopy technique has recently been developed as a means of imaging the depletion regions of working microelectronic devices beneath their thick metallisation and passivation layers. IBIC microscopy is analogous to electron beam induced current microscopy but has the advantages of a larger analytical depth, lower lateral scattering of the incident focused MeV ion beam and negligible charging effects. These characteristics enable IBIC to image small, buried active device regions without the need to remove the surface layers prior to analysis. The basis of this new technique is outlined and the applications for integrated circuit analysis, characterising upset mechanisms, and for imaging dislocation networks in semiconductor wafers are reviewed.

Key Words: Ion beam induced charge (IBIC) microscopy, integrated circuit analysis, ion-solid interactions, nuclear microprobe.

Introduction

In its most basic form, an integrated circuit device may be thought of as comprising a semiconductor substrate with a patterned array of pn junctions at the surface, which provides the depletion region associated with the various components, as shown in Figure 1a. Above this are thick patterned layers of insulators and metallisations which connect different regions of the device [17, 34]. These layers are deposited by a complex series of fabrication processes and there are many ways in which integrated circuits can fail, due to fabrication problems or during operation. It is important to have analytical techniques capable of determining the electrical and structural characteristics of devices in order to determine reasons for failure or unexpected performance [21, 30]. There are various modes of scanning optical and electron microscopy used for this, such as optical beam induced current (OBIC) [33], electron beam induced current (EBIC) [25], and voltage contrast microscopy [28]. Each has its own strengths but also its own associated problems, such as a shallow analytical depth, the inability to analyse under metallisation layers [28], sample charging or difficulties in relating the measured results to the device structure.

The use of the recently developed ion beam induced charge (IBIC) microscopy technique to overcome some of these problems is reviewed in this paper. The first IBIC images from integrated circuits were produced using the nuclear microprobe at the SPM Unit, University of Oxford in 1991 [4, 5] and several other nuclear microprobe groups have since started work in this field. Results obtained using the Oxford and Melbourne nuclear microprobes, from work in refs. [3, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14], are given here to illustrate the capabilities of IBIC microscopy; work by other groups is reviewed in **Single Event Upset Analysis** and **Other Uses of IBIC Microscopy**. It is beyond the scope of this paper to cover more than the basic aspects of the generation of IBIC images and its applications; for all aspects of IBIC microscopy and other aspects of materials analysis using a nuclear microprobe see ref. [15].

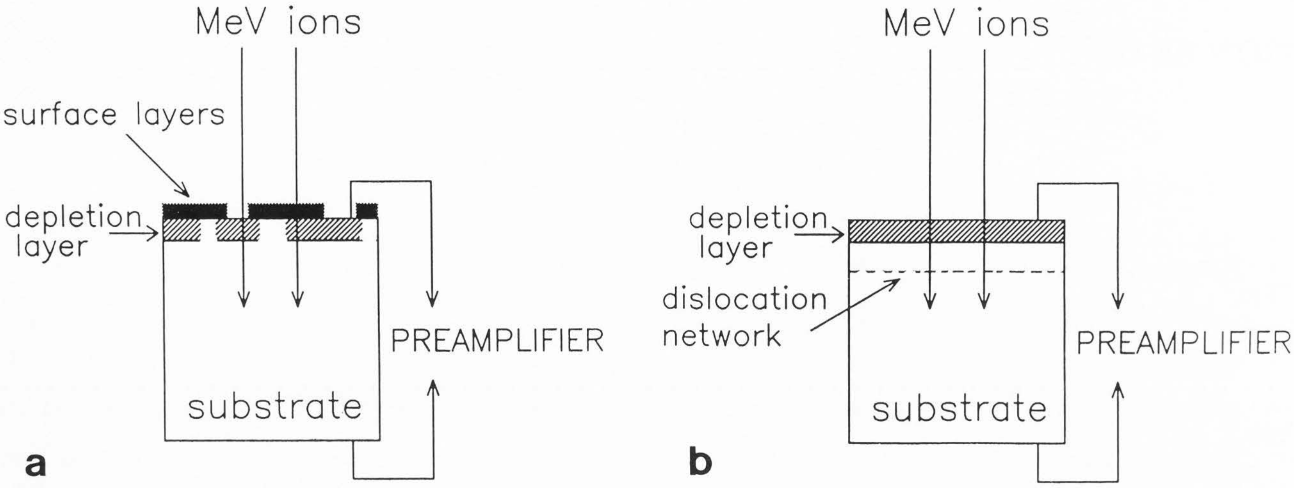

Figure 1. Schematic geometry used for IBIC analysis of (**a**) integrated circuits and (**b**) semiconductor wafers. The charge sensitive preamplifier is connected to the device pins of interest in (a) and across the front and back wafer surfaces in (b).

The IBIC technique utilises a nuclear microprobe to focus MeV light ions to a spot size of about 100 nm on the surface of an integrated circuit. A nuclear microprobe [15, 18] has many similarities with a scanning electron microscope, except that it uses a series of powerful magnetic quadrupole lenses to focus MeV ions, instead of keV electrons. The higher energy and mass of the MeV ions necessitates the use of quadrupole lenses, rather than axially symmetric electron lenses, and there has been much work over the last twenty years in devising the best configuration and quality of lenses to focus MeV ion beams to smaller spot sizes [15, 18, 36]. The increased complexity of a nuclear microprobe, compared, for example, with the scanning electron microscope, is rewarded when considering the interaction of the MeV ion beam with the sample, since the use of MeV ions enables high spatial resolution analysis through thick device layers with no sample charging problems, as described in **Comparisons of Different Aspects of IBIC**.

Practical aspects of IBIC image generation are fully described in ref. [15]. However, it suffices to say that the main experimental difference compared with other modes of beam induced current microscopies, such as EBIC and OBIC, lies in the method by which the electron-hole charge carriers are detected. On average, 3.6 eV is needed to create an electron-hole pair in silicon, irrespective of the type of ionizing radiation [22]. Each incident electron for EBIC (typically with an energy of less than 20 keV), and each photon for OBIC, creates a relatively small number of charge carriers, which cannot be resolved from the noise level. With these two techniques, images are produced by displaying the variation in the current of charge carriers induced by a large, continuous incident beam (typically 1-100 pA for EBIC) in order to increase the measured signal size above the noise level. With IBIC, however, each incident MeV ion creates such an enormous number of charge carriers that the charge pulses produced by each incident ion within the semiconductor material can be resolved from the noise level. To researchers unfamiliar with charged particle detection in accelerator laboratories, this may sound difficult. But in practice, IBIC experiments utilise standard charged particle detection electronics which are readily available. Since individual charge pulses are measured with IBIC, the incident ion beam current is very low in order that the separate ion induced pulses can be measured using nuclear microprobe data acquisition systems. Such systems are capable of measuring up to 20,000 charge pulses per second, and in most IBIC analyses to date, a typical beam current of 1 fA (6000 ions per second) has been used. This very low focused beam current is produced using extremely small object and collimator apertures, which enables focused beam spot sizes on the sample surface of about 100 nm [15]. The charge pulse data used to produce IBIC images are collected for 5 to 10 minutes using this beam current.

Comparison of Different Aspects of IBIC

Topographical contrast for different ions

Figure 2a shows the rate of electronic energy loss (i.e., that fraction of the beam energy which creates electron-hole charge carriers within the semiconductor) as a function of distance travelled in silicon for 2 MeV H^+ ions (protons), 3 MeV $^4He^+$ ions (α-particles),

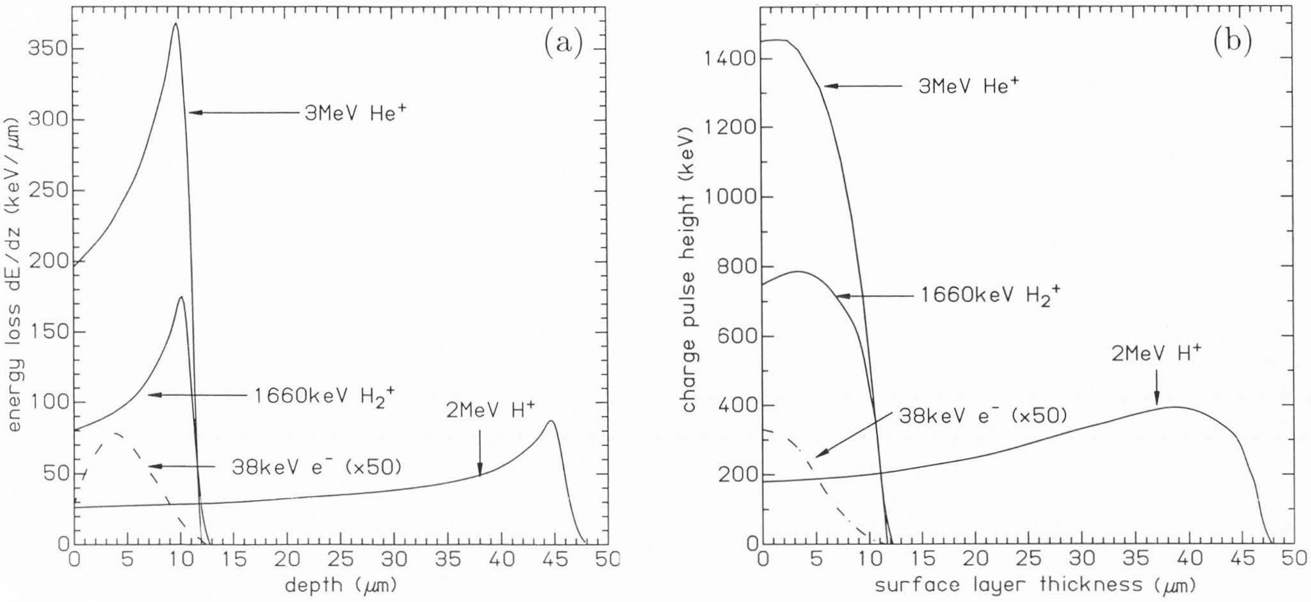

Figure 2. **(a)** Rate of electronic energy loss as a function of distance travelled for 3 MeV He$^+$ ions, 1660 keV H_2^+ ions and 38 keV electrons (these three particles all have the same range) and 2 MeV H$^+$ ions (protons). **(b)** Calculated charge pulse height resulting from a depletion layer thickness of 1 μm and a minority carrier diffusion length of 6 μm, as a function of increasing surface layer thickness for the same incident charged particles as (a).

1660 keV H_2^+ ions (molecular hydrogen), and 38 keV electrons. These charged particle energies were chosen such that three of them have the same range, which enables changes in their energy loss to be directly compared. These ion energies are typical of those commonly available for nuclear microprobes. The rate of ion energy loss increases gradually towards the end of range and then abruptly decreases to zero. In comparison, the keV electrons produce a more smoothly varying energy loss curve with no flat region and no sharp cut-off at the end of range.

The sensitivity of these different types of charged particles to variations in device surface layer thickness is important to characterise properly since it is essential for correctly interpreting and quantifying the observed IBIC image contrast, and also for comparing the merits of using each type of particle. All these charged particles lose different amounts of their energy in passing through the surface layers, which reduces the number of charge carriers which they create in the underlying semiconductor, and consequently alters the measured charge pulse height. Figure 2b shows the calculated charge pulse height, in keV, resulting from a depletion layer thickness of 1 μm and a substrate diffusion length of 6 μm as a function of increasing surface layer thickness. So, for an incident ion with an energy of 2 MeV, a charge pulse height of 1 MeV means that half of the ion energy has produced charge carriers in the semiconductor which are measured. The measured charge pulse comprises carriers created in the depletion region by the incident ion and also a fraction of carriers created in the substrate which diffuse to the depletion layer, as described in ref. [3]. The number of carriers from the substrate which can diffuse to the depletion region depends on the diffusion length, which depends on the substrate defect density. A short diffusion length indicates a high defect density, which causes many diffusing charge carriers to become trapped and recombine, and consequently are not collected at the depletion region, whereas a long diffusion length means the opposite. Complete charge collection within the depletion layer is assumed here, and the rate of electronic energy loss of the charged particles, which is responsible for generating charge carriers, is shown in Figure 2a. Figure 2b thus gives a guide of the sensitivity of the different charged particles to changes in the thickness of the device surface layers, i.e., the device topography and structure.

For 3 MeV $^4He^+$ ions, the maximum slope of the charge pulse height variation as a function of varying surface layer thickness is a hundred times greater than that obtained with 2 MeV protons (which have a much greater range). This difference in the sensitivity to changes in surface layer thickness demonstrates the enormous differences in sensitivity to device topography using different types of MeV ions, arising because of the greatly differing rates of energy loss close to the surface. With MeV protons, the measured charge pulses are nearly independent of the thickness of the surface

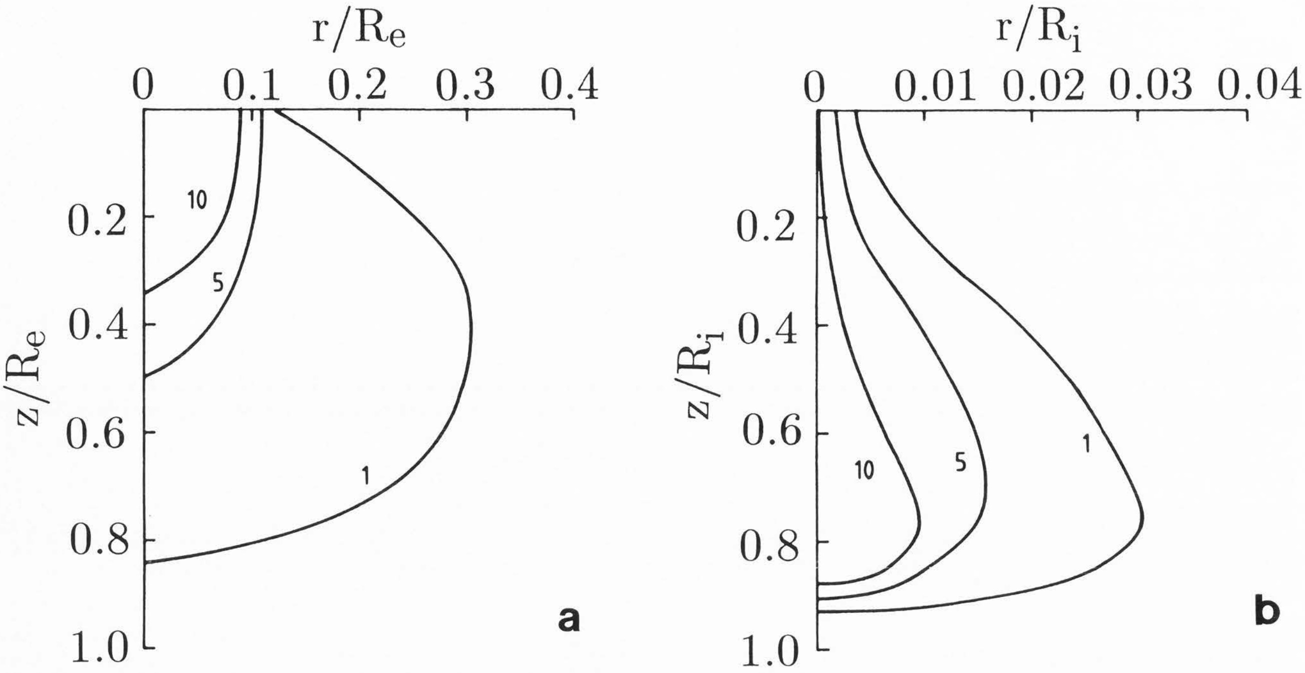

Figure 3. Comparison of the charge carrier generation volumes for (**a**) 10 keV electrons and (**b**) 3 MeV protons in silicon. Both are displayed in profile as a function of particle penetration depth (z) and the radial beam extent (r) normalised to the electron range (R_e) and the ion range (R_i). The numbers 10, 5, 1 refer to the intensity of the charge carrier contours.

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layers. The measured charge pulses depend only on the thickness of the underlying depletion region and the minority carrier diffusion length of the substrate. With heavier ions, such as MeV $^4He^+$ ions, the measured charge pulses strongly depend on device topography as well as the underlying electrical properties. Examples of this are given in **IBIC Analysis of Integrated Circuits**.

With EBIC microscopy, a current gain induced by a steady beam current of keV electrons is measured rather than individual charge pulses, since these would not be resolved from the device noise level, which is typically 50-100 keV on the scale shown in Figure 2. However, in Figure 2, the charge pulse height from a single 38 keV electron is shown on the same scale as for MeV ions to compare the sensitivity of EBIC to changes in surface layer thickness. There is no sharp variation in the resultant charge pulse height because the incident electrons have no well-defined range. The maximum gradient of the charge pulse height variation is larger than for protons and smaller than with MeV $^4He^+$ ions. Thus, whereas IBIC can be made either sensitive or insensitive to topographical contrast by the choice of different types of incident ions, ERIC (and OBIC) do not have this flexibility and it can be difficult to distinguish effects in the resultant images caused by the device topography and the underlying electrical properties.

Beam spreading

Figure 3 compares the charge carrier generation volumes for 10 keV electrons and 3 MeV protons in silicon. Because of their light mass, keV electrons are heavily scattered in collisions with the atomic electrons of the material, resulting in a generation volume of charge carriers which is approximately spherical [29]. In comparison, MeV ions are much heavier so they are more difficult to deflect in collisions and undergo much less lateral scattering. Their generation volume can be thought of as a "teardrop" shape, in which lateral scattering can be ignored in the first part of the ion trajectory and is only significant close to the end of range. It is this property which gives IBIC the ability to analyse buried layers with high spatial resolution.

Sample damage

The other major consideration in assessing the merits of different ions for IBIC microscopy is the rate of damage of the sample by the incident ions, which alters the measured charge pulse height spectrum and consequently the observed image contrast. Each incident ion displaces a few atoms in the semiconductor away from their original lattice site. The resulting lattice vacancy and displaced atom act as sites for trapping and recombination of ion induced charge carriers, causing a reduction in the semiconductor diffusion length with cumulative beam dose, as described in ref. [15]. Ion induced damage may become detectable in IBIC images after doses as low as 10^9 to 10^{11} ions/cm^2. This is the major drawback with IBIC microscopy, with no comparable problem in EBIC and OBIC since the incident electron beam energy and laser wavelengths are respectively too low to cause significant displacement damage within the device.

There has been considerable recent efforts devoted to understanding the effects of ion induced damage for IBIC microscopy. The result of this is that IBIC can still give quantitative analysis, even in the presence of damage [3, 11, 14], partly because of the highly sophisticated manner in which data can be collected and also because of the greater understanding of how ion induced damage affects the measured charge pulse data. As a result of this, several IBIC images can be produced from the same device area, and interpreted in terms of the device characteristics.

In general, charge carriers generated in the depletion region have a much lower recombination probability than those generated in the substrate, because they move much faster due to the associated electric field of the depletion region. This reduces the probability of the charge carriers being trapped and recombining at the ion induced defects in the depletion region. This principle has been used to substantially reduce the effects of ion induced damage in IBIC images by optimising the beam energy and ion type so that the majority of ions are stopped within the device depletion regions, where they cause little effects of ion induced damage (see ref. [14] for more details). This leads to the surprising situation that while heavier ions create more defects than lighter ions, a lighter ion beam may result in more observable effects of damage than a heavier ion beam of the same energy, since the heavier ions are producing a majority of defects in the depletion layer whereas the lighter ion produce the majority of defects in the substrate.

Any beam induced sample damage is, of course, a drawback to an analysis technique, and in this respect IBIC compares unfavourably with EBIC and OBIC microscopy. However, with IBIC there is no need to strip off thick surface layers for analysis of the underlying semiconductor properties, whereas there frequently is with EBIC and OBIC microscopy owing to insufficient analytical depth. It is thus debatable as to whether IBIC is a more destructive method of analysis, since there is still a fully intact device structure after analysis. In addition, since individual ions are used to produce individual charge pulses, rather than a large continuous beam current, there are no problems of sample charging which is a common problem for EBIC microscopy, particularly for devices with surface passivation layers. Also, individual ions do not cause any effects due to local beam heating which can also be a problem with other modes of beam induced current microscopies.

IBIC Analysis of Integrated Circuits

This section shows results which highlight some of the characteristics of IBIC microscopy described above for the analysis of integrated circuits. It should be noted that the ability to produce IBIC images from an integrated circuit necessitates an uninterrupted, electrically conducting path from the region of interest to the relevant device data pins. Some device regions do not lend themselves for this type of analysis since they may be only accessible through latches or buffers that must be opened with suitable clocking or current sourcing. This procedure may introduce an unacceptable amount of noise for IBIC analysis.

Output driver of a EPROM memory device

The first device structure used to demonstrate the formation and interpretation of IBIC images was a working EPROM (erasable programmable read only memory) circuit [5]. The region studied was part of the output driver circuitry for one of the data pins located around the memory field. This region has a 1 μm thick aluminum metallisation connected together in an interdigitated structure and there are connections to the doped silicon substrate via the small circular depressions along the length of the horizontally-running metallised regions. Underneath these are the pn junctions associated with the separate drains and source regions of the individual field effect transistors (FETs). There is a 1 μm thick passivation layer on the device surface and the average surface layer thickness in this area is about 3 μm.

Figure 4 presents three 300 μm x 300 μm IBIC images of this device, generated using 2 MeV protons, together with a secondary electron micrograph of the same area in the lower right corner. These three IBIC images all show the same area of the fully functioning device, but with different connections and pin voltages in each case. On these images, dark regions represent areas of large measured charge pulses and light regions represent areas of small measured pulses. The dark regions correspond to those regions where the incident protons pass through pn junctions comprising the sources and drains of the individual transistors within this device area which are connected to the detection electronics. Some device regions appear as regions of large charge pulses in some images and are absent in others, depending on the device conditions used in each case. Using such images, the switching behaviour of the working device structure beneath the surface layers can be studied by varying the device pin voltage levels.

Figure 5 compares the IBIC images obtained from the same device area as in the central region of Figure

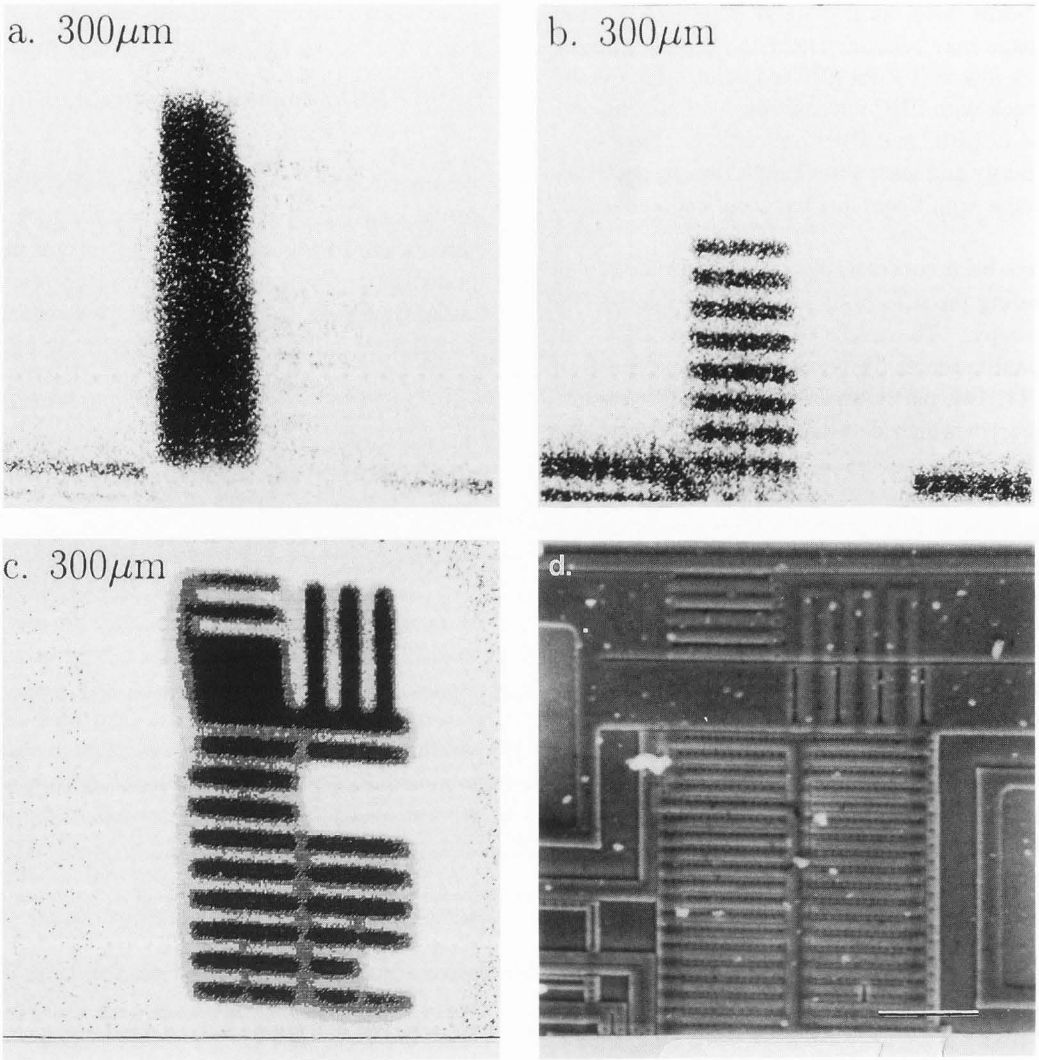

Figure 4. Three 300 μm x 300 μm IBIC images (**a**, **b**, and **c**) of the same area of a EPROM device recorded with different connections and pin voltages to the fully functioning device. (**d**) A plan view secondary electron micrograph of this same device area (bar = 50 μm).

4, using the same device connections in both cases, but with two different incident ions. Figure 5a was generated using 2 MeV protons (range of 45 μm in silicon) and Figure 5b using 2 MeV He$^+$ ions (range of 7 μm in silicon). The darker regions in Figure 5a correspond to those horizontally-running pn junctions beneath the metallisations which are connected up to the detection electronics. There is no IBIC contrast arising from the device topography, as can be seen by the absence of any indication of the circular contact holes along the metallisation fingers which are visible in the central region of the scanning electron micrograph in Figure 4d. This makes the resultant IBIC image easy to interpret in terms of the electrical device structure, since the contrast is not complicated by any effects of the device topography. In Figure 5b, the contact holes along the horizontally-running metallisation fingers are now visible, as are the gaps between the individual metallisation fingers. Indeed the topographical contrast in this image recorded using MeV He$^+$ ions is so strong that the contact holes can be seen in the lighter grey region in the lower half of the figure, which corresponds to a pn junction which is not connected up to the measurement electronics, and is only visible through lateral charge diffusion into those collecting junctions which are connected.

Memory field of a PROM device

This device is a 16 Kbit mask programmed PROM, and the IBIC results are presented and interpreted in more detail in refs. [14, 15]. This work encompassed

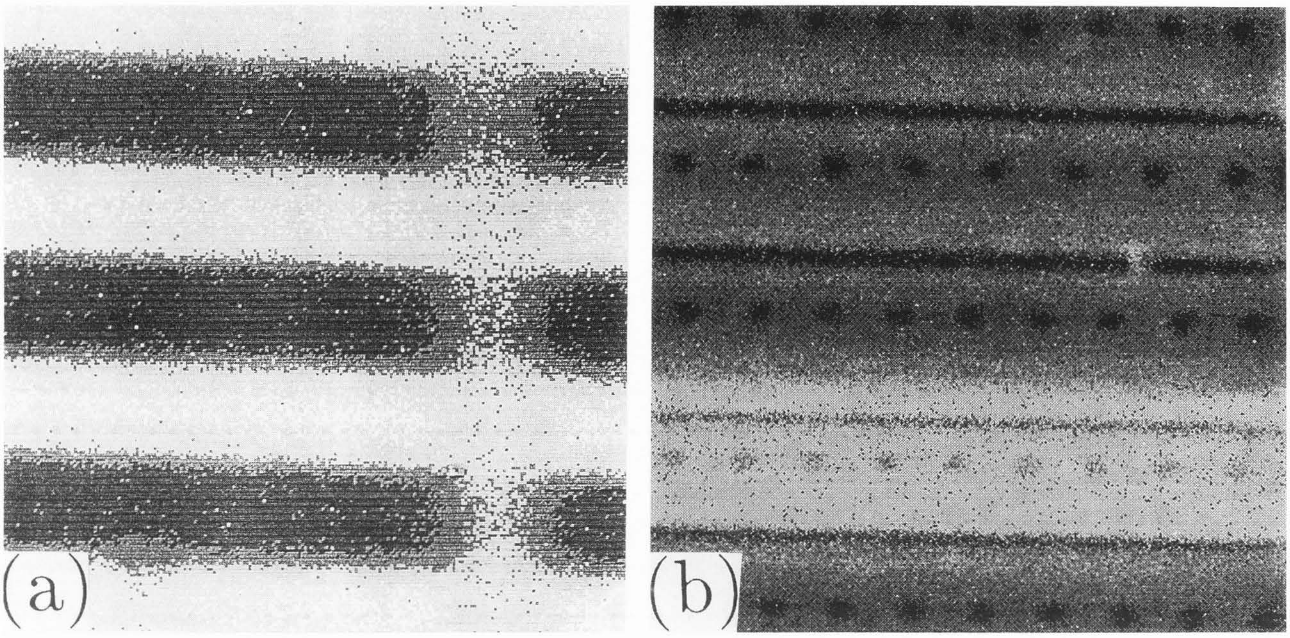

Figure 5. IBIC images showing the variation of the average charge pulse height from the central region of the EPROM device images shown in Figure 4. (**a**) A 75 μm x 75 μm region generated using 2 MeV protons, and (**b**) a 40 μm x 40 μm region generated using 2 MeV He$^+$ ions.

a thorough study into the different IBIC image contrasts, rates of damage and different interpretations using several different types and energies of MeV ions.

Figure 6 shows a plan-view schematic of a region of the device memory field, and a cross-section through the line labelled AA'. Figure 7a shows a plan-view, and Figure 7b shows a cross-section scanning electron micrograph also through the memory field. This area has a 1 μm thick phosphorous-doped glass passivation layer over the surface. The hexagons shown in Figure 6 and Figure 7a are 600 nm thick polysilicon gate regions of the field effect transistors which make up the memory elements: the drains are inside the hexagons and the source regions are outside them. Underneath the hexagonal gates there is an undoped field-free region which controls the operation of the field effect transistors. The vertically-running strips shown in Figure 6 and Figure 7a are 1 μm thick aluminium metallisations which are alternately connected to the device source regions (and thence to ground) and drain regions. The metal drain lines run through the centres of the hexagonal gates and the source metal lines are located between the hexagons. The n$^+$ drain and source regions are 0.5 μm deep and these lie within a P well diffusion region which extends between a depth of 4 to 5 μm beneath the semiconductor surface, as can be seen on the cross-section schematic in Figure 6 and the cross-section scanning electron micrograph in Figure 7b.

The charge preamplifier used to make these IBIC measurements was connected between the transistor drains and ground, so charge pulses generated from the drain regions of the device were detected, but not from the source regions which were at ground potential. Charge carriers generated in and around the P well were also measured, since this depletion layer is connected to the preamplifier.

The IBIC images in this section are displayed in a different manner compared with all the others in this section. Figures 8 and 9 show sequences of IBIC images displaying the measured number of counts within the scanned area for different "windows" on the measured charge pulse height spectrum, produced using 2 MeV He$^+$ ions in both cases, so the observed contrast arises from both the distributions of the surface layers and the underlying junctions. The scanned area in Figure 8 was a 500 μm x 500 μm region between the two memory fields of the device, showing different parts of the controlling logic circuitry in different map windows. By analysing the way in which such sets of IBIC images change under different device conditions, the various logical connections can be studied.

Figure 9 shows a similar sequence of IBIC images from a 40 μm x 40 μm area of the memory field shown in Figures 6 and 7, from a region at the right hand edge of the area shown in Figure 8. Map 2, which was extracted from the smallest measured charge pulses, shows

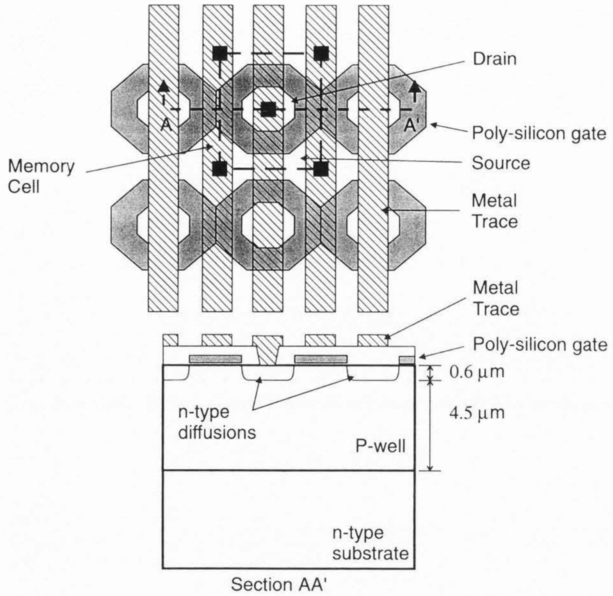

Figure 6. Schematic plan view of the memory field and cross-section through the line labelled AA'. A single memory cell is indicated by the dashed box.

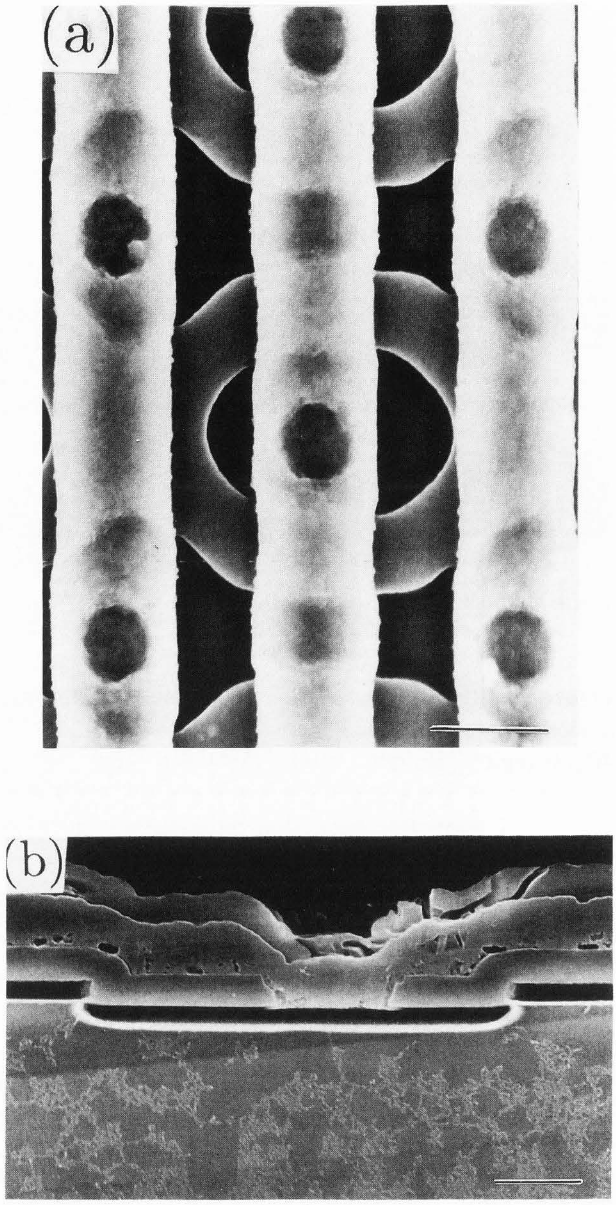

Figure 7. **(a)** Plan view and **(b)** cross-section secondary electron micrographs of the PROM memory field. The n-type diffusion call be seen in (b), located at a depth of 0.5 μm within the P well, which is 4.5 μm deep. Bars = 5 μm (a) and 2 μm (b).

Figures 8 and 9 (on the facing page). IBIC images showing the variation in charge pulse intensity from 500 μm x 500 μm (**Fig. 8**) and 40 μm x 40 μm regions (**Fig. 9**), generated with 2 MeV ^{4}He$^+$ ions, for different "windows" on the measured charge pulse height spectrum. The window using the smallest measured charge pulses is in the top left (map 2 in Fig. 8, and map 1 in Fig. 9) and the window using the largest pulses in the bottom right (map 7 in Fig. 8 and map 8 in Fig. 9). Dark and light regions represent large and small measured number of pulses, respectively.

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regions around the edges of the drain and source contact holes in the vertical metal strips, the edges of the vertical strips, a few uncontacted drain regions and source regions (thin horizontal regions between the vertically adjacent hexagonal gates). The other maps extracted from progressively larger measured charge pulses show other features such as the drain and source contact holes in map 4, and different portions of the hexagonal gates. The vertically-running metallisations are regions where the surface layer coverage is thickest and no counts are detected from ions passing through these regions except at the drain and source contact holes in map 4, where the surface layers are thinner. In maps 2 and 3, asymmetric dark contrast can be seen around the contact holes in a vertically-running metallisation strip just to the left of centre. This shows evidence of a possible problem in the deposition of one of the layers within this structure, and demonstrates the power of IBIC in detecting such faults in buried layers.

IBIC images of a GaAs HEMT device

Figure 10 shows IBIC images of a high electron mobility transistor (HEMT). The device was fabricated as an n-type GaAs/AlGaAs heterostructure which acts as a two-dimensional electron gas. The surface of the device was patterned with a dose of Be$^+$ ions which formed p-type material and resulted in the formation of a field effect transistor with a very narrow gate depletion region which was confined both literally and in depth.

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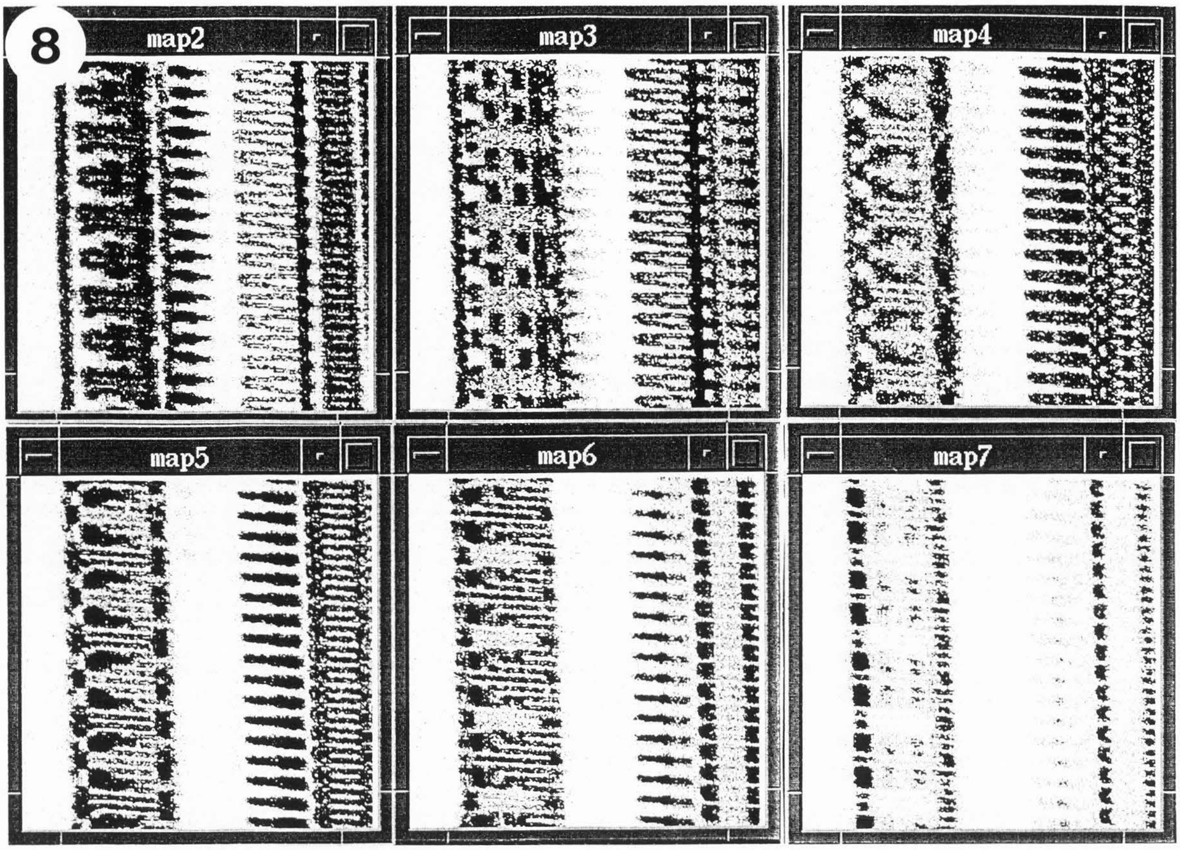

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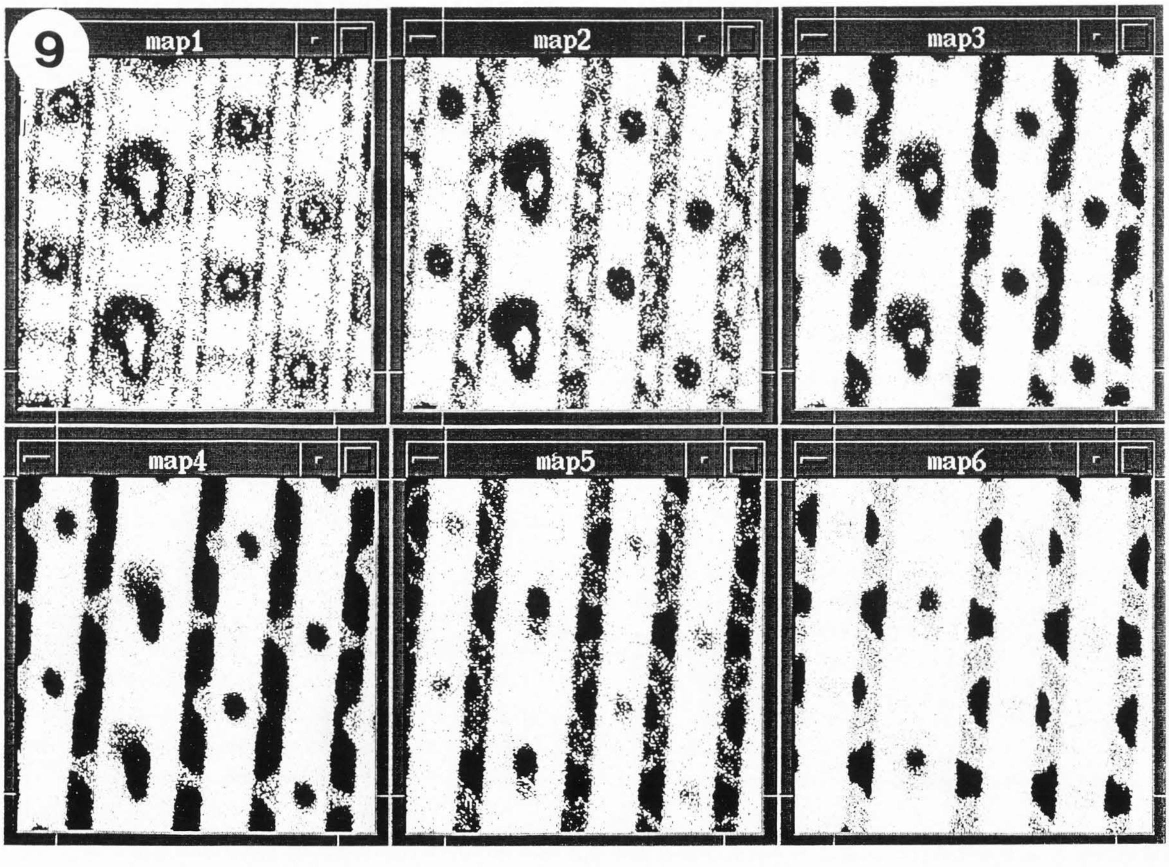

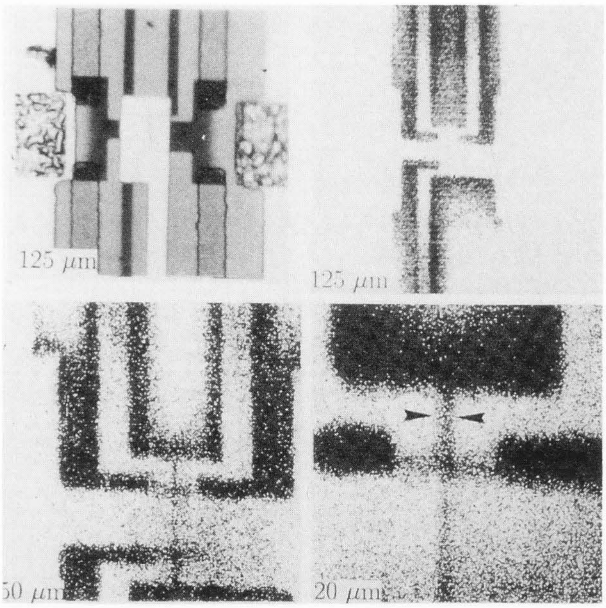

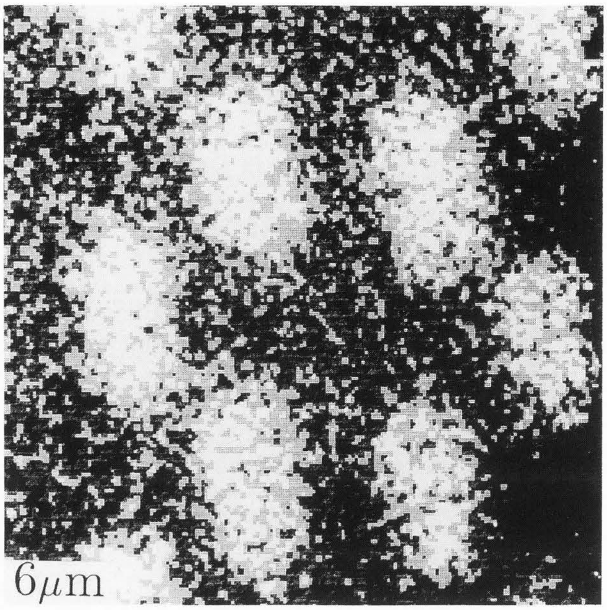

Figure 10 (at left). Optical micrograph of the GaAs device, and three IBIC images with scan sizes shown in the lower left corner. A 0.8 μm wide depletion region is indicated in the highest magnification image.

Figure 11 (at right). A 6 μm x 6 μm IBIC image of the DRAM memory field showing the individual trench cells.

The IBIC images were generated using contacts between the p- and n-type materials, with a 10 μm thick aluminum foil placed between the focused 3 MeV proton beam and the device surface. On the 20 μm x 20 μm IBIC image, a 0.8 μm wide depletion region is arrowed, demonstrating that high spatial resolution IBIC analysis is possible through thick surface layers due to the low lateral straggling of the focused MeV proton beam [9].

IBIC images of DRAM trench cells

IBIC images of a 4 Mbit dynamic random access memory (DRAM) with 1 μm wide trench cells have also been produced. The doping concentration of the p-type silicon substrate was ~ 2 x 10^{15} cm^{-3} and the area ~ 100 nm around the 1 μm holes was heavily n-doped. To prepare a sample suitable for IBIC microscopy, all the device surface layers were removed, leaving just the p-type substrate and the n-doped trench walls. Electrical contacts were produced by depositing a thin gold layer onto the back surface to form an ohmic contact and a thin aluminum layer onto the front surface to form a Schottky contact, similar to the geometry shown in Figure 1b. Figure 11 shows a 6 μm x 6 μm IBIC image of the DRAM memory field and the individual trench cells are clearly resolved. This work is described in more detail in ref. [9].

IBIC Images of Dislocation Networks

IBIC microscopy has also been used to image bands of misfit dislocations in a 4 μm thick epitaxial layer of $Si_{0.875}Ge_{0.125}$ grown on a Si substrate [10]. This $Si_{0.875}Ge_{0.125}$ layer thickness is greater than the critical thickness at which misfit dislocations are generated to relieve the strain induced by the lattice mismatch, and so interface dislocations are present to relieve the strain. A Nomarski optical micrograph of the sample is shown in the upper half of Figure 12; the dislocations can be seen as faint dark lines running along the horizontal [110] and vertical $[\bar{1}10]$ directions.

A thin gold layer was deposited on the front surface to form a 2 mm diameter Schottky barrier, and a gold wire was connected to this using silver loaded paint to form the front connection to the sample, as shown in Figure 1b. The back face was attached to the microprobe sample holder using silver loaded paint to make the ohmic contact. Capacitance-voltage measurements showed that the network of dislocations at the $Si_{0.875}Ge_{0.125}$/Si interface was outside the depletion region.

Two IBIC images of this sample are shown in the lower half of Figure 12. On these images, there are bands visible running along the [110] and [110] directions, and dark areas represents a high number of measured charge pulses and light areas represent a low number of measured charge pulses. The interpretation of the image contrast is that the dark areas represent regions of low dislocation density whereas the light regions represent regions of high dislocation density. The minimum

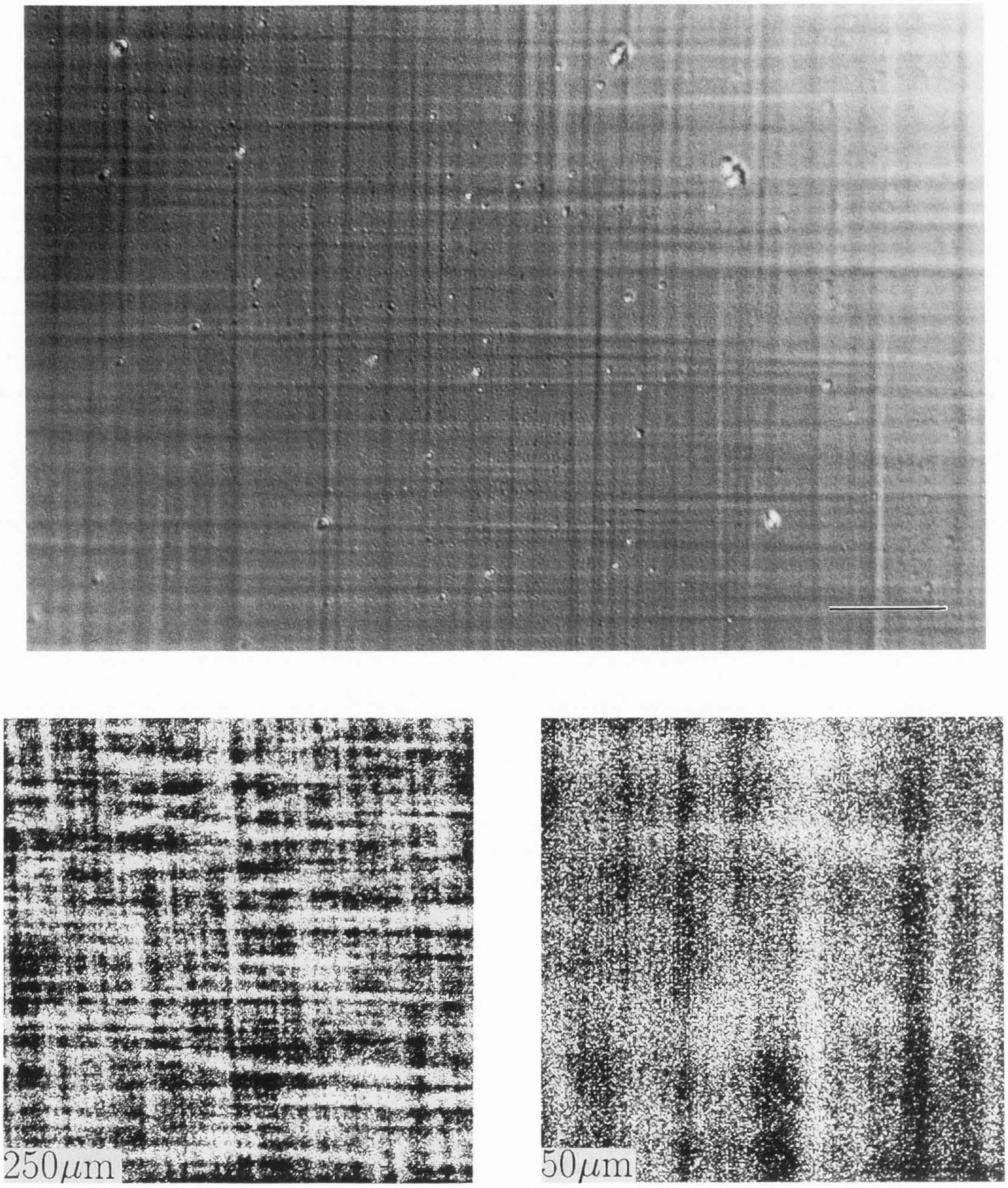

Figure 12. **Top**: Nomarski optical micrograph of $Si_{0.875}Ge_{0.125}$/Si sample (bar = 25 μm). **Bottom**: Two IBIC images of the sample, with the scan sizes shown in the bottom left corner of each image.

resolvable band width in the 50 μm x 50 μm image was 0.8 μm. Further work on this same material showing the dependence of the observed IBIC image contrast on the crystallographic orientation of the dislocation network as well as the electrical properties is described in ref. [13]. This is important, as it shows that IBIC may be able to determine the burgers vector of the observed dislocations, which is not possible with EBIC or OBIC since the distribution of charge carriers produced with them does not depend on the crystallographic orientation of the sample.

Single Event Upset Analysis

As integrated circuit features continually shrink, the amount of charge which defines the different logic levels becomes smaller, i.e., the charge generated by the passage of ionizing radiation through the device is more likely to cause a change in its state (called a soft upset, or a single event upset) [2, 23, 27]. This is a serious problem in the design of high density semiconductor memories, particularly for satellite-based devices which are exposed to a high flux of cosmic ionizing radiation, and also for terrestrial devices owing to the emission of radionuclides from device packaging material.

Much work has been carried out using unfocused high-energy heavy ion beams from very large accelerators, pulsed lasers and pulsed electron beams as the source of ionizing radiation to study upset mechanisms, but the lack of spatially resolved information hampered the interpretation of which part of the device causes the upsets for many years. The technique of SEU (single event upset) imaging, developed by the Sandia microprobe group [16, 19, 20, 31, 32] for the analysis of static random access memory (SRAM) chips and other devices, uses a heavy focused ion beam from a nuclear microprobe, such as 24 MeV Si^{6+} ions, scanning over the device surface. The information stored within the device is sampled at each beam position within the scanned area so that an image can be constructed showing the upset probability at each location. An IBIC image of the same area can be generated using the same heavy ion beam, or a lower-energy light ion beam, to enable the ion impact locations which give rise to upsets within this scanned area to be directly identified by comparing the SEU and IBIC images with the device layout. Other work on DRAM devices [35] was also able to locate those areas most susceptible to memory corruption using SEU images.

Other Uses of IBIC Microscopy

Work related to the production and interpretation of IBIC images from integrated circuits has been reviewed. However, work is in progress by several groups to extend the use of IBIC microscopy across a wider range of materials and different types of applications. Other work using IBIC microscopy includes the study in Melbourne of segmented pad detectors which are designed for high energy physics experiments into measuring spatially resolved distributions of sub-atomic particles. The charge collection efficiency of the individual segmented pads, and in the gaps between the segments, was studied using IBIC images with different bias voltages on the individual pads [1].

Other work includes characterising chemical vapour deposition (CVD) grown diamond films using IBIC microscopy by several Italian groups [26], and also recently in Melbourne (personal communication). The microprobe group at Waseda University have developed a variation of IBIC in which the beam dose at each pixel within a scanned area is accurately controlled using a beam deflector located at the object aperture [24], in order to deliver a known ion dose into specific regions.

Groups at Sandia and Melbourne are developing systems capable of time resolving the IBIC pulses in order to separate the components due to large diffusion and drift. It is envisaged that this will also improve the effective spatial resolution in IBIC images since it will enable the effects of lateral charge diffusion to be distinguished. IBIC has also been used as a means of imaging the halo of scattered particles around the focused beam spot produced within the nuclear microprobe chamber [6] in order to understand the origin and effects of the beam halo.

A further application of IBIC is the validation of charge transport computer codes used in device simulation. Design phase testing of circuits is becoming of greater importance as fabrication complexity and expense increases. IBIC provides a unique means of validating computer simulation with controlled experiment, which is not possible with unfocused ion beams.

Conclusions

The ability of the recently developed IBIC microscopy technique to image the distribution of active pn junctions which are buried under thick surface layers within a range of different working integrated circuit structures has been shown. The strengths and weaknesses of this new technique have been compared with other forms of beam induced current microscopy. Its strengths are high resolution analysis of buried layers, which means there is no need to remove any surface layers, good quantitative interpretation of the measured charge pulses, no charging and no beam heating effects. Its weak points are a low signal to noise level resulting from measuring individual charge pulses and ion induced damage which must be carefully monitored.

IBIC can be optimised to give the maximum topographical contrast and insensitivity to ion induced damage for a given device structure. Long range MeV ions result in little topographical contrast, and since a large fraction of the charge carriers and ion induced defects are created in the substrate, the charge pulse height is rapidly affected by ion induced damage. Shorter range MeV ions, which are stopped within the depletion region, result in strong topographical contrast, and since most of the charge carriers and ion induced defects are created in the depletion layer, the charge pulses are only slowly affected by ion induced damage.

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Discussion with Reviewers

A.B. Campbell: You mention the disadvantage of the technique because of radiation damage, but are not quantitative. What is the typical particle fluence necessary for one image? Is there enough damage from this confluence to be seen in a subsequent image?
Author: Ion induced damage is usually detectable in IBIC images at doses of 10 to 1000 ions/μm^2. Consider a typical case of a beam flux of 3000 ions per second and a data collection period of 5 minutes. This represents a total dose of approximately 10^6 ions per image. For the 300 μm x 300 μm IBIC images in Figure 4, for example, this represents a dose of approximately 10 ions/μm^2 in each image, so damage effects were barely detectable. In comparison, Figure 11 was produced using a dose of several thousand ions/μm^2 and damage caused very noticeable effects on the resultant charge pulse height spectrum. This required special data collection procedures as described in ref. [15].

A.B. Campbell: What is the dependence of the images on pin voltages? Do higher voltages imply sharper images?
Author: Altering the pin voltages may not necessarily produce sharper images. However, by opening or closer certain junctions with different pin voltages, the IBIC image contrast does change, as shown in Figure 4.

Reviewer IV: Where does the future lead with this technique?
Author: I believe IBIC has a role to play in failure analysis and characterisation of multilayered integrated circuits because of its unique capabilities. Together with single event upset imaging, it provides a powerful tool for characterising which device areas are most subject to ionizing radiation and more microprobe groups are starting work in this area. Any aspect of charge collection microscopy which is hampered by charging effects, thick surface layers or metallisation layers would be worth while overcoming using IBIC microscopy.

Editor: What does the beam current unit "fA" stand for?
Author: This stands for femtoamp, which is a current of approximately 6,000 single charged ions per second.