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RELIABILITY ANALYSIS OF FOIL SUBSTRATE BASED INTEGRATION OF SILICON CHIPS

Nagarajan Palavesam

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Vorsitzender: Prof. Dr. rer. nat. Stefan Mannsfeld
1. Gutachter: Prof. Dr.-Ing. Dr. h.c. mult. Karlheinz Bock
2. Gutachter: Prof. emerit Dr. Ing. multi DHC. Paul Svasta
Prüfer: Prof. Dr. rer. nat. Johann W. Bartha

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Declaration

I hereby declare that except where specific reference is made to the work of submitted in whole or in part for consideration for any other degree or others, the contents of this dissertation are original and have not been qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text.

Nagarajan Palavesam
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Abstract

Flexible electronics has attracted significant attention in the recent past due to the booming wearables market in addition to the ever-increasing interest for faster, thinner and foldable mobile phones. Ultra-thin bare silicon ICs fabricated by thinning down standard ICs to thickness below 50 µm are flexible and therefore they can be integrated on or in polymer foils to create flexible hybrid electronic (FHE) components that could be used to replace rigid standard surface mount device (SMD) components. The fabricated FHE components referred as chip foil packages (CFPs) in this work are ideal candidates for FHE system integration owing to their ability to deliver high performance at low power consumption while being mechanically flexible. However, very limited information is available in the literature regarding the reliability of CFPs under static and dynamic bending. The lack of such vital information is a major obstacle impeding their commercialization.

With the aim of addressing this issue, this thesis investigates the static and dynamic bending reliability of CFPs. In this scope, the static bending reliability of CFPs has been investigated in this thesis using flexural bending tests by measuring their fracture strength. Then, Finite Element Method (FEM) simulations have been implemented to calculate the fracture stress of ultra-thin flexible silicon chips where analytical formulas may not be applied. After calculating the fracture stress from FEM simulations, the enhancement in robustness of ultra-thin chips (UTCs) against external load has also been proved and quantified with further experimental investigations. Besides, FEM simulations have also been used to analyse the effect of Young's Modulus of embedding materials on the robustness of the embedded UTCs. Furthermore, embedding the UTCs in polymer layers has also been experimentally proven to be an effective solution to reduce the influence of thinning and dicing induced damages on the robustness of the embedded UTCs.

Traditional interconnection techniques such as wire bonding may not be implemented to interconnect ultra-thin silicon ICs owing to the high mechanical forces involved in the processes that would crack the chips. Therefore, two novel interconnection methods namely (i) *flip-chip bonding with Anisotropic Conductive Adhesive (ACA)* and (ii) *face-up direct metal interconnection* have been implemented in this thesis to interconnect ultra-thin silicon ICs to

the corresponding interposer patterns on foil substrates. The CFP samples thus fabricated were then used for the dynamic bending reliability investigations.

A custom-built test equipment was developed to facilitate the dynamic bending reliability investigations of CFPs. Experimental investigations revealed that the failure of CFPs under dynamic bending was caused mainly by the cracking of the redistribution layer (RDL) interconnecting the chip and the foil. Furthermore, it has also been shown that the CFPs are more vulnerable to repeated compressive bending than to repeated tensile bending. Then, the influence of dimensional factors such as the thickness of the chip as well as the RDL on the dynamic bending reliability of CFPs have also been studied. Upon identifying the plausible cause behind the cracking of the RDL leading to the failure of the CFPs, two methods to improve the dynamic bending reliability of the RDL have been suggested and demonstrated with experimental investigations.

The experimental investigations presented in this thesis adds some essential information to the state-of-the-art concerning the static and the dynamic bending reliability of UTCs integrated in polymer foils that are not yet available in the literature and aids to establish in-depth knowledge of mechanical reliability of the components required for manufacturing future FHE systems. The strategies devised to enhance the robustness of UTCs and CFPs could serve as guidelines for fabricating reliable FHE components and systems.

Table of contents

List of figures

List of tables

List of Acronyms

ACA Anisotropic Conductive Adhesive

AE Acoustic Emission

AFM Atomic Force Microscopy

BOR Ball-on-Ring test

CFP Chip Foil Package

CMP Chemical Mechanical Polishing

DUT Device Under Test

eWLB embedded Wafer Level Ball Grid Array

FEM Finite Element Method

FHE Flexible Hybrid Electronics

FFOWLP Foldable Fan-Out Wafer Level Packaging

IC Integrated Circuit

IoT Internet of Things

LLT Line-Load Test

NCA Non Conductive Adhesive

PCB Printed Circuit Boards

PEN Polyethylene naphthalate

PET Polyethylene terephthalate

PI Polyimide

PSA Pressure Sensitive Adhesive

PTFE Polytetrafluoroethylene

RDL Redistribution Layer

R2R Roll-to-roll

SEM Scanning Electron Microscope

SMD Surface Mount Device

TTV Total Thickness Variation

UTC Ultra-Thin Chip

UTCP Ultra-Thin Chip Package

ZIF Zero Insertion Force

3PB 3-point-bending test

List of Symbols

$P_{\mathbf{f}}$ Failure Distribution

F Applied Load or Force

F_C Characteristic Fracture Load or Force

m Weibull Modulus

σ_{3PB} Fracture Strength

L Load span

b Breadth of the chip

t Thickness of the chip

p Position of the neutral plane

E Young's Modulus

r_b Bending radius

t_s Thickness of chip foil package

ΔR Increase in resistance

R_0 Initial resistance

Chapter 1

Introduction

1.1 Background and motivation for Flexible Electronics

The emerging Internet-of-Things (IoT) framework aims to connect almost every physical object via devices placed on them, thereby enabling seamless communication between the objects without requiring human interaction [1–3]. Market research studies forecast that there will be at least 20 billion IoT devices in 2020 [4–6] and high computing performance at low power consumption will be the vital requirement for several of these devices that are expected to sense, acquire and transmit the data from the objects to the internet. Therefore, sensors and actuators providing high performance at low power requirements and manufactured at low cost will be the key for successful implementation of IoT. Furthermore, a substantial fraction of these IoT devices will be placed on curved surfaces of buildings, industrial equipment and automobiles as well as at locations that will be subjected to repeated bending and folding during device usage such as human skin, prosthetics and textiles. Conventional rigid electronics based on Printed Circuit Board (PCB) might not fulfill the flexibility and conformability demands of such IoT applications. Therefore, flexible electronics has often been touted as the key enabler of IoT [7–11]. Besides, flexible electronics has also captivated considerable attention generated by the booming wearables market [12, 13] as well as the arrival of flexible [14] and foldable mobile phones [15].

The market for flexible electronics has been estimated to reach up to $24.78 billion in 2024 from $5.53 billion in 2017 [16]. Driven by such a huge market potential, research and development of flexible electronics has garnered remarkable attention in the recent years with the evolution of a variety of devices and systems for a myriad of applications such as flexible displays [17–21], health monitoring [22–25], electronic skin for robotics [26, 27] and prosthetics [28–30], implantable devices [31–33], smart textiles [34–36], smart packaging [37, 38], point-of-care diagnostics [39, 40] and IoT sensors [41–44] to name a few.

1.2 Substrates for fabricating Flexible Electronics

Flexible electronics is a generic term that can be applied to define any electronic device or system that is mechanically flexible. Though development of flexible electronics has been around for more than 50 years when the first flexible solar cell arrays were assembled on plastic substrates [45, 46], significant progress in the field has been demonstrated during the last decade due to the rapid advances in materials and processes that has resulted in the emergence of novel materials, processes and devices for flexible electronics [47–54].

Flexible electronics is still at its nascent stage of development and a variety of substrates such as paper [55–58], polymer foils [59–63], flexible glass [64–66] and thin metal foils [67–69] have been explored and demonstrated to fabricate flexible electronic devices and systems. However, polymer foils are the most commonly used substrates owing to several advantages exhibited by them over other substrates such as very good flexibility and foldability, high surface quality, excellent dielectric properties, lightweight, thin form factor and large area manufacturing feasibility [63, 70, 71]. Furthermore, when roll-to-roll (R2R) manufacturing processes are implemented, high throughput with fast and continuous production can be achieved at low costs [72, 73]. Some of the commonly used polymer foil substrates and their important properties are summarized in table 1.1. The given numbers are typical values and the actual material properties could differ between different manufacturers as well as individual products.

Table 1.1 Key properties of common polymer foil substrates [74]

Property	Polyimide (PI)	Polyethylene naphthalate (PEN)	Polyethylene terephthalate (PET)
Glass transition temperature (°C)	270	120	70
Water Absorption (%)	2-3	0.4	0.6
Coefficient of Thermal Expansion (ppm/°C)	8-20	20	33
Surface Roughness	Good	Poor	Poor

1.3 Types of polymer foil based Flexible Electronics

Based on the principal materials used for the fabrication process, polymer foil based flexible electronics can be generally classified into three types namely,

1. organic semiconductor devices using thiophenes, pentacenes etc. [75–80]
2. inorganic thin film semiconductor devices with amorphous and polycrystalline silicon, indium gallium zinc oxide etc. [81–88] and

3. Flexible Hybrid Electronics (FHE) by integrating

   (a) standard rigid Surface Mount Device (SMD) components [89–96] and

   (b) bare flexible ultra-thin chips (UTCs) [97–109]

1.4 Flexible Hybrid Electronics

1.4.1 Integration of SMD components on/in polymer foils

Among the four types of polymer foil based flexible electronics listed above, FHE integrated with SMD components can be fabricated at cheaper costs and is capable of delivering higher performance at lower power consumption compared to the first two types [110]. However, FHEs integrated with SMD components fall short of delivering the desired (and often required) full flexibility for several emerging applications owing to the rigid and bulky SMD components. Figure 1.1 presents FHE assemblies integrated with SMDs and UTC bent to a radius of 10 mm where the interconnection of some SMD components were damaged, thus leading to failure of the system whereas the FHE assembly with the integrated UTC remained intact and functional even when bent to a radius of 5 mm (Figure 1.2). Such lack of complete flexibility and conformability is a massive bottleneck towards realising truly flexible electronics for futuristic applications such as electronic skin for robotics and prosthetics, implantable electronics, IoT applications, flexible displays and smart packaging to name a few. Thus, the quest for realising totally flexible and conformable electronic systems capable of delivering high performance at low power consumption has opened the doors for FHE systems fabricated by integrating UTCs.

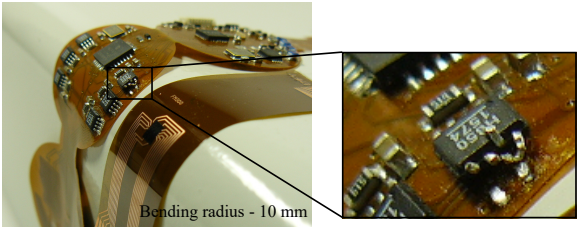

Fig. 1.1 FHE assemblies bent to a radius of 10 mm showing damaged SMD interconnection

Fig. 1.2 Conformability of Chip Foil Package. Originally published in [99]. ©2016 IEEE. Slightly modified and reused here with permission from IEEE.

1.4.2 Integration of bare ultra-thin chips on/in polymer foils - Chip Foil Packages

Since silicon becomes flexible at thicknesses below 50 µm, UTCs fabricated by thinning bare, rigid monocrystalline silicon Integrated Circuit (IC) chips can be used to replace SMD components in FHEs to improve the conformability and bending reliability. The resulting devices with improved flexibility and conformability obtained by integrating UTCs in polymer foils are referred to as ***Chip Foil Packages (CFPs)*** in this work. These CFPs thus fabricated are capable of providing industry standard high performance at low power consumption exhibited by the state-of-the-art devices since the UTCs are essentially the same ICs that are present inside the SMD components. Thus, by replacing standard SMD components with UTCs, the lack of conformability and complete flexibility encountered in FHE with rigid SMD components can be effectively addressed.

1.5 Bending reliability analysis of Chip Foil Packages

Several applications targeting flexible electronics demand the systems to remain functional when bent, often times requiring them to undergo multiple bending cycles while remaining functional. FHE is a relatively younger field and therefore only very limited information is available regarding the bending reliability of FHEs and CFPs [100, 111–114]. However, extensive information about the bending reliability of CFPs is absolutely indispensable for transferring the processes for manufacturing CFPs from research labs to industrial platforms and thereon for enabling the products to reach consumer markets. In order to be considered

as a potential component in future flexible electronic systems, the bending reliability of the CFPs need to be investigated in detail to establish guidelines for their fabrication and product usage. This work aims to address this objective by primarily investigating the reliability of the CFPs under static and dynamic bending.

1.6 Outline of the Thesis

This thesis is organised in three chapters.

In the following chapter 2, state-of-the-art static bending test methods for analysing the fracture stress of standalone thin chips is introduced. Then, the fracture strength or stress of silicon chips of varying thickness ranging from thin to ultra-thin regime have been calculated using analytical formula and Finite Element Method (FEM) simulations. Next, the enhancement in fracture force or robustness of UTCs against external load achieved by embedding of UTCs in polymer foils is elucidated with experimental investigations. Lastly, the influence of embedding on the damages on the chip surface and edges resulting from wafer thinning and dicing processes is discussed with experimental results. The investigations on the impact of embedding of UTCs on their robustness increase and the discussions on the influence of embedding on the damages induced on the UTCs arising from the wafer thinning as well as dicing processes have been performed for the first time to the extent of the author's knowledge.

Chapter 3 describes the two divergent interconnection approaches namely (i) *flip-chip bonding with Anisotropic Conductive Adhesive (ACA)* and (ii) *face-up direct metal interconnection* applied for fabricating CFPs in this work. The implementation of both processes to interconnect UTCs having daisy chain patterns have also been described in detail.

Chapter 4 begins with the description of the custom-built test equipment and the test protocol followed to study the dynamic bending reliability of the CFPs. Various investigations performed on the CFPs and the obtained test results are discussed in this chapter. Firstly, the effect of tensile as well as compressive bending stresses on the dynamic bending reliability of CFPs are compared and it has been experimentally found that the CFPs are more vulnerable to compressive stress than to tensile stress. Such an experimental analysis has been performed for the first time to the best of the author's knowledge. Then, the cause of failure of the CFPs during dynamic bending tests is identified and a hypothesis for the initiation as well as development of the failure under dynamic bending has been proposed which is in coherence with several other studies. Furthermore, the influence of dimensional factors such as the thickness of integrated chip and the interconnecting redistribution layer (RDL) on the dynamic bending reliability of the CFPs were also experimentally analysed for the first time

to the best of the author's knowledge. Finally, two methods to improve the dynamic bending reliability of CFPs have also been suggested and the resulting enhancement in the dynamic bending reliability of CFPs have been experimentally verified for the first time to the extent of the author's knowledge.

The final chapter 5 includes the concluding remarks and outlook for follow-up works. The key contributions and findings of this thesis are also listed in this chapter.

Chapter 2

Static bending reliability analysis of Chip Foil Packages

The key advantage of UTCs over commercially available SMD components is their mechanical flexibility and bendability. The extent to which UTCs can be bent without fracture can be determined from the fracture strength of the UTCs. Fracture strength is the maximum stress at which the UTC breaks or fractures due to the externally applied load and it is commonly expressed in Pascal (Pa). Fracture strength of samples is generally calculated from experimentally measured force values using analytical formulas that depend on the geometry and dimensions of the UTC. The maximum load or force at which the UTC fractures (called the fracture load or force) is measured by conducting flexural bending tests where the device under test (DUT), UTC in this case, is placed on a holder of a defined geometry and a known external load is applied to the DUT until it fractures.

Based on the type of stress applied on to the DUT, commonly used flexural bending tests can be classified into two groups: (1) uniaxial bending tests and (2) biaxial bending tests. Some of the widely used flexural bending tests for assessing the fracture strength of silicon chips are illustrated in figure 2.1. Flexural bending tests are generally conducted with a universal testing machine. The test results are sensitive to the loading and specimen geometries. Therefore, it is important to maintain the same dimensions for the samples and the test setup throughout the experiment series.

2.1 Description of test equipment and samples

As mentioned earlier, fracture strength of a DUT is determined from the experimentally measured fracture load or force obtained from flexural bending tests. The measured fracture

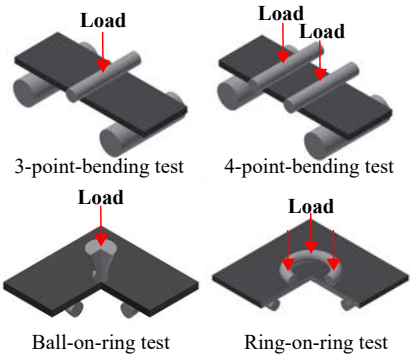

Fig. 2.1 Commonly used flexural bending tests

load or force is then used to calculate the fracture stress or strength by converting the measured force values to stress values using analytical formulas specific to the test and sample geometry. In this thesis, 3-point-bending (3PB) tests were conducted to measure the fracture force of UTCs having a thickness of 30 µm. The 3PB tests were performed with a universal testing machine, *Inspektmini* (Figure 2.2) from *Hegewald & Peschke GmbH* equipped with variable load cells. A 50 N load cell was used for measuring the force in this work. During the 3PB test, the UTC was placed on two supporting rods and a mechanical load was applied with a loading rod at a speed of 1 mm/min. Besides UTCs, the fracture strength of relatively thicker chips having thicknesses of 65 and 130 µm were also calculated in this work to understand the relationship between chip thickness and fracture strength. Figure 2.3 shows a bent UTC during a 3PB test. The loading rod used for applying the load had a radius of 1 mm and the loading span was 8 mm for chips with 30 and 65 µm thicknesses while a loading span of 10 mm was used for chips having a thickness of 130 µm. Rectangular samples having dimensions of 12 mm x 4 mm were used for the 3PB tests so that the stress along the breadth of the sample remains constant during load application, thus resulting in an equally loaded stress on the surface as well as along the edges of the sample. The same sample length and breadth was maintained for all chip thicknesses.

2.2 Fabrication of ultra-thin chips

UTCs can be manufactured using both additive and subtractive approaches. Additive methods involve processes to grow and release thin silicon layers after fabrication of the device whereas subtractive methods consist of thinning and dicing of the device silicon wafer down to the

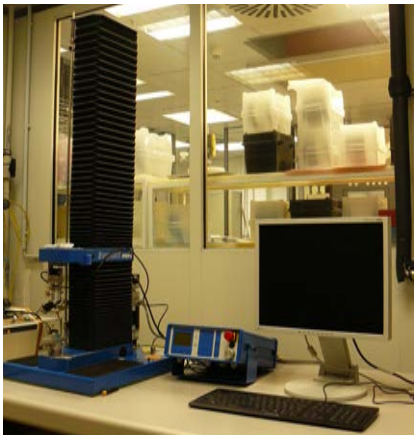

Fig. 2.2 Universal Testing Machine used for experiments

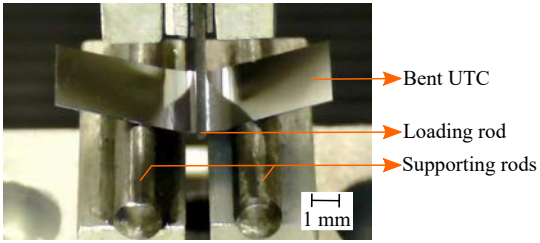

Fig. 2.3 A standalone UTC during a 3PB test [115]. Reused with permission from IMAPS.

desired thickness. Some of the renowned additive and subtractive techniques of fabricating UTCs are listed in table 2.1. In this work, UTCs were prepared using well-established *Dicing-by-Thinning* process that follows a subtractive approach consisting of two main steps: (a) wafer dicing and (b) wafer grinding. A schematic of the *Dicing-by-Thinning* process followed to prepare the thin and ultra-thin chips is portrayed in figure 2.4.

The process started with the selection of silicon prime wafers having thickness of $\approx$700 µm. Since no electrical functionality is required to measure the fracture strength of the chips, test samples were fabricated from blank silicon wafers without any metal patterns. However, it should be noted that the fracture strength of processed chips with structures is expected to be lower than that of blank chips without any structures [113, 125]. After selection of wafers, grooves were scribed on the front side of the sample wafers using

Table 2.1 Technologies for fabricating UTCs

Additive methods	Subtractive methods
Trench-protect-etch-release [116]	Dicing Before Grinding [117]
Controlled spalling technique [118]	Soft-etch-back [119]
Epitaxial layer transfer [120]	Dicing by Thinning [121]
Chip Film [122]	TAIKO Process [123]

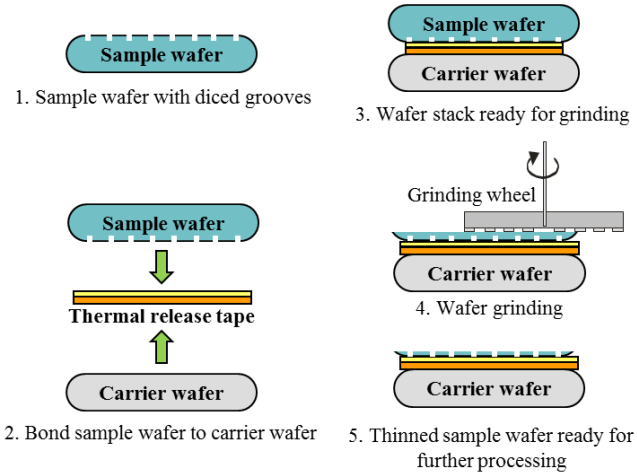

Fig. 2.4 *Dicing-by-Thinning* process for fabricating UTCs, Figure originally published in [124]. Slightly modified and reused here with permission from Springer Science and Bus Media B V.

Wafer Sawing for the predefined *l* x *b* dimensions in a sawing equipment having diamond equipped rotating cutting wheels. Precise dicing of the wafers is crucial since the depth of the grooves defines the final thickness of the chips. Then, the sample wafers were bonded to carrier wafers using a thermal release tape, *Revalpha*® from *Nitto Denko Corporation*, that is releasable at 90 °C. The carrier wafers provide rigid support for the sample wafers after thinning below 50 µm where silicon becomes flexible, thus ensuring secure handling and further processing of the sample wafers. Next, the sample wafers were thinned from the rear side with *Wafer grinding* where rotating diamond wheels grind and remove material physically. The wafer grinding process usually consists of a coarse and a fine grinding step. Coarse grinding step is performed with bigger diamonds for fast material removal while fine grinding is effected with smaller diamonds. Wafer grinding usually results in a rough

rear side having total thickness variation (*TTV*) in the range of ≈1-2 µm. Following the wafer grinding step, a *Wet chemical spin etching* process was performed as the stress-relief step where the damaged layers on the rear side of the sample wafer arising from the wafer grinding step were removed chemically. Wet-chemical spin etching normally results in a mirror-like finish on the rear side of the sample wafer and improves the fracture strength of the chips [126]. However, such complete removal of micro-defects from the surface as well as edges of the chips to achieve a mirror-like finish would require complex, long-lasting and expensive polishing processes. Therefore, some micro-cracks as well as notches would persist on the chips in most of the wafer thinning processes. Finally, the chips from the sample wafers were released from the carrier wafers on a hotplate at 100 °C. Further detailed information regarding the *Dicing-by-Thinning* process of fabricating UTCs can be found here [121].

2.3 Principle of 3-point-bending tests

As mentioned earlier, 3PB tests were conducted on thin and ultra-thin silicon chips to measure their fracture force in this work. During the 3PB tests, the applied load was measured continuously and a load-time curve was plotted (Figure 2.5). When the chip fractured due to the applied load at its fracture force, the applied load drops suddenly as indicated by the vertical drop of the load curve (Figure 2.5) and the fracture force of the chip was determined from the load value corresponding to the peak of the load-time curve.

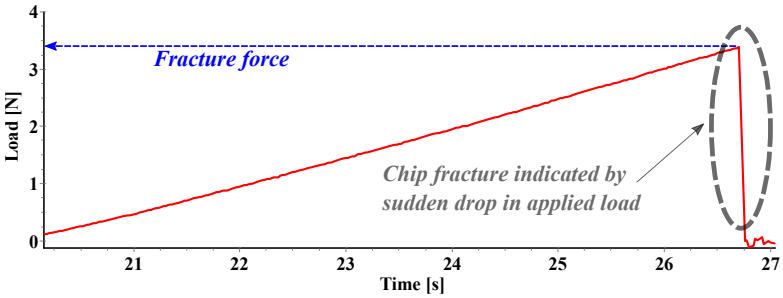

Fig. 2.5 Load-time curve plotted during a 3PB test. The load value corresponding to the peak of the red load-time curve denoted by the blue arrow line is the fracture force [115]. Reused with permission from IMAPS.

Table 2.2 Mean fracture force of chips measured using 3PB tests

Chip thickness	**Mean Fracture Force**	**Characteristic Fracture Force** *@63.2% Fracture Probability*
(µm)	(N)	(N)
30	0.0766	0.08
65	0.6149	0.626
130	2.2735	2.44

2.4 Fracture force measurement of thin and ultra-thin chips

3PB tests were performed on 30 test samples for each chip thickness and the results obtained from the tests are summarized in table 2.2. Generally, data obtained from the tests are plotted in various types of graphs such as histograms, box charts, scatter plots and Weibull plots for statistical analysis. Among these different types of graphs, Weibull plots provide information concerning failure analysis, failure probability and failure forecasts even for a small number of samples. The slope of a Weibull plot corresponds to the variation in results and hence a steeper Weibull plot indicates lower distribution of the results. The fit of any chosen data to a Weibull distribution can be evaluated with a Weibull plot. In case of a Weibull probability plot for fracture strength analysis, the x axis of the Weibull plot is the fracture force (F in N) or fracture stress (σ in Pa) and the y axis is the fracture probability. Figure 2.6 presents the Weibull probability plot of the measured fracture force of the chips with three different thicknesses. In figure 2.6, the straight line corresponding to a fracture probability of 63.2% denotes the force at which 63.2% of the samples would fail indicating the most likely load for chip fracture called *Characteristic Fracture Force or Load*. The Failure Distribution (P_{f}) is defined by the following formula:

$$P_{\mathrm{f}} = 1 - \exp(-\frac{F}{F_C})^m \tag{2.1}$$

where F is the applied load or the force, F_C is the characteristic fracture force or load and m is the value of variability or Weibull modulus.

2.5 Fracture stress calculation

When a comparative analysis is performed with different chip types and if the chip thickness remains the same across the different types, either fracture force or strength can be used to compare the strength of the different chips. But, when the chip thickness changes, thicker chips would sustain a higher applied load before fracture than thinner chips, thus exhibiting

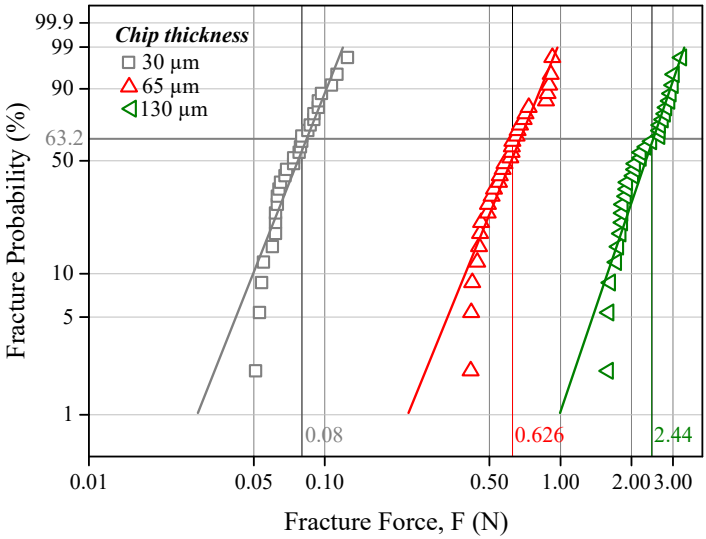

Fig. 2.6 Weibull probability plot comparing the fracture force of standalone chips having different thicknesses (30, 65 and 130 µm) during 3PB tests

higher fracture forces. In such a case, fracture force can no longer be used to compare the strength of the chips and fracture stress is required to evaluate the strength of the chips since fracture stress is a material property that does not change with variations in the sample dimensions. However, it should be noted that material properties such as Young's Modulus of experimental samples differ from ideal material properties due to various process induced changes in the samples. Therefore, a comparative analysis based on fracture stress would provide the real information regarding the strength of the chips when chips with different thicknesses are examined. Hence, the measured fracture force must be converted to fracture stress by eliminating the influence of the geometrical factors such as cross-sectional area since stress is defined as the force applied per unit area. The fracture stress of chips examined using 3PB tests can be calculated using equation 2.2 given below.

$$\sigma_{3PB} = \frac{3FL}{2bt^2} \tag{2.2}$$

where σ_{3PB} is the fracture stress in Pa, F is the fracture force in N, L is the load span or the distance between the supporting rods, b is the breadth of the chip and t is the thickness of the chip (Figure 2.7).

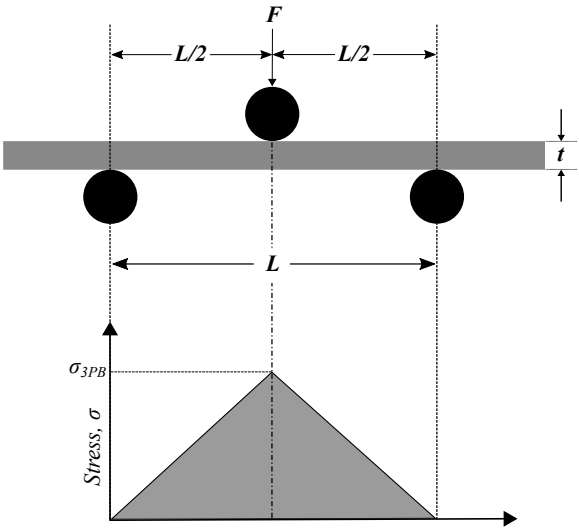

Fig. 2.7 Principle of 3-point-bending test [115]. Reused with permission from IMAPS.

2.6 Calculation of fracture stress of UTCs

The equation 2.2 can be used to calculate fracture stress from measured fracture force only when a linear force-displacement relationship exists for the samples. In case of flexible UTCs, the force-displacement relationship becomes non-linear at higher displacements due to slipping of the chips from the supporting rods of the sample holder causing the chips to undergo higher displacements before fracture [127]. Therefore, equation 2.2 may not be used to calculate the fracture strength of the UTCs. In such cases, Finite Element Method (FEM) simulations can be used to calculate the fracture stress of the UTCs. Such FEM simulations were performed in this work to calculate the fracture stress from the measured fracture force values. As mentioned earlier, the material properties of experimental samples are different from ideal material properties due to various process induced changes in the samples. For the sake of simplicity, ideal material properties of Silicon <110> (Young's Modulus = 168.9 GPa and Poisson's ratio = 0.361 [128]) were used for the simulations performed in this work. Due to sample and test setup symmetry, only a quarter symmetrical model was used for the simulations and the simulations were performed with displacement control. Figure 2.8 presents the quarter symmetrical model used for the FEM simulations.

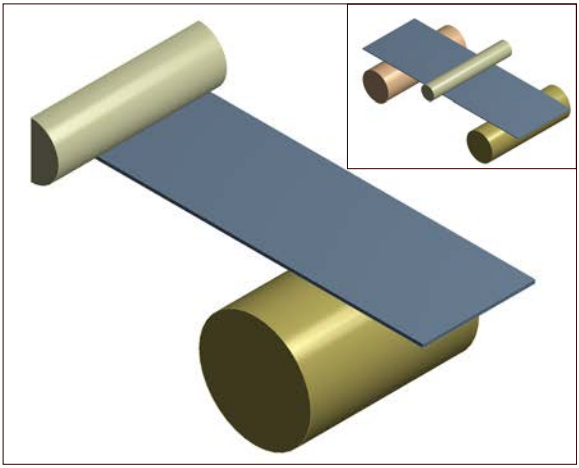

Fig. 2.8 Quarter symmetrical FEM model used for calculating fracture stress of UTCs. Inset: Full symmetrical model [115]. Reused with permission from IMAPS.

Table 2.3 Mean fracture stress of standalone chips calculated using analytical formula and FEM simulations

Chip Thickness	**Mean Fracture Force**	**Mean Fracture Stress**		**Characteristic Fracture Stress** *@63.2% Fracture Probability*	
		Analytical	FEM	Analytical	FEM
(µm)	(N)	(MPa)	(MPa)	(MPa)	(MPa)
30	0.077	-	249	-	260
65	0.615	437	420	425	445
130	2.274	505	517	542	554

The stress values obtained from the FEM simulations are plotted alongside analytically calculated values (using equation 2.2) in a Weibull plot in figure 2.9. The mean stress values calculated from FEM simulations and analytical calculations that are summarized in table 2.3 indicate very good correlation with each other, thus validating the FEM simulations. Table 2.3 also reveals that the fracture stress of the chips decrease with a corresponding decrease in the chip thickness which complies with an earlier published work [129]. However, other studies have shown that the fracture stress of thinner chips can be increased by implementing advanced dicing and thinning processes [130, 131], thus indicating that wafer thinning as well as dicing processes followed in this work could be improved to achieve higher fracture stress

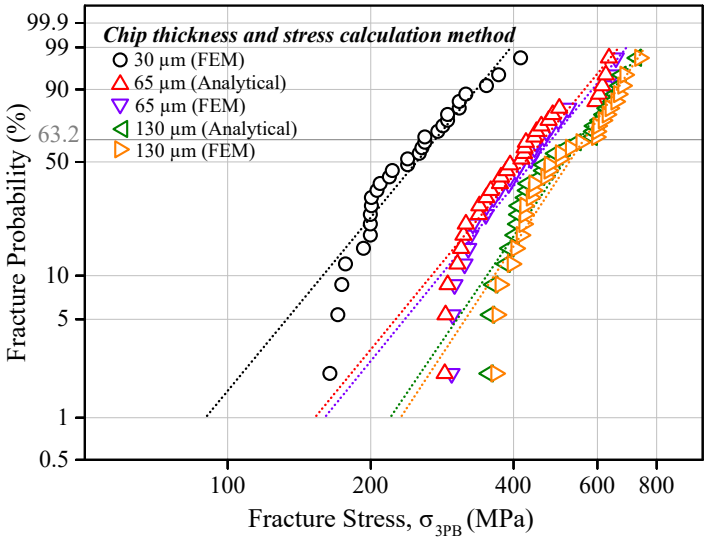

Fig. 2.9 Weibull probability plot comparing the fracture stress values of standalone chips having different thicknesses (30, 65 and 130 µm) calculated using FEM simulations and analytical formula for 3PB tests. Figure originally published in [115]. Slightly modified and reused here with permission from IMAPS.

for thinner chips. Therefore, it becomes evident that the fracture stress of thinner chips could be enhanced by following advanced dicing and thinning processes such as plasma etching or longer stress relief processes to singulate the chips where almost all of the micro-cracks as well as notches could be eliminated resulting in defect-free edges and chip surface [132, 133]. However, plasma etching is rather expensive compared to wafer sawing due to the additional requirement of a mask to define the etching streets and it becomes cheaper only when huge number of wafers are processed [134]. Similarly, a longer stress relief process would also increase the cost due to the decrease in throughput. Therefore, a cheaper solution to enhance the fracture strength of the UTCs is required.

2.7 Enhancement of robustness of UTCs

As mentioned earlier, fracture stress is a material property that depends on the thinning as well as the dicing processes and UTCs would fracture when they reach their fracture stress. Therefore, fracture stress of chips can not be enhanced without improvising the thinning and

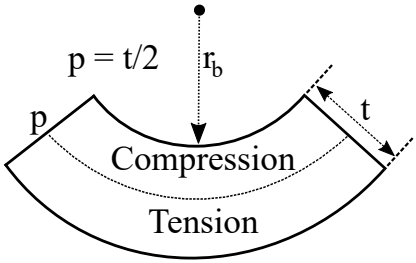

Fig. 2.10 Position of neutral plane (p) in an isotropic standalone chip

dicing processes. However, by embedding the chips in a stack of polymer layers, the applied load can plausibly be distributed across the sample surface, thus reducing and preventing the sample from stress peaks. Such a load distribution across the sample would result in enhancement of the robustness of the UTCs against externally applied loads without altering the thinning and dicing processes. The position of the embedded chip with respect to the neutral plane of the CFP stack determines the stress experienced by the UTC. Neutral plane is the plane of zero stress where compressive and tensile stresses cancel each other during bending (Figure 2.10). Since silicon is piezoresistive, the electrical performance of silicon ICs change when they are stressed due to both in-built stresses resulting from IC processing [135] and externally applied stress [136, 137]. Sometimes better electrical performance can be derived from the ICs when they are stressed [138, 139]. Yet, it is complicated to include the bending effects of ICs in most state-of-the-art simulation tools to predict the electrical performance. Therefore, it is simpler and advantageous to have the same electrical performance for the ICs in both flat and bent state.

When a standalone chip is bent to a radius (r_b), the neutral plane lies at its mid-plane. Likewise, the neutral plane of a symmetrical stack lies at its mid-plane during bending. However, when the stack is unsymmetrical, the position of neutral plane is controlled by the thickness and the Young's Modulus of the embedding layers.

A schematic of the bent symmetrical CFP stacks analysed in this work is depicted in figure 2.11. The stacks were prepared by mounting ICs on commercially available Polyimide (*PI*) foil substrates, *UPILEX 50S*™ from *UBE Industries* having a thickness of 50 µm. The chips were attached to the PI foil substrates with a ≈5 µm thin layer of a Pressure Sensitive Adhesive (*PSA*) coated on top of the PI foil substrates. A manually operated flip-chip bonder, *FINEPLACER*® from *Finetech Gmbh & Co. KG* was used to bond the chips. Then, similar PI foil substrates coated with ≈5 µm thin PSA were laminated on top of the chips to fabricate *Chip Foil Packages (CFPs)* with symmetrical layers so that the neutral plane

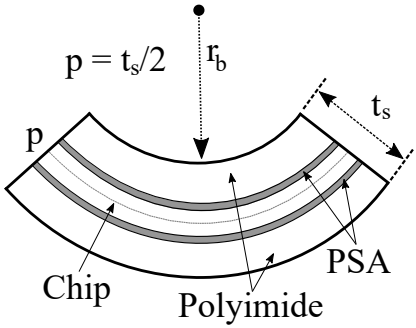

Fig. 2.11 Schematic of the cross-section of a bent symmetrical CFP showing the position of the neutral plane (p)

of the CFPs remained at their mid-plane during bending. 3PB tests were then performed on the fabricated CFPs using the same test geometries and conditions followed for the 3PB tests for standalone chips. The mean fracture force obtained from the tests were then used to analyse the enhancement of robustness of the UTCs by comparing the mean fracture force of embedded and standalone UTCs. Since fracture stress of the chip remains the same whether or not it is embedded, the chips would fracture when subjected to the same stress irrespective of embedding.

Figure 2.12 summarizes the fracture force (F_{max}) measured for standalone chips and chips embedded in polymer layers (CFPs) for the three different chip thicknesses. It can be noticed in figure 2.12 that the fracture force is higher for the CFPs than for the standalone chips of corresponding thickness. This increase in fracture force indicates that a higher force is required to impose the same stress on the chips when they are embedded in polymer layers. The increase in fracture force of CFPs results from the increase in stiffness effected by the overall thickness increase arising from the additional polymer layers. Therefore, fracture of both standalone and embedded chips with the same chip thickness would occur at the same fracture stress irrespective of embedding. However, a higher force (F_2) is required to induce the fracture stress in an embedded chip compared to a standalone chip (F_1) having the same chip thickness as evident from the experimental results (Figure 2.13).

A summary of the mean fracture force values measured from 30 samples is presented in figure 2.14. It can be noticed from the graphs that the normalised difference between the mean fracture force of embedded and standalone chips increases as the chips become thinner. The normalised difference between the mean fracture force of embedded and standalone chips was 353,%, 65% and 11% for chip thickness of 30, 65 and 130 µm respectively. Thus,

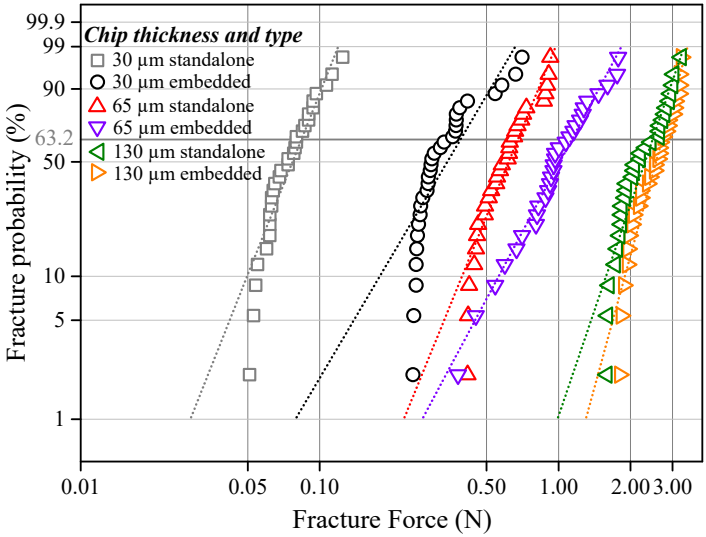

Fig. 2.12 Weibull probability plot comparing the fracture force of standalone and embedded chips having different thicknesses (30, 65 and 130 µm) during 3PB tests. Figure originally published in [115]. Slightly modified and reused here with permission from IMAPS.

it can be understood that the influence of embedding of chips on their fracture force/strength increases with a decrease in chip thickness. Since stiffness increases with an increase in thickness and Young's Modulus, a higher force is required to bend the chips embedded in PI substrates compared to standalone UTCs. Therefore, the robustness of chips against external load (i.e. fracture force or load) can be drastically enhanced either by increasing the thickness of the embedding polymer substrates or by replacing the polymer substrates by materials with higher Young's Modulus like metal foils.

2.8 Effect of Young's Modulus of embedding material on the robustness of embedded UTCs

The influence of Young's Modulus of the embedding material on the stress experienced by the chip during bending was analysed in this work with FEM simulations where the stress experienced by the embedded chip was compared for a CFP with top and bottom layer of the CFP made of Stainless Steel 316 and PI foil having the same thickness of 50 µm. The

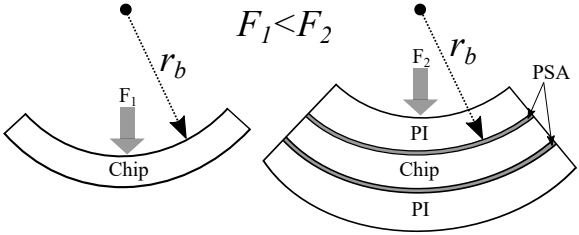

Fig. 2.13 Bent UTCs: Standalone and embedded in PI substrates at the same bending radius

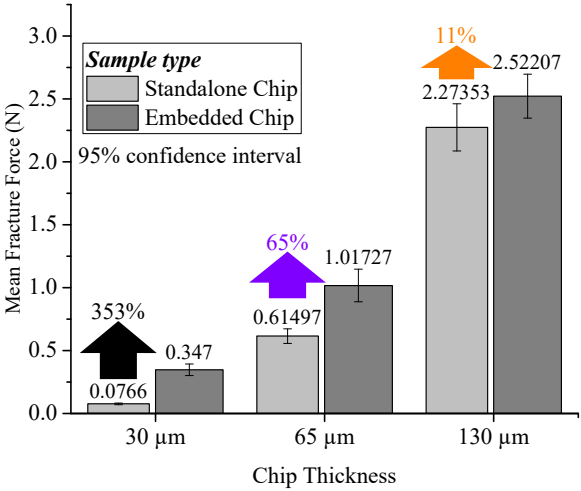

Fig. 2.14 Mean fracture force of standalone and embedded chips during 3PB tests. The arrows and the numbers above the arrows represent the increase in fracture force of the chips due to embedding. The numbers elucidate that a higher load distribution was achieved for CFPs with thinner chips with the same embedding foil thickness. Figure originally published in [115]. Slightly modified and reused here with permission from IMAPS.

Table 2.4 Fracture force of standalone and embedded chips measured using 3PB tests

Chip Thickness	**Type**	**Mean Fracture Force**	**Characteristic Fracture Force** *@63.2% Fracture Probability*
(µm)		(N)	(N)
30	Standalone	0.077	0.08
	Embedded	0.347	0.332
65	Standalone	0.615	0.626
	Embedded	1.017	1.075
130	Standalone	2.274	2.44
	Embedded	2.522	2.74

Table 2.5 Material properties used for FEM simulations [128, 140, 141]

Material	**Young's Modulus** (GPa)	**Poisson's ratio**
Silicon <110>	168.9	0.361
UPILEX 50S	9.3	0.35
Stainless Steel 316	194.6	0.294

PSA layers bonding the chip with the foils were not included in the simulation model for simplifying the simulations. The material properties used for the FEM simulations are listed in table 2.5. Table 2.6 compares the fracture force as well as fracture displacement calculated using FEM simulations for a fracture stress of 249 MPa (determined from 3PB tests and corresponding FEM simulations) when PI and Stainless Steel 316 are used as the embedding layers. It can be noticed that the embedded chip in a CFP with Stainless Steel 316 foils would fracture at a lower displacement than the embedded chip in a CFP with PI foils. However, a much higher load (≈16x more) would be required by the UTC to reach its fracture stress of 249 MPa i.e.) the fracture force of an UTC embedded in Stainless Steel 316 foils would increase by (≈16x more) with a corresponding decrease in fracture displacement (≈4.4%) than an UTC embedded in PI foils. In other words, UTCs can be bent up to ≈4.4% more if a compliant substrate such as PI foil is used as the embedding layer instead of a stiffer substrate like Stainless Steel. Therefore, stiffer materials such as Stainless Steel 316 can be used as the embedding material where a higher durability against externally applied load at smaller bending radii is required and softer materials like PI foils can be used for applications targeting higher bendability. Thus, embedding of chips with appropriate material could prove as a faster and cost effective alternative to increase the robustness of chips against externally applied load rather than performing expensive polishing and stress relief processes.

Table 2.6 Fracture force and displacement for embedded UTCs with different embedding materials (calculated with FEM simulations for a fracture stress of 249 MPa)

Embedding Material	**Fracture Force** (N)	**Fracture Displacement** (µm)
Polyimide	0.36	309
Stainless Steel 316	5.74	296

2.9 Minimising the impact of chip micro-defects on the robustness of UTCs

2.9.1 Acoustic Emission assisted fracture force detection of chip foil packages

As mentioned earlier, the fracture force of UTCs can be improved if plasma etching is implemented instead of wafer sawing to singulate the chips. However, the higher costs effected for less number of samples hamper the usage of plasma etching for several applications. Nevertheless, the fracture force of chips singulated using plasma etching were investigated in this work to have a comparative analysis with the fracture force of chips diced using wafer sawing. Furthermore, both chip types were also embedded in polymer layers to evaluate the influence of embedding polymers on their fracture force and thereof on the micro-defects arising from chip dicing was analysed. The UTCs measured 3.2 mm x 2.4 mm with a thickness of 20 µm and the only difference between the UTCs was the dicing method. Owing to the smaller dimensions of the chips, Line-Load Test (*LLT*) [142] was implemented instead of 3PB tests to measure the fracture force of UTCs where the samples were placed on an elastomeric polymer platform and mechanical load was applied with a loading rod. A 7 mm thick Silicone supporting platform was picked off the shelf and the test samples were laid on top of the platform during the tests as the load was applied to the samples with the same loading rod used for 3PB tests. The measurement of fracture force of standalone UTCs was simpler and straight forward as the fracture of the samples was detectable by the force sensor of the universal testing machine. However, in case of CFPs, the fracture of the embedded UTCs was undetectable by the force sensor. Therefore, an Acoustic Emission (AE) sensor was added to the setup to accurately detect the fracture event and to precisely determine the fracture force by correlating the peak amplitude short burst AE signal of the AE sensor with the corresponding load value on the load-time curve (Figure 2.15). A schematic and the photo of the AE assisted LLT test setup used in this work are presented in figure 2.16.

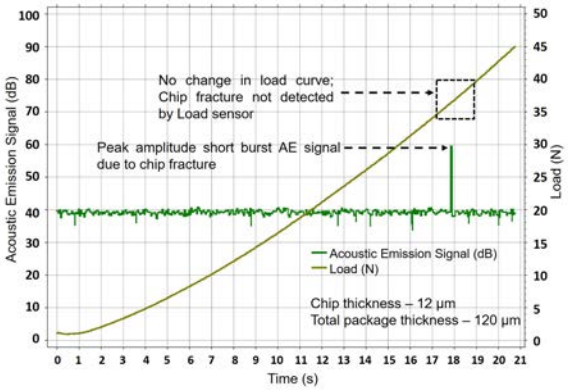

Fig. 2.15 Accurate determination of fracture force of embedded UTCs during LLT by correlating load and AE curves. Figure originally published in [143]. Reused here with permission from Mesago Messe Frankfurt GmbH.

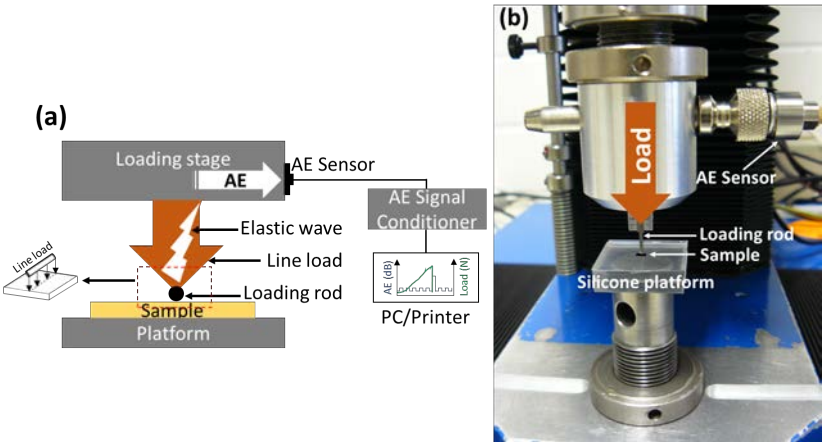

Fig. 2.16 (a) Schematic and (b) photo of the AE assisted LLT test setup implemented in this work. Figure originally published in [143]. Reused here with permission from Mesago Messe Frankfurt GmbH.

2.9.2 Principle of Acoustic Emission sensors

AE sensors have long been used as quality assurance and failure identification tool in Civil Engineering, Geology, Material Science, industrial process monitoring and machine condition analysis to name a few [144–147]. Acoustic Emission is the phenomenon in which acoustic waves are generated due to the redistribution of the materials resulting from the irreversible changes in their internal structure. Internal changes such as plastic deformation, crack formation and propagation, erosion and corrosion, and impact produce transient elastic waves due to sudden release of elastic energy. The transient elastic wave arising from the internal structural change propagates in the material until it reaches the material surface where it creates a surface motion by interacting with the material surface. When AE sensors are attached to the surface of the material, the surface motion can be captured by the sensors which then convert the captured surface motion into an electric signal. The converted electrical signal can be then processed and used to identify the exact moment of failure occurrence. If the surface area of the material to be tested is too small, sensors can be mounted to an adjacent body that is in physical contact with the sample. Two types of failures, namely failures occurring once (burst AE) or repeatedly (continuous AE) can be identified and monitored using AE sensors. In short, AE sensors are much more sensitive to material damages than force sensors and hence they enable accurate detection of a fracture event. In this work, the exact fracture force of the samples were obtained by correlating the peak amplitude short burst AE signal with the corresponding load value on the load-time curve as elucidated in figure 2.15.

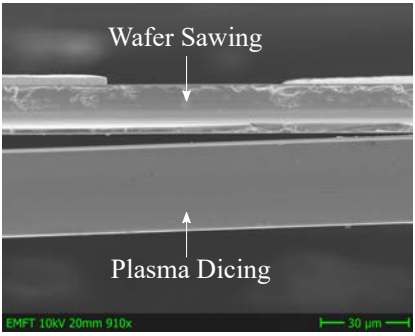

Fig. 2.17 Scanning Electron Microscope (SEM) image of sidewall of wafer sawn and plasma diced UTCs [99]. ©2016 IEEE. Reused here with permission from IEEE.

2.9.3 Effect of dicing induced micro-defects on the fracture force of UTCs

10 samples for each chip dicing type were tested and the measured fracture force values are plotted in a Weibull Plot (Figure 2.19). Since all the examined UTCs have the same thickness of 20 µm, strength of the UTCs can be analysed by comparing their fracture force. The mean fracture force of the UTCs measured from the experiments are included in table 2.7. A closer look at (Figure 2.19) and the table 2.7 exemplifies the influence of the dicing induced damages on the fracture strength of standalone UTCs. It can be noticed that the mean fracture force of standalone plasma diced chips are higher (7.79 N or ≈197% more) than that of standalone wafer sawn chips. The difference in fracture force between the two standalone UTC types is attributed to the presence of defects such as micro-cracks and notches on the edges as well as sidewalls of the UTCs. Since the chip edges of plasma diced chips are almost devoid of micro-defects, plasma diced UTCs tend to have a higher fracture strength compared to wafer sawn UTCs. The following subsection 2.9.4 elucidates the difference in the chip sidewall roughness of wafer sawn and plasma diced chips via Atomic Force Microscopy (AFM) analysis performed on the sidewall of the chips.

2.9.4 Sidewall roughness analysis of UTCs

Figure 2.17 exemplifies the difference in the sidewalls as well as the chip edges of wafer sawn (t=17 µm) and plasma diced (t=30 µm) UTCs. AFM analysis conducted on the sidewalls of the chips emphasized the difference in surface roughness of the sidewalls. The AFM image presented in figure 2.18 reveals the presence of peaks and craters created on the sidewalls due to chipping during wafer sawing whereas the sidewalls of plasma diced UTCs shows only scallops resulting from the plasma etch process, thus confirming that the sidewalls of plasma diced chips were completely free from any other extreme topographical structures (Figure 2.18). Furthermore, the root mean square (RMS) values of the sidewalls obtained from the AFM analysis also indicate that the sidewalls of plasma diced UTCs are ≈3 times smoother than wafer sawn UTCs (Figure 2.18).

2.9.5 Reducing the influence of surface damages of UTCs on their robustness

When the UTCs were embedded in symmetrical PI (t=50 µm) and PSA (t=5 µm) layers on either side of the UTCs similar to the samples discussed in section 2.7, the fracture force of both plasma diced and wafer sawn UTCs increased as expected. Figure 2.19 and figure 2.20

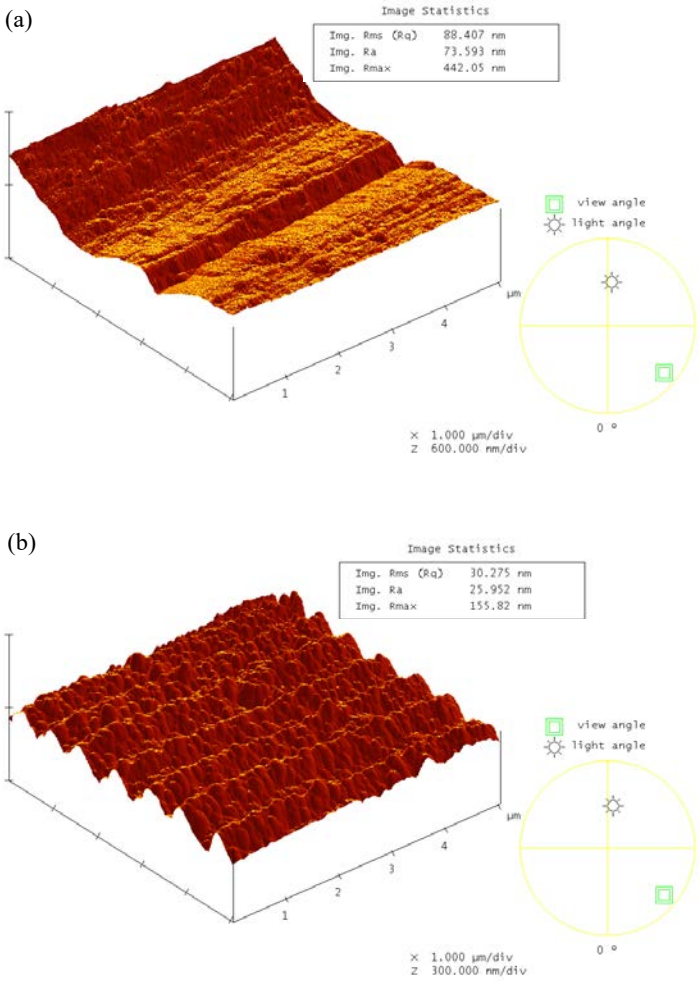

Fig. 2.18 Surface profile of the sidewalls of (a) wafer sawn and (b) plasma diced UTCs [99]. ©2016 IEEE. Reused with permission from IEEE.

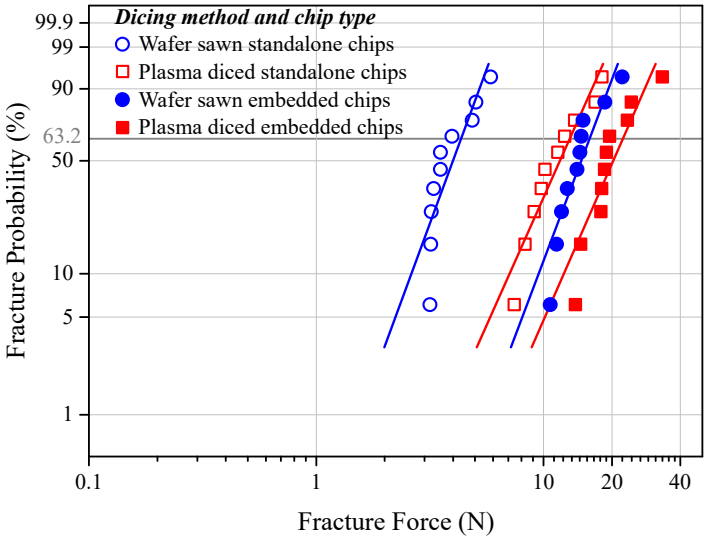

Fig. 2.19 Weibull probability plot comparing the fracture force of standalone and embedded UTCs measured with LLT for chips singulated using wafer sawing and plasma dicing

reveal the improvement in fracture force of both types of UTCs due to embedding. The mean fracture force of plasma diced and wafer sawn standalone UTCs were 11.75 N and 3.96 N respectively with a normalised difference of ≈197% between the two sample types. The mean fracture force of plasma diced and wafer sawn UTCs when embedded were 20.26 N and 14.59 N respectively with ≈39% normalised difference between the two samples types revealing a decrease in the normalised difference in fracture force between the sample types when embedded. The increase in fracture force of plasma diced and wafer sawn UTCs due to embedding were 72% and 268% respectively. Therefore, it becomes evident that wafer sawn UTCs benefited more from embedding than plasma diced UTCs and the difference in mean fracture force of the two UTC types after embedding dropped to ≈39% from ≈197% in case of standalone UTCs. The decrease in the difference in fracture force of plasma diced and wafer sawn UTCs after embedding confirmed that the impact of dicing induced micro-cracks on the fracture force of the UTCs can be significantly reduced by embedding the UTCs. The reduced difference in the fracture force of the UTCs after embedding was caused plausibly due to the embedding polymer acting as a load buffer that distributes the load across the chip surface, thus protecting the chip surface with micro-cracks from stress peaks. Hence, considering the reduced difference in the fracture force (≈39%) of the UTCs

Table 2.7 Fracture force of plasma diced vs. wafer sawn UTCs

Chip singulation method	**Type**	**Mean Fracture Force** (N)	**Characteristic Fracture Force** *@63.2% Fracture Probability* (N)
Wafer sawn	Standalone	3.96	3.96
	Embedded	14.59	14.68
Plasma diced	Standalone	11.75	12.42
	Embedded	20.26	19.55

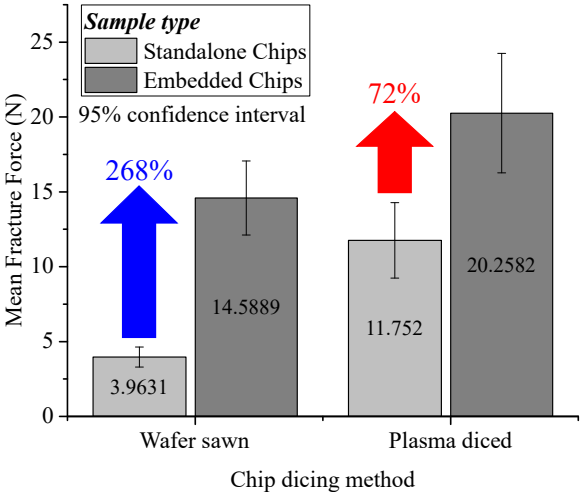

Fig. 2.20 Mean fracture force of standalone and embedded UTCs measured with LLT: Wafer sawing vs. Plasma dicing. The arrows and the numbers above the arrows represent the increase in fracture force of the chips due to embedding.

after embedding, it can be plausibly concluded that embedding in PI foils is a cost-effective solution to enhance the robustness of the UTCs against external loads for smaller production volumes rather than implementing expensive dicing techniques like plasma dicing. Besides, the embedding PI foil and PSA could also help to protect the surface scratches (arising from the wafer grinding process) from stress peaks thereby improving the fracture strength of the chips when embedded in polymer layers. This was verified experimentally in the ensuing subsection 2.9.6.

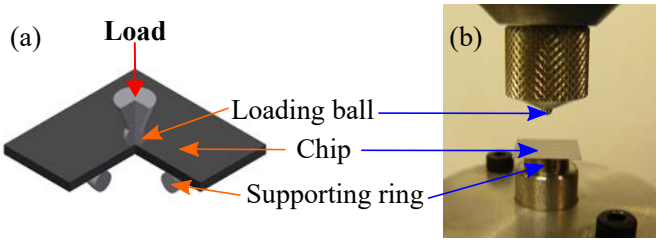

Fig. 2.21 (a) Schematic (3/4 view) and (b) photo of the Ball-on-ring test

2.9.6 Improvement in biaxial fracture force of UTCs due to embedding

Similar to dicing induced micro-defects, surface damages occurring on the chips due to the thinning processes also affect their fracture force. In order to analyse the influence of surface damages of the chips on their fracture force, a larger surface of the chips need to be stressed. Therefore, biaxial flexural bending tests are best suited to analyse the effect of surface defects on their fracture strength. Surface defects are inflicted on chips primarily due to wafer thinning steps such as grinding, etching and Chemical Mechanical Polishing (CMP). In this thesis, the fracture force of thin and ultra-thin chips were measured by conducting ball-on-ring (BOR) tests where the chips were placed on a ring and stressed with a ball. Similar to the 3PB tests, chips having three different thicknesses, 30, 65 and 130 µm, were used for the BOR tests. Square shaped chips with a larger surface area measuring 10 mm x 10 mm were used for the BOR tests. Figure 2.21 presents the schematic of the BOR test and a standalone chip during a test. The radius of the ball was 0.5 mm and the internal radius of the ring was 4.5 mm. Due to the expected higher forces, a 1 kN force sensor was used for the BOR tests. The speed of load application was 1 mm/min.

Figure 2.22 shows that the fracture force of the chips increase when the chips are embedded in polymer layers indicating that the embedding PI foil and PSA concealed the

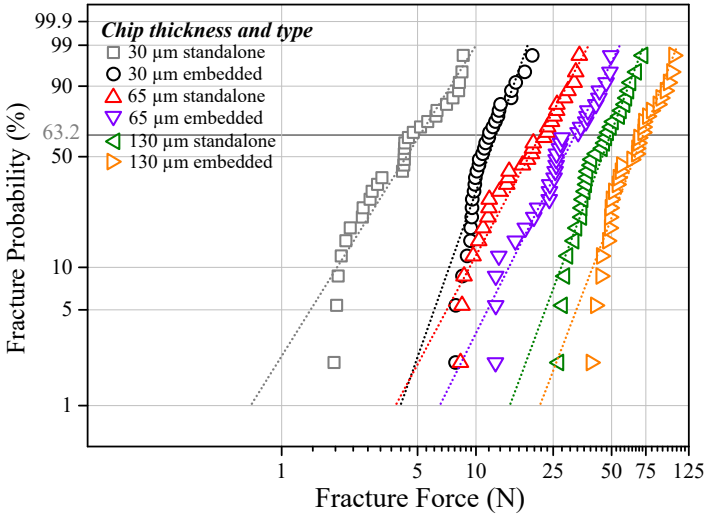

Fig. 2.22 Weibull probability plot comparing the fracture force of standalone and embedded chips with three different thicknesses (30, 65 and 130 µm) during BOR tests

surface damages of the chips enabling the chips to withstand a higher applied load. Alike 3PB tests, the influence of embedding on the mean fracture force increased as the chips became thinner (Figure 2.23). Therefore, it has been experimentally confirmed that embedding of chips reduces the impact of surface damages on the chips and the influence of embedding of chips on their fracture force increases as the chips become thinner. Thus, it can be concluded that embedding of chips is much more crucial for UTCs.

Table 2.8 Fracture force of standalone and embedded chips measured using BOR tests

Chip Thickness	**Type**	**Mean Fracture Force**	**Characteristic Fracture Force** *@63.2% Fracture Probability*
(µm)		(N)	(N)
30	Standalone	4.536	4.77
	Embedded	11.547	11.77
65	Standalone	19.079	23.38
	Embedded	28.759	27.85
130	Standalone	44.501	48.3
	Embedded	65.583	72.4

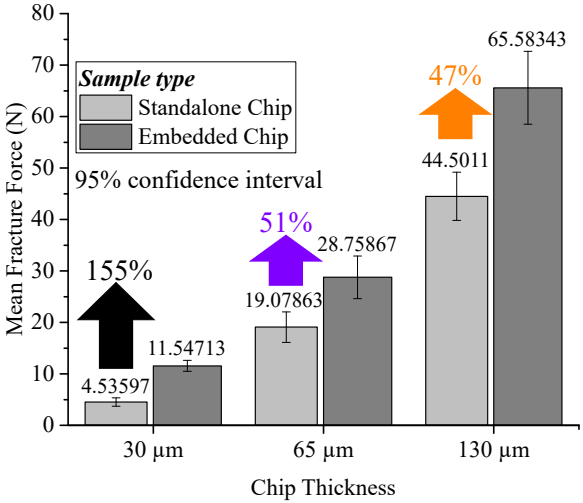

Fig. 2.23 Mean fracture force of standalone and embedded chips during BOR tests. The arrows and the numbers above the arrows represent the increase in fracture force of the chips due to embedding.

2.10 Summary

The static bending reliability of silicon chips can be analysed from the fracture stress calculated using the corresponding fracture force values measured using flexural bending tests. In this thesis, uniaxial 3-point-bending (3PB) tests were conducted on thin and ultra-thin silicon chips to measure the fracture force and the fracture force values were then used to calculate their fracture stress. However, standard analytical formula defined by the 3PB test for calculating fracture stress is not valid for UTCs due to the non-linear force-displacement relationship they exhibit at higher displacements. Therefore, the fracture stress of UTCs were calculated in this work by performing FEM simulations using the measured fracture force values. The fracture stress calculated from the FEM simulations were in good agreement with the fracture stress calculated using the formulas defined by the standard test method for chips with thickness of 65 and 130 µm where the formulas are valid.

Experimental results obtained from 3PB tests on standalone chips revealed that the fracture stress of the chips reduced as the chips became thinner, thus indicating the need to improve the edge and surface quality of the chips by following advanced dicing as well as thinning processes such as plasma etching or longer stress relief processes to singulate the

chips where almost all of the micro-cracks as well as notches could be eliminated resulting in defect-free edges and chip surface. However, implementing such advanced and longer processes would result in a significant cost increase. Therefore, a cheaper solution to enhance the fracture strength of the UTCs is required. Embedding the chips in polymer layers is a cost effective solution to increase the strength of the chips. Experiments conducted in this work proved that the robustness of chips against external loads can be improved by embedding the chips in polymer layers. Furthermore, the impact of Young's Modulus of the embedding layers of the CFPs on the robustness of the UTCs against external load was analysed by performing FEM simulations and it was shown that the fracture force of the UTCs can be enhanced by embedding chips in stiffer materials such as metal foils. However, an increase in stiffness would hamper the bendability of the CFPs. Therefore, the material and the thickness of each of the constituting embedding layers must be meticulously chosen for the CFPs ad-hoc to the target application. Softer, compliant materials such as PI foils are recommended as embedding layers for CFPs when bendability is preferred over durability against external load for applications such as mounting of sensors on curved surfaces. Thus, a faster and cost effective alternative to increase the robustness of chips against externally applied load rather than performing expensive polishing as well as stress relief processes could be achieved by selecting appropriate embedding materials by foreseeing the expected load type/range for the particular application scenario.

Acoustic Emission assisted Line-Load Tests conducted on UTCs proved that the effect of edge defects arising from chip dicing can be remarkably reduced by embedding the UTCs. Furthermore, Ball-on-Ring tests performed on standalone and embedded chips indicated that embedding of chips reduces the impact of surface defects of the chips arising from chip thinning process on their fracture force. Hence, embedding of chips can be recommended as a cost-effective solution to improve the overall robustness of chips with surface and edge defects resulting from wafer thinning as well as dicing processes especially for UTCs.

Chapter 3

Fabrication of Chip Foil Packages: Interconnection of bare ultra-thin chips

In order to investigate the dynamic bending reliability of the CFPs, electrically interconnected samples similar to real IC packages are required so that the reliability of several components such as the integrated chip, interconnecting RDL and the chip-RDL interface can be examined. However, as mentioned in chapter 1, bare UTCs are fragile in terms of mechanical strength. Therefore, commonly used interconnection techniques such as wire-bonding cannot be employed to interconnect UTCs as the process involves high mechanical forces that will fracture the UTCs [148–151]. Hence, two other processes namely, (i) **Flip-Chip bonding with Anisotropic Conductive Adhesive (ACA)** and (ii) **Face-up direct metal interconnection** were implemented in this work to integrate and electrically interconnect the UTCs with the RDL on the polymer foils. This chapter includes detailed description of these two interconnection processes. In principle, both these interconnection techniques consist of two basic steps, (a) fabricating the RDL on polymer foils and (b) integration and interconnection of the UTC with the RDL. However, the basic difference between the two methods lies in the sequence of the two interconnection steps.

3.1 Flip-Chip bonding of UTCs with ACA

Flip-chip bonding of UTCs with ACA follows an ***"RDL first, chip last"*** approach where the RDL layer is first fabricated on the substrate onto which the UTCs are bonded next. Flip-chip bonding has been used to interconnect ICs on PCBs since the 1960s [152, 153]. However, standard flip-chip bonding process may not be used for bonding UTCs owing to the higher, localised stress on the UTCs exerted by the bumps during the integration process as

well as during usage of the IC [113, 154] and hence it has been seldom used to interconnect UTCs. Alternatively, the conventional flip-chip bonding process could be slightly modified to interconnect UTCs by using ***"Anisotropic Conductive Adhesive (ACA)"*** which results in several benefits over traditional soldering such as improved mechanical flexibility, simpler processing at relatively lower temperatures, reliable fine pitch interconnection capability without bridging adjacent bumps, lead-free (hence environmental friendly) and fluxless formulation [155, 156]. Owing to these advantages, flip-chip bonding with ACA was implemented to interconnect UTCs several years ago [109]. Studies reported by Klink et al. also highlights the need to optimise the process to avoid failures such as chip cracking due to high bonding forces [109]. Since then, plenty of research has been performed in the field and the ever-increasing demand for UTCs with finer I/O pitches has led to the inevitable emergence of several innovative methods to fabricate the RDL on polymer foil substrates [157–161].

3.1.1 Semi-additive patterning of RDL on polymer foils

As mentioned earlier, flip-chip bonding of UTCs with ACA starts with the fabrication of the RDL patterns on polymer foil susbtrates. In this work, the RDL patterns were fabricated by following the semi-additive patterning technique reported by Drost et al. [161]. The semi-additive process follows the footprint of classical microfabrication approach involving sputter deposition, lithography and electroplating. Commercially available *UPILEX S* Polyimide (PI) foils with a thickness of 50 µm were used as the substrates. Thin metal layers on foil substrates can be manufactured using sputter deposition of metallic ions. Before depositing the thin metal layer on the foil, an inline plasma pre-treatment step was performed to clean, activate and modify the foil surface to enhance adhesion of the metal to the foil. After the plasma pre-treatment of the foil, a chromium layer with a thickness of few nm was sputter deposited on the foil substrate. Then, a 500 nm thin layer of copper was sputter deposited on top of the chromium layer. It should be noted that a second separate etching step is required to remove the chromium adhesion layer since etch removal of copper and chromium cannot be performed concurrently using the same etchant. Following the sputter deposition of 500 nm copper, a negative tone dry film photoresist (*MX5015*™) from DuPont was laminated directly onto the PI foil substrate with a lamination system from Stork GmbH. The resolution of the fabricated metal structures is mainly determined by the thickness and the stability of the resist as well as the overlying *Mylar*® coversheet during various processing steps. Hence, the resist and the overlay materials must be carefully selected to ensure a reliable fabrication process. The PI foils laminated with the resist on top of the sputter deposited copper were then transferred to an OptoLine 2200 system from Ciposa S.A. to define the fine metallic

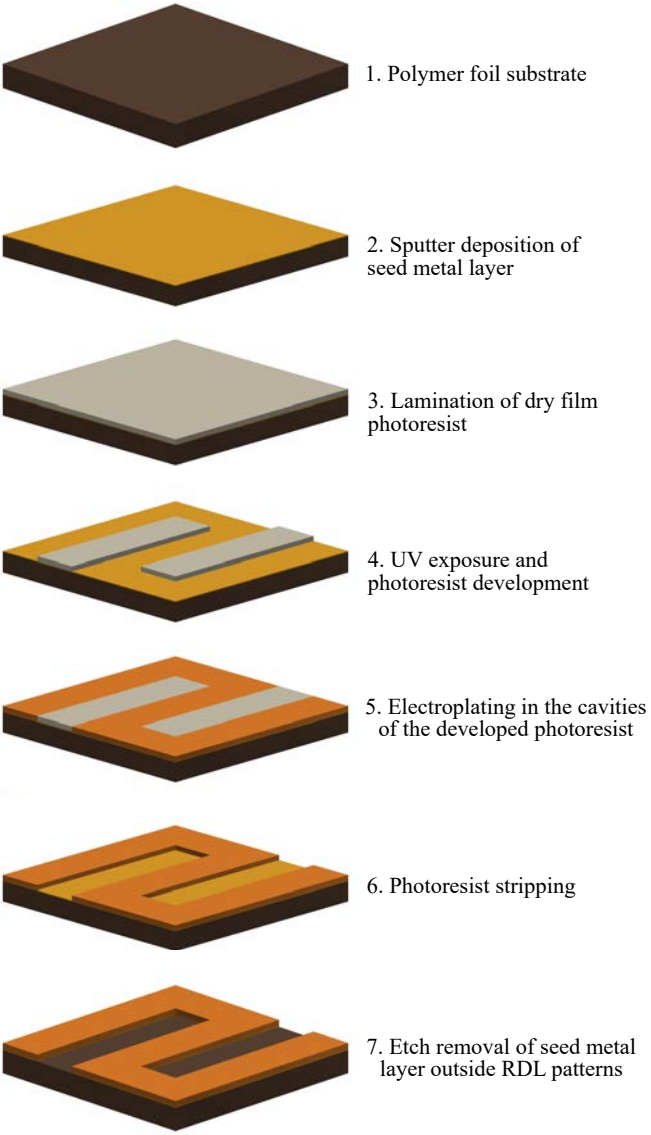

Fig. 3.1 Schematic of the RDL fabrication process

structures of the RDL. Then, photolithography was performed with a collimated mercury (broadband) light source at an intensity of about $20\,mW/cm^2$ using chromium coated 9 inch glass masks. Next, the exposed resist was developed at 28 °C using 0.5% soda solution (Na_2CO_3) as the developer.

After completion of the resist development step, the RDL patterns were thickened to few µm by implementing an electroplating process where the thickness of the electroplated metal layer was defined by the resist thickness. Though electroplating is a well-established technology for growing thicker metal layers on rigid substrates like PCBs, it's usage and application in polymer foils has been rather minimal. Electroplating is primarily applied on polymer foils for selective deposition and patterning of RDL in a resist layer involving photolithography and resist development. The key requirement for electroplating process is the presence of a seed metal layer over which thicker metal patterns can be grown. Hence, a thin film metal deposition step such as sputter deposition or Physical Vapour Deposition is usually performed prior to electroplating for depositing the seed metal layer on the polymer foils. The presence of surface contaminants such as polymer residues affect and reduce the adhesion of the photoresist to the seed metal layer. Therefore, a cleaning step was performed prior to lamination of the photoresist to enhance the adhesion of the photoresist to the seed metal layer. A continuously operating Direct Current electroplating system was used for depositing the thicker copper layers over the seed metal layer. The electroplating process was performed in a R2R electroplating equipment from Sessler GmbH with an acid copper bath as the medium.

Figure 3.1 illustrates the R2R process sequence implemented for fabricating the RDL. In this work, copper RDL with thickness up to 10 µm were patterned using electroplating. After deposition of thicker RDL using electroplating, the resist was stripped off from the foil surface at 50 °C using a 10% potassium hydroxide solution (KOH). Then, the copper seed layer and the interfacial chromium adhesion layer were etched in two separate steps. The copper seed layer etching step was performed at 28 °C in a chemical bath consisting of 13% sodium persulphate ($Na_2S_2O_8$) that has an etch rate of about 0-5 µm/min. An in-built ultrasonic tool aided the exchange of the etch medium to the surface of the polymer foils by removing the bubbles that might adhere to the tiny resist gaps while the foil was moved in the etching bath.

Upon completion of copper seed layer etching, the chromium adhesion layer was removed in a separate step at an external bath with a highly diluted alkaline potassium ferricyanide solution ($K_3Fe(CN)_6$). Lastly, the polymer foil with the electroplated RDL patterns was rinsed in deionized water and dried using hot air flow. In principle, the target metal thickness for etching is determined by the retention time of the polymer foil in the bath and consequently

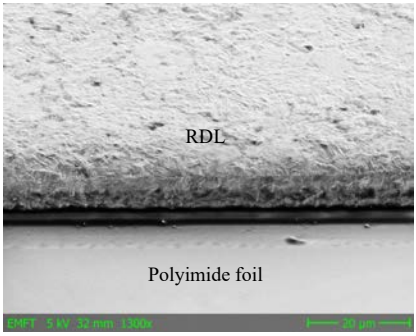

Fig. 3.2 SEM image of 10 µm thick electroplated RDL

the speed with which the polymer foil roll is moved in the bath during etching. Overall, wet etching is a relatively slow and time consuming process that plays the key role in determining the duration of the RDL fabrication process. Figure 3.2 presents an SEM image of the electroplated RDL pattern with a thickness of 10 µm fabricated in this work.

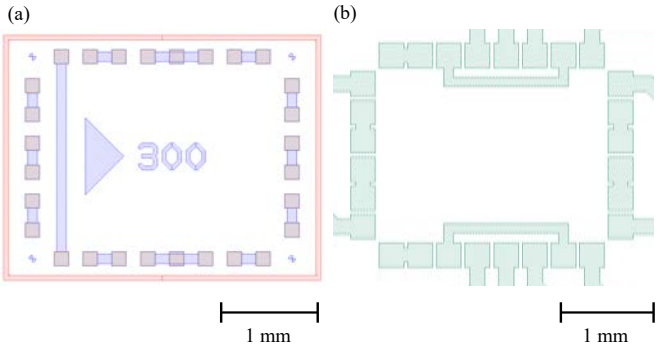

Fig. 3.3 Designed layout of (a) the chip and (b) its corresponding interposer RDL pattern

3.1.2 Integration and interconnection of UTCs on RDL

Flip-chip bonding with ACA was implemented in this work to mount bare UTCs (t<50 µm) on polymer foil substrates. Though flip-chip bonding of UTCs with ACA has already been demonstrated several years ago [109], few parameters such as (i) bonding force, (ii) bonding temperature and (iii) quantity of ACA dispensed must be regulated to achieve effective

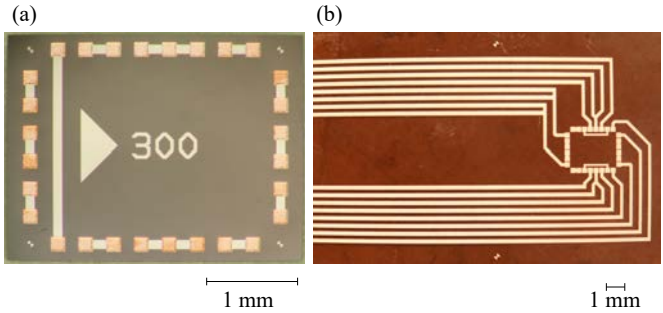

Fig. 3.4 Fabricated (a) chip and (b) its corresponding interposer RDL pattern on foil showing the layout [99]. ©2016 IEEE. Reused with permission from IEEE.

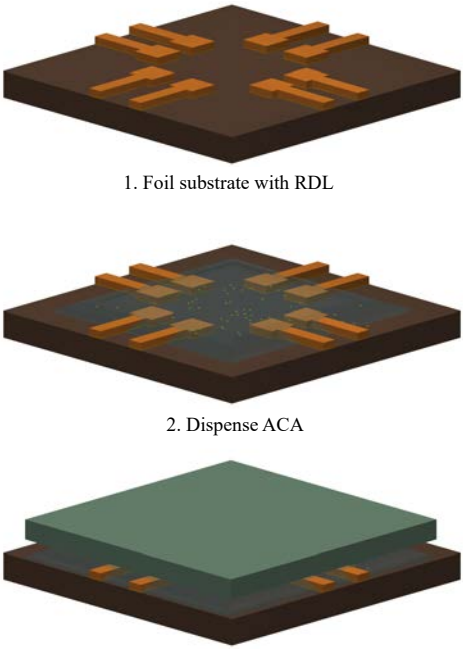

Fig. 3.5 Schematic of flip-chip bonding process of UTCs

interconnection without affecting the flexibility of the fabricated CFP. These aforementioned parameters need to be controlled to avoid fracture of UTCs, submersion of UTCs in ACA due to too much ACA and poor interconnection due to too less ACA. Several iterations were performed in this work to determine optimal parameters and to develop a reliable process to bond UTCs as thin as 20 µm having daisy chain test patterns on PI films[1]. The chip pads were prepared using standard microfabrication processes on prime silicon wafers having a thickness of 700 µm. After patterning of the chip pads, the wafers were thinned and singulated using processes explained in Chapter 2. Figures 3.3 and 3.4 show the designed and fabricated patterns on the UTCs as well as the corresponding interconnecting RDL patterns on the foil substrate respectively. The index 300 on the chip refers to the 300 µm pitch of the chip pad with 150 µm pad width and 150 µm pad spacing.

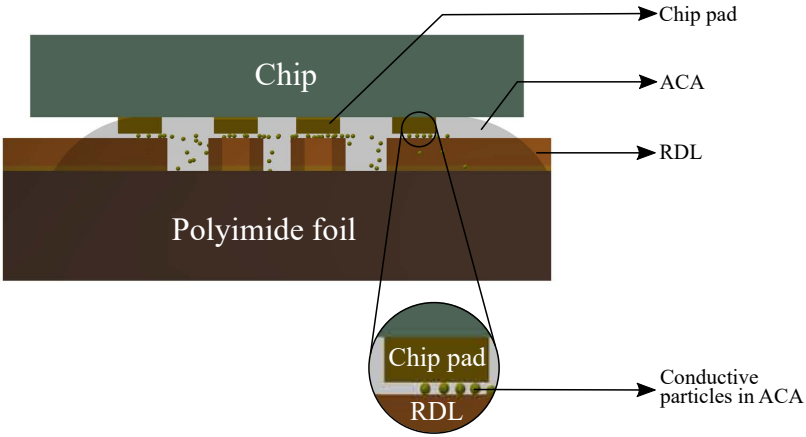

Fig. 3.6 Sketch of the cross-section of flip-chip bonded CFP

A schematic of the process sequence followed for mounting UTCs using flip-chip bonding is outlined in figure 3.5. At first, a commercially available ACA, Delo Monopox AC 245 was dispensed on to the electroplated RDL patterns on the polymer foils. ACA is a lead-free and environmentally friendly adhesive interconnect system consisting of conductive, usually metal particles suspended in an epoxy medium to realize electrical as well as mechanical connections between the IC and the substrate. The size and composition of the conductive particles vary between different products. The ACA used in this work consisted of a modified

[1]Detailed information about the daisy chain test patterns is included in Appendix A

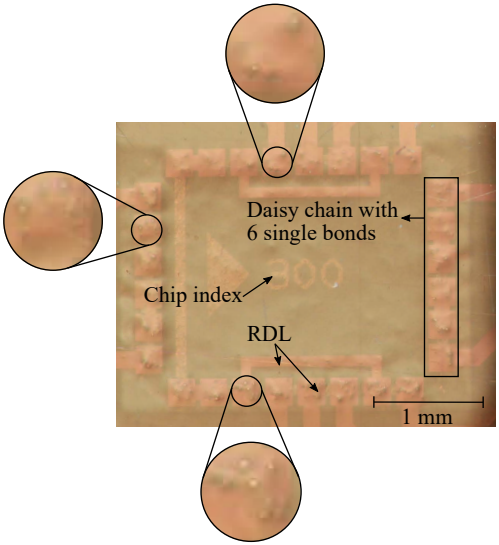

Fig. 3.7 Rear view of a flip-chip bonded CFP revealing the ACA interconnection between the chip and the foil RDL. Some of the protrusions on the RDL resulting from pressing the ACA conductive particles are shown within the circles.

epoxy resin filled with Nickel particles with a diameter of 5.3 µm. Then, the UTCs were bonded onto the foil substrates using a programmable die bonding equipment (Panasonic FCB 3) to realize the integration and interconnection of UTCs with the RDL thus fabricating CFPs. The chip bonding process was performed with a bonding force of 5 N and at a temperature of 200 °C. Due to the high temperature involved in the bonding process, the substrate material should be selected accordingly. UPILEX S foils used in this work are stable up to 300 °C. During the flip-chip bonding process, the UTCs were pressed against the substrate with the dispensed ACA and cured thermally. Electrical interconnection is established between the UTCs and the RDL through the conductive particles. The cured epoxy serves as an underfiller, thus augmenting the mechanical reliability of the assembly. Figure 3.6 illustrates the cross-section of a flip-chip bonded CFP. The major drawback of ACA is the complexity in predicting the electrical contact resistance arising from the uncertainty in the number of trapped ACA particles at each interconnection owing to the random uncontrolled distribution of conductive particles in the epoxy medium [156]. After completion of the chip bonding process, the CFPs were electrically characterized to measure the resistance of daisy chain test patterns of the CFPs for evaluating the process as well as to analyse the process yield.

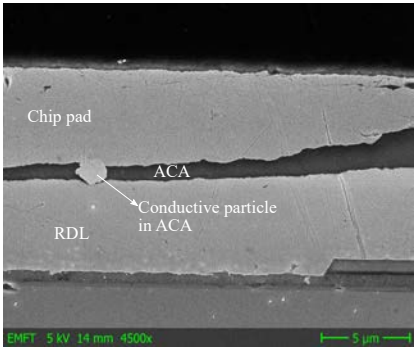

Fig. 3.8 SEM image of the cross-section of a single contact of a flip-chip bonded CFP [162]. Reused with permission from MDPI.

A view from the rear side of the flip-chip bonded CFP revealing the protrusions created on the RDL due to pressing of the conductive particles in ACA on to the RDL is presented in figure 3.7. The protrusions created due to pressing of the conductive particles in ACA on the foil RDL patterns are clearly visible at every interconnection and some of these are enlarged within the circles. Figure 3.8 presents an SEM image of the cross-section of the flip-chip bonded CFP showing the conductive particle that facilitates the electrical interconnection.

3.1.3 Optimisation of flip-chip bonding process

Apart from optimising the bonding force, the volume of ACA dispensed to bond the chips must also be refined to ensure a reliable bonding process. An insufficent ACA volume would inhibit good electrical interconnection due to reduced number of conductive particles whereas too much ACA would result in excess squeezed out ACA that would contaminate the chip bonding head of the equipment. Besides, removal of ACA from the bonding head is quite complicated since ACA is an epoxy and it is very difficult to remove once cured. Therefore, the parameters for the flip-chip bonding process must be optimised so that good electrical conductivity is ensured while keeping the bonding head clean. The images presented in figure 3.9 exemplify the difference in the volume of squeezed out ACA between an optimised and unoptimised process.

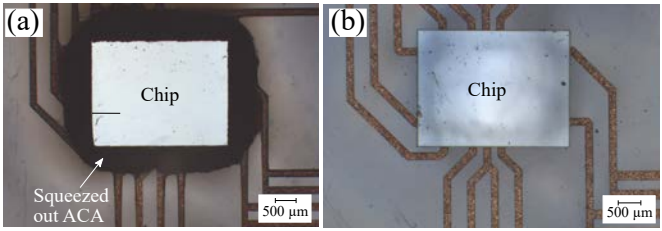

Fig. 3.9 Squeezed out ACA for (a) unoptimised and (b) optimised flip-chip bonding processes

3.1.4 Electrical characterisation

The flip-chip bonding process described here was implemented to bond more than 15 UTCs. The bonding process resulted in an excellent interconnection with a single bond interconnection resistance of <100 mΩ. A typical measurement of a single bond interconnection is presented in figure 3.10. The mean resistance of a daisy chain consisting of 6 single bonds of the CFP was measured to be 1.079 Ω with minimum and maximum values of 520 mΩ and 1.95 Ω respectively.

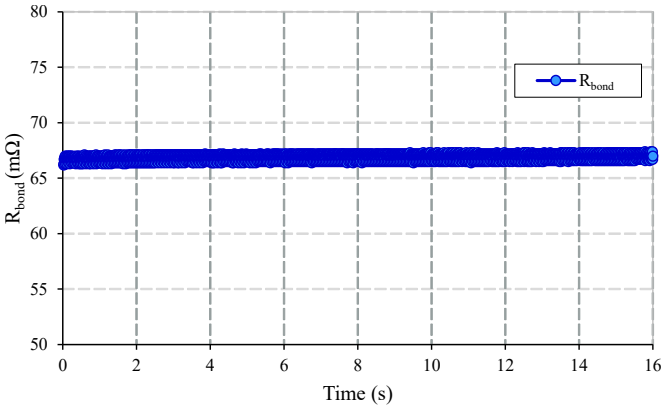

Fig. 3.10 Resistance of a single bond of the flip-chip bonded CFP [163]. ©2015 IEEE. Reused with permission from IEEE.

3.2 Face-up interconnection of ultra-thin chips

The ever-increasing interest for faster, thinner and smaller devices with growing I/O pad counts is driving the global IC packaging experts to develop novel interconnection technologies for flexible ultra-thin ICs with smaller I/O pad size/pitches while assuring efficient, low resistance interconnection at lower costs. This quest for fabricating thin IC packages with smaller I/O pad size/pitch ratio has resulted in several solutions such as embedded Wafer Level Ball Grid Array (eWLB) [164], Foldable Fan-Out Wafer Level Packaging (FFOWLP) [165], Ultra-Thin Chip Package (UTCP) [105] to name a few among several others [98, 103, 166–168]. Following the footprints of the global IC packaging community, a novel interconnection technology called ***Face-up direct metal interconnection*** that follows a ***"chip first, RDL last"*** approach has been developed in this work to fabricate CFPs with direct metal on metal low resistance interconnection.

Schematics of the process flow followed for face-up interconnection of the UTCs and the cross-section of an interconnected CFP are depicted in figure 3.11 and figure 3.12 respectively. The process was performed at wafer level on *UPILEX 50S* PI foils having a thickness of 50 µm attached to 200 mm silicon carrier wafers that enabled easy and secure processing.

The first step in the process was the bonding of ultra-thin silicon chips with a thickness of 20 µm having daisy chain test patterns on to *UPILEX 50S* polyimide foil substrates using a Non Conductive Adhesive (NCA) with the IC pads facing up. The chip bonding process was performed using a commercially available die bonding equipment, *Panasonic FCB 3*. Alignment marks scribed on the foil substrates using a laser prior to chip bonding to predefine the chip landing area facilitated accurate placement of the chips on the substrate. After the chips were accurately placed on the foil substrates, the embedding dielectric polymer layer was coated over the chips with a film applicator from Zehntner GmbH® that was thermally cured in an oven. Then, blind vias were drilled in the embedding polymer layer on to the chip pads using selective removal of the polymer by laser ablation. Figure 3.13 presents a microscopic top view of a blind via drilled by the laser. After completion of the via drilling process, residual embedding polymer was noticed on top of some of the chip pads during optical inspection as shown in figure 3.13. Therefore, a plasma etching step was performed to ensure complete removal of the embedding polymer from the chip pads without any residues. Besides, the plasma etching step also improves the adhesion of metal to be deposited on to the embedding polymer.

Upon complete removal of the embedding polymer from the chip pads, a thin layer of copper seed metal was sputter deposited on top of the embedding polymer layer and inside the laser blind via on to the chip pads. Next, interconnecting RDL patterns (t=5 µm) were fabricated by following a semi-additive metallisation process consisting of photolithography,

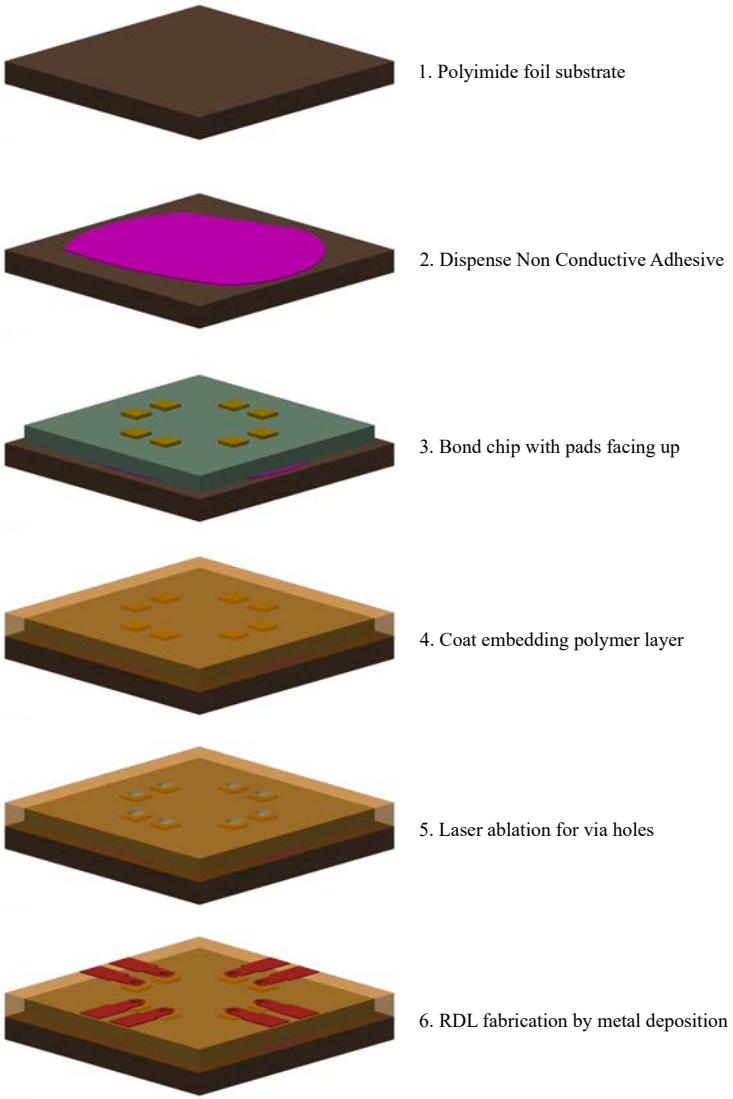

Fig. 3.11 Schematic of the face-up interconnection process for fabricating CFPs. Figure originally published in [115]. Slightly modified and reused here with permission from IMAPS.

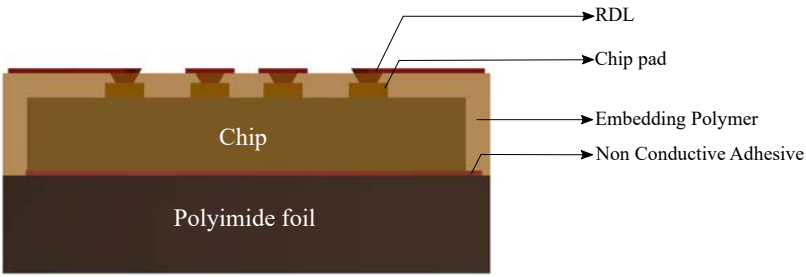

Fig. 3.12 Illustration of cross-section of the face-up interconnected CFP [115]. Reused with permission from IMAPS.

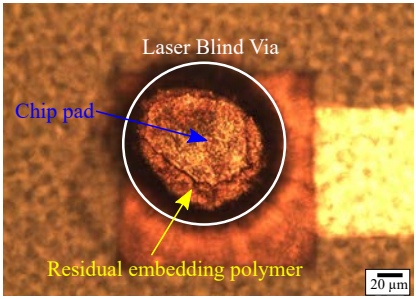

Fig. 3.13 Top view of a laser blind via [115]. Reused with permission from IMAPS.

electroplating and seed layer etch removal described in subsection 3.1.1. Figure 3.14 presents the fabricated chip foil packages on the carrier wafer after completion of the interconnection process. Then, a laser dicing step was performed to singulate individual chip foil packages using accurately defined boundaries and the singulated chip foil packages were finally released from the carrier wafer. Figure 3.15 shows an SEM image presenting the cross-section of a single interconnection between the chip pad and the RDL.

3.2.1 Electrical characterisation

The resistance of various structures in the CFPs were electrically characterized to calculate the process yield. Electrical characterisation of various structures such as daisy chains and single vias revealed that most of the structures were interconnected resulting in a very promising yield of 94%. The mean resistance of a single bond of the CFP was measured

to be 65.6 mΩ with minimum and maximum values of 55 mΩ and 75 mΩ respectively. The mean resistance of a daisy chain consisting of 6 single bonds of the CFP was measured to be 531.6 mΩ with minimum and maximum values of 505 mΩ and 561 mΩ respectively.

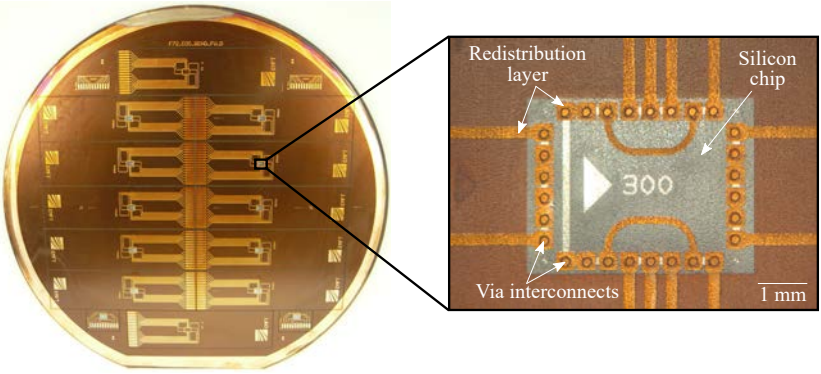

Fig. 3.14 Face-up interconnected CFPs prior to detachment from 6" handling wafer and a closer view of a CFP [115]. Reused with permission from IMAPS.

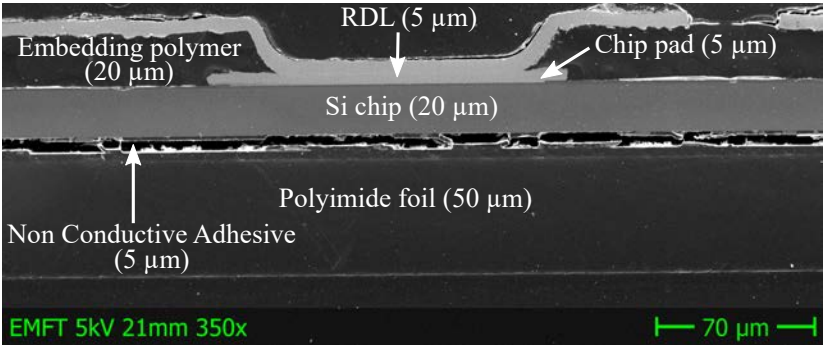

Fig. 3.15 SEM image of the cross-section of a single contact of face-up interconnected CFP [115]. Reused with permission from IMAPS.

3.3 Summary

Traditionally used wire bonding technique is not suitable for interconnecting UTCs owing to the high mechanical forces involved in the process that would fracture the UTCs. Therefore, two advanced interconnection techniques namely, (i) flip-chip bonding with Anisotropic Conductive Adhesive (ACA) and (ii) face-up direct metal interconnection were used in this work to integrate UTCs having daisy chain test patterns with pad pitch of 300 µm. Various process parameters were optimised for the flip-chip bonding with ACA and the face-up direct metal interconnection processes to establish reliable interconnection between the UTCs and the corresponding RDL patterns on the foils. The key advantage of these processes is their compatibility with R2R processing. Such R2R processing will enable low cost high volume industrial manufacturing of future flexible electronic components.

Chapter 4

Dynamic bending reliability analysis of Chip-Foil Packages

The dynamic bending reliability of CFPs is investigated in detail in this chapter. Dynamic bending reliability was analysed by conducting repeated bending tests on electrically interconnected CFPs fabricated using the processes described in chapter 3. The first part of this chapter is dedicated to the description of the custom-built test equipment and the test protocol followed to investigate the dynamic bending reliability. Then, section 4.3 discusses the dynamic bending reliability analysis of flip-chip bonded CFPs. Lastly, the dynamic bending reliability investigations of face-up interconnected CFPs is presented in section 4.7.

4.1 Test equipment

The dynamic bending reliability of the CFPs can be examined either by performing (a) offline measurements where the test samples are subjected to a specified number of bending cycles followed by measurement of the electrical characteristics at defined intervals or (b) online measurements in which the electrical characteristics are monitored in real-time during the bending cycles. Though both the approaches are practised extensively to study the dynamic bending reliability of electronic components, online monitoring of electrical characteristics of samples provides precise and in depth information regarding the behaviour of various components of the test samples during the bending cycles. Therefore, the bending tests performed in this work were conducted on a custom-built test setup equipped with online monitoring of daisy chain resistance of the CFPs.

In order to facilitate concurrent measurement of electrical characteristics of the CFPs during bending cycles, an ad-hoc test equipment was designed and built. The test equipment

offers the possibility for conducting variable angle bending tests at a fixed radius as well as under free-form (without a defined bending radius). A schematic of the test setup used for fixed radius bending tests is shown in figure 4.1. During the tests, one end of the CFPs was attached to the fixed platform while their other end fixed to the movable arm was bent repeatedly around a Polytetrafluoroethylene (PTFE) mandrel of a defined radius or under free-form bending without the PTFE mandrel. The motion of the movable arm was controlled by a stepper motor whose rotation was programmed through a software interface. The fixed end of the CFPs was connected to a parameter analyser for online monitoring of the electrical characteristics and a change in electrical characteristics was used as the failure criterion to detect failure of the CFPs. Upon occurrence of a failure, the samples were detached from the test equipment and they were optically inspected to identify the cause of failure.

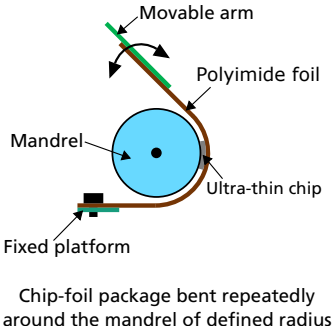

Fig. 4.1 Schematic of the test equipment used for the fixed radius dynamic bending tests [162]. Reused with permission from MDPI.

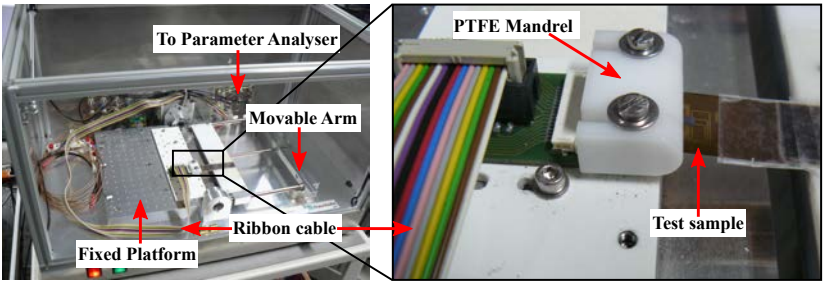

Fig. 4.2 Custom built test equipment used for the dynamic bending tests [162]. Reused with permission from MDPI.

The custom built test equipment used for dynamic bending tests is presented in figure 4.2. The equipment enables concurrent testing of 4 samples. The fixed platform was equipped with 4 PCBs each soldered with a Zero Insertion Force (ZIF) connector (Figure 4.3). The test samples were connected to the PCBs through their corresponding ZIF connectors and the PCBs were in turn connected to a parameter analyser with ribbon cables. In this work, daisy chain resistance of the samples was measured continuously and a change in resistance was set as the criterion for detecting failure. Precise measurement of electrical resistance was enabled by a high resolution semiconductor parameter analyser, *HP4156C*, from *Keysight Technologies* (Figure 4.4). The other end of the test samples was attached to the movable arm with a pressure sensitive adhesive tape. The motion of the movable arm was controlled by a stepper motor (from *Festo AG & Co. KG*) attached to the movable arm and the rotation of the stepper motor was controlled through a software interface. The software interface was developed using *Keysight VEE* which is a graphical dataflow programming environment from *Keysight technologies*. The developed software interface allowed to define the number of bending cycles, the bending angle and the frequency of bending cycles (Figure 4.5).

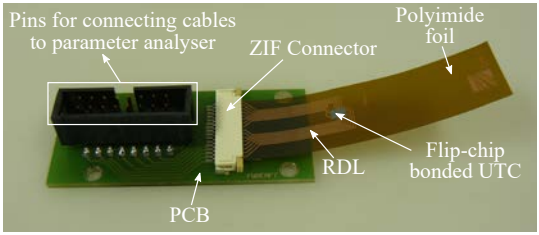

Fig. 4.3 A CFP sample attached to the PCB through the ZIF connector [162]. Reused with permission from MDPI.

4.2 Test protocol

The dynamic bending tests were conducted following a cyclic procedure during which the samples were bent from an initial flat 0° position to either a defined angle, for e.g. upright 90° position or to a complete fold at 180° position. Each bending cycle constituted of 4 steps in the following sequence:

1. 0° start position
2. Bending from 0° to 90° or 180°

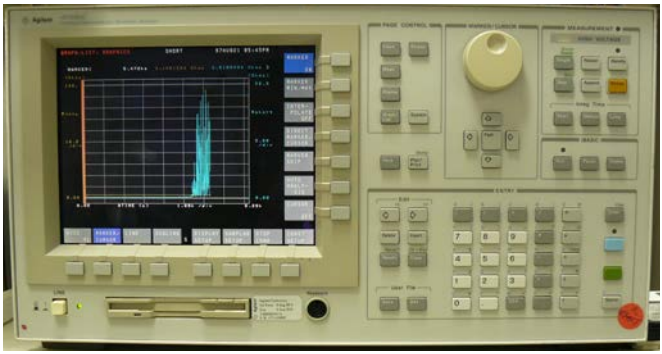

Fig. 4.4 Parameter analyser showing the plotted daisy chain resistance of a CFP during a bending test

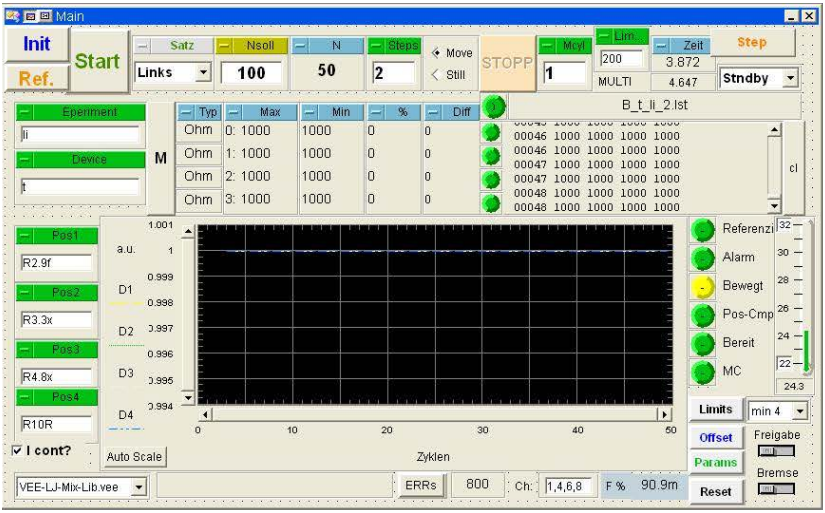

Fig. 4.5 Software interface used for controlling the dynamic bending tests

3. 90° or 180° rest position
4. Bending from 90° or 180° to 0° start position

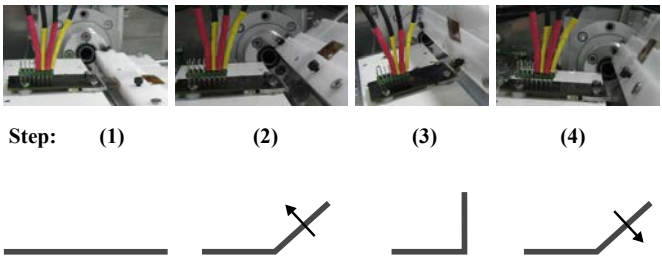

Fig. 4.6 Dynamic bending test protocol for a 90° free-form bending test [99]. ©2016 IEEE. Reused with permission from IEEE.

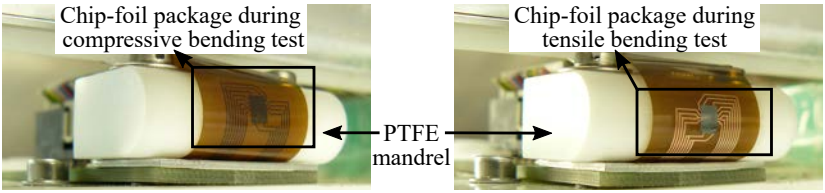

Fig. 4.7 Chip-foil package samples during 180° compressive and tensile bending tests at a bending radius of 5 mm

4.3 Choice of bending stress: Compressive vs. Tensile stress

4.3.1 Test samples

In principle, dynamic bending tests can be performed either by applying compressive or tensile stress to the CFPs. However, it is important to understand the effect of both types of stress and identify if one type of stress inflicts a higher damage to the CFPs than the other type. In order to understand the effect of both types of stress on the dynamic bending reliability of CFPs, repeated bending tests were performed on the CFPs where the samples were subjected to both compressive and tensile bending tests. The CFP samples used for the tests were fabricated by flip-chip bonding of chips with a thickness of 20 µm on PI foil

substrates (UPILEX 50S) with electroplated copper RDL patterns having a thickness of 10 µm. Then, the CFP samples were subjected to 180° bending tests at a bending radius of 5 mm under both compressive and tensile stresses. Four samples were tested for each stress type. The CFP samples consisted of three daisy chain test patterns and the resistance of one of the daisy chains was monitored continuously during the bending tests. A change in the measured daisy chain resistance was used as the indicator to identify failure of the test sample.

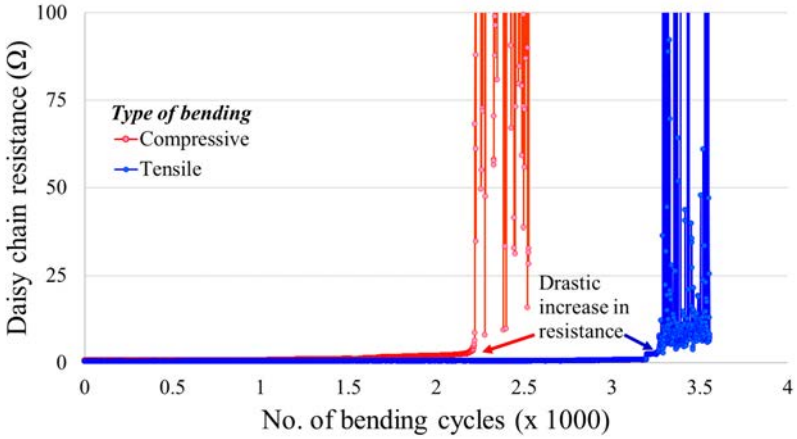

Fig. 4.8 Comparison of daisy chain resistance behaviour of CFPs during 180° compressive and tensile bending tests at a bending radius of 5 mm

4.3.2 Analysis of test results

The monitored daisy chain resistance during a 180° compressive and tensile bending test are plotted in figure 4.8. It can be noticed from figure 4.8 that both compressive and tensile bending induced an abrupt drastic increase in the daisy chain resistance. The abrupt increase in resistance indicates a failure caused by an open circuit and it can be seen that the failure occurred in the sample under compressive stress ≈1000 bending cycles earlier than the sample under tensile stress. Similar results were obtained from the other six test samples as well, thus confirming that the CFP samples are more vulnerable to compressive stress than to tensile stress (Figure 4.9). Furthermore, the mean bending cycles to failure from both

the tests suggest that the CFPs are ≈4 times more durable under tensile bending than under compressive bending (Figure 4.9).

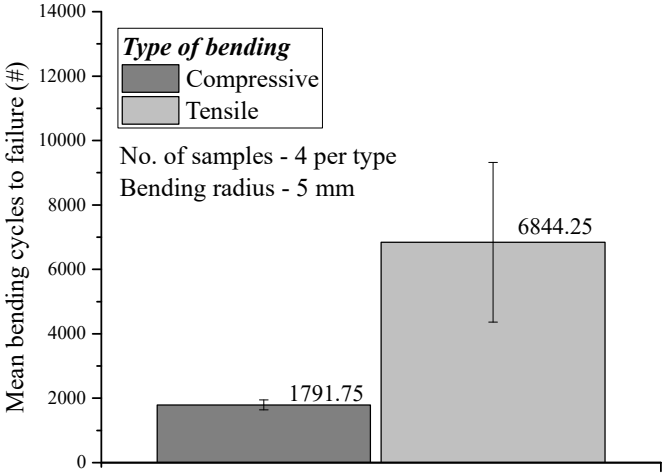

Fig. 4.9 Comparison of dynamic bending reliability of CFPs during compressive and tensile fixed radius bending tests at a bending radius of 5 mm

Besides 180° fixed radius bending tests, 90° free-form bending tests were also performed on CFPs under both compressive and tensile bending stress to verify if the obtained results are also valid for cases under free-form bending. The CFP samples for these tests were fabricated using relatively thicker chips with a thickness of 250 µm so that reasonably higher stress is induced on the RDL patterns during the bending tests resulting from the increased chip thickness. The chips were flip-chip bonded on to PI foil substrates (UPILEX 50S) with electroplated copper RDL patterns having a thickness of 5 µm. The obtained results were in coherence with the 180° fixed radius bending test results where the sample under compressive bending failed ≈300 bending cycles earlier than the sample under tensile stress (Figure 4.10).

Optical analysis performed on the CFP samples after the abrupt increase in resistance revealed that the increase in resistance was caused by the cracking of the RDL patterns perpendicular to the bending direction (Figure 4.11). Thus, it can be concluded that failure of CFPs during dynamic bending is caused by cracking of RDL patterns perpendicular to the bending direction as shown in figure 4.11.

Furthermore, investigations performed by A. Bag et al. [169] on PI foils having a thickness of 40 µm with 10 µm thick electro-deposited copper confirm that failure of their

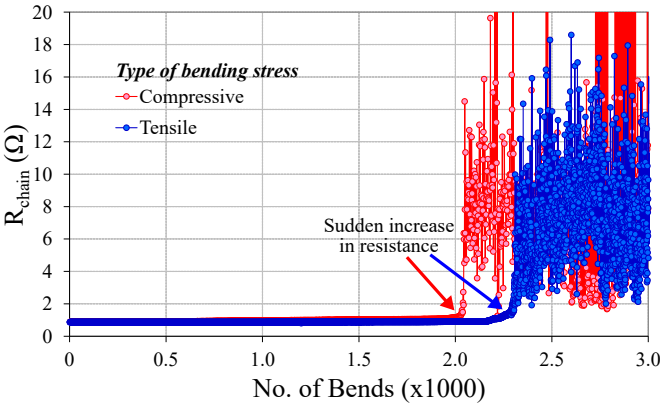

Fig. 4.10 Comparison of daisy chain resistance behaviour of CFPs during 90° free-form compressive and tensile bending tests. Figure originally published in [163]. ©2015 IEEE. Slightly modified and reused here with permission from IEEE.

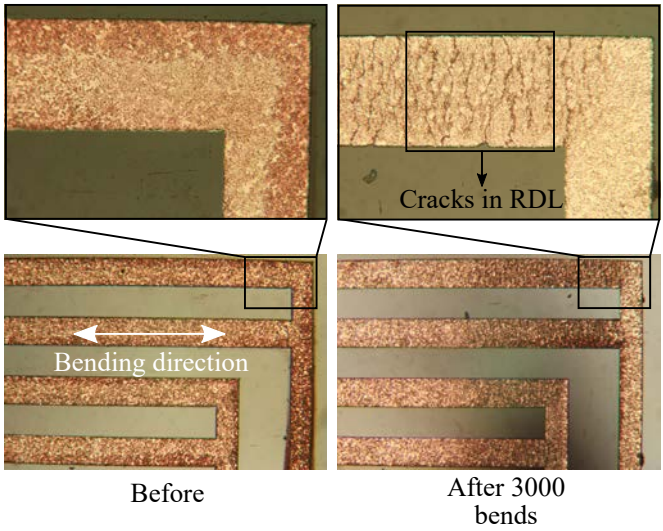

Fig. 4.11 Microscopic view of RDL patterns revealing the cracks perpendicular to bending direction after 3000 free-form compressive bending cycles at 90° bending angle. Figure originally published in [163]. ©2015 IEEE. Slightly modified and reused here with permission from IEEE.

test samples also occurred due to the formation of cracks in the copper layer. Their study also demonstrated that the average surface micro-crack length in the area of the sample under compressive bending was several times longer than those in the area under tensile bending, thus proving that compressive bending instigates comparatively larger damages to the copper layer than tensile bending. Therefore, further experiments in this work were performed only under compressive bending. A detailed analysis on the mechanism behind RDL cracking is included in the following section 4.4.

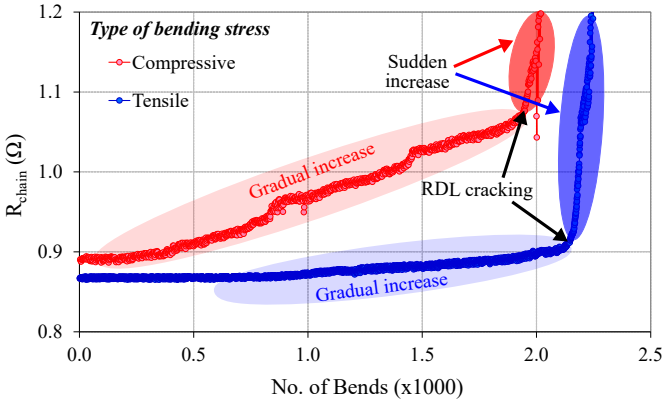

Fig. 4.12 A closer view to the change in daisy chain resistance shown in figure 4.10 elucidating the correlation between the cracking of the RDL and the increase in daisy chain resistance

4.4 RDL cracking mechanism

Figure 4.12 reveals that there are two distinct regimes in the behaviour of daisy chain resistance increase of CFPs during dynamic bending tests. Initially, the daisy chain resistance increased gradually before surging abruptly to higher values after ≈2000 bending cycles. Similar behaviour of daisy chain resistance during the bending tests was observed with other samples as well. Therefore, the daisy chain resistance behaviour of the RDL patterns in CFPs during dynamic bending can be considered to consist of two distinct regimes: (1) initial gradual increase and (2) abrupt surge. RDL cracking identified as the cause of the increase in resistance from post failure optical inspection can be correlated with the increase in daisy chain resistance to shed light on the RDL cracking mechanism. The correlation analysis indicates that the cracking mechanism of RDL patterns occurs in two phases: (a) the *"soft*

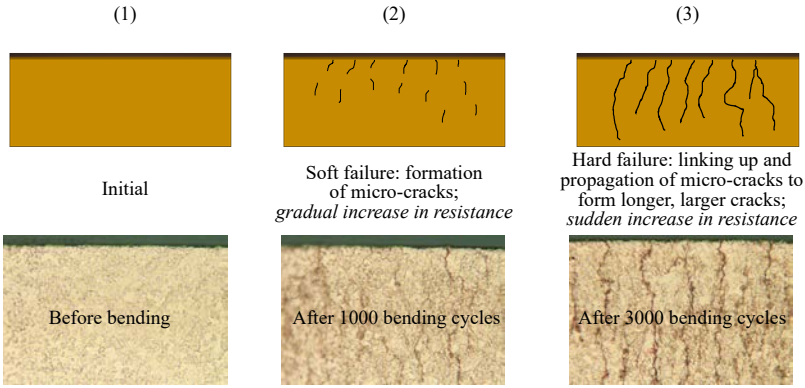

Fig. 4.13 Mechanism of formation of cracks in electroplated RDL patterns during dynamic bending test

failure" phase attributed by the initial gradual increase of the resistance and (b) the *"hard failure"* phase characterized by the abrupt surge in resistance. Figure 4.13 elucidates the RDL cracking mechanism by presenting microscopic images of the RDL captured at the same location during various stages of crack formation.

During the soft failure phase, several micro-cracks were instigated at various locations of the RDL (Figure 4.13 (2)) due to repeated bending attributed by the gradual increase in resistance. Various mechanisms such as intergranular fracture [170, 171], formation of dislocation microstructures at the intrusions at metal/substrate interface [172] and presence of defects such as voids [173] and particles at the metal/substrate interface [171] have been reported to initiate cracks. Considering these different mechanisms reported in the literature, crack initiation of the RDL patterns examined in this work could plausibly be attributed to ***intergranular fracture***. However, in-depth statistical evidences to support this hypothesis was not obtained in this study. Nevertheless, it is crucial to determine the exact mechanism causing the crack initiation of the RDL patterns. Therefore, further in-depth experiments and analysis to ascertain the mechanism behind the RDL crack formation are proposed for future studies.

During the second step in the crack formation process, the instigated micro-cracks grew longer across the width of the RDL and perpendicular to the bending direction as the bending cycles progressed leading to further increase in the daisy chain resistance. Finally in the third step, larger cracks started developing across the width causing the abrupt increase in the daisy chain resistance as exemplified by Figure 4.13 (3). This hypothesis is in coherence

with other studies that explain the correlation between the resistance increase and cracking of copper thin films [169, 174].

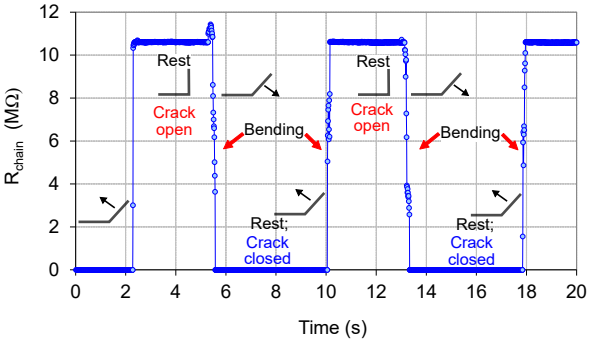

Fig. 4.14 Alternating increase and decrease in daisy chain resistance after abrupt increase due to opening and closing of RDL cracks after 5000 90° free-form tensile bending tests. Figure originally published in [163]. ©2015 IEEE. Slightly modified and reused here with permission from IEEE.

During further bending cycles after the sudden increase in resistance, the larger cracks opened and closed alternatively during repeated bending causing the alternating increase and decrease in resistance shown in figure 4.14. In case of tensile bending tests, the opening of the cracks under tensile state at 90° induced an increase in resistance whereas the closing of the cracks under relaxed state at 0° resulted in a decrease in the daisy chain resistance after the sudden increase as elucidated in figure 4.14. Therefore, it can be concluded that cracks observed on the RDL patterns under both compressive as well as tensile stress were instigated due to intergranular fracture. Apart from optical inspection, AFM section analysis was also performed on the RDL patterns after failure to validate the cracks. A typical section analysis of an RDL pattern across the crack is presented in figure 4.15.

4.5 Investigations on the factors influencing the dynamic bending reliability of CFPs

After identifying the critical bending stress type and the cause of failure, the influence of dimensional factors such as thickness of the integrated chip as well as the RDL on the cracking of the RDL and therefore the dynamic bending reliability of CFPs were investigated.

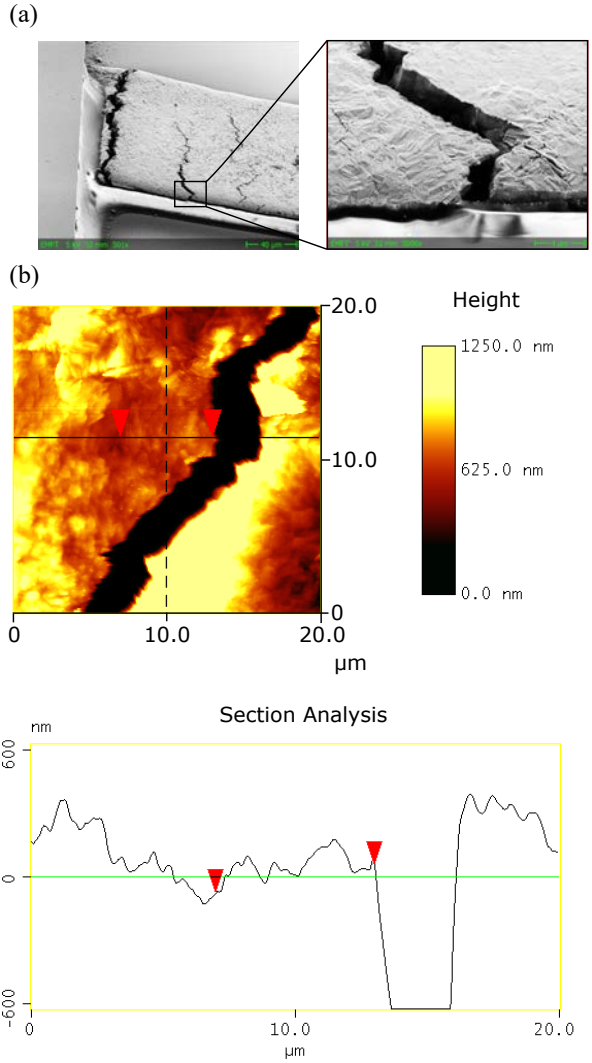

Fig. 4.15 AFM Section analysis of a crack in the electroplated RDL pattern

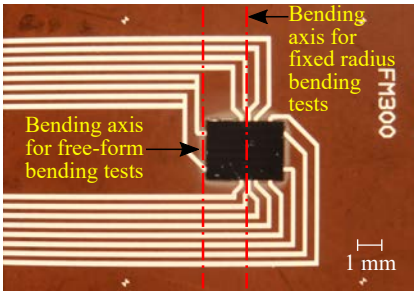

Fig. 4.16 Location of bending axis on the CFP for free-form and fixed radius dynamic bending tests [99]. ©2016 IEEE. Reused with permission from IEEE.

4.5.1 Chip thickness

Majority of ICs integrated in today's electronic devices are rigid having thickness in the range of few 100 µm. Despite their rigidity, considerable research is dedicated to the integration of thicker ICs and SMD components for creating FHE systems owing to the ease of their availability and minimal requirement for complete flexibility of the system [89–96]. Such FHE systems are normally designed in a way that the bending axis lies outside the location of the integrated rigid ICs and SMD components. Nevertheless, the rigidity of the integrated components would still affect the bendability and thereof the bending reliability of the FHE systems.

In order to investigate the influence of the rigidity of the integrated components on the dynamic bending reliability of the FHE systems, free-form repeated bending tests were performed on CFPs where the bending axis lie outside the chip area in the foil near the chip edges (Figure 4.16). The tests were performed with CFPs integrated with (a) rigid chips with a thickness of 250 µm and (b) flexible UTCs having a thickness of 28 µm.

2 CFPs for each chip thickness were tested and the test samples were prepared by flip-chip bonding of chips on UPILEX 50S foils with an RDL thickness of 4 µm following the process described in chapter 3. Figure 4.17 presents a typical result from the tests where the dynamic bending reliability of CFPs with 28 and 250 µm thick integrated chips are compared. Similar to the results presented in Section 4.3, failure of the both sample types was attributed by a sudden surge in the daisy chain resistance. However, CFPs integrated with flexible UTCs endured the dynamic bending test almost 2x longer than CFPs with rigid chips as exemplified in figure 4.17. Alike other investigations discussed earlier, the sudden increase in the daisy chain resistance was caused by RDL cracking which was confirmed by microscopic inspection of the samples before and after failure.

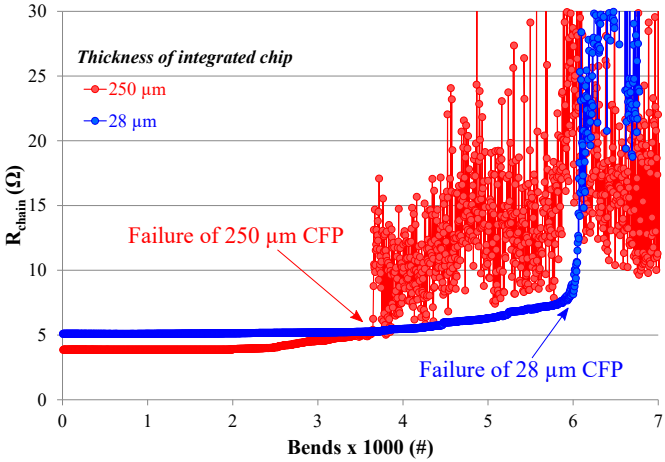

Fig. 4.17 Dynamic bending reliability of CFPs with two different chip thickness, 28 and 250 µm. Figure originally published in [99]. ©2016 IEEE. Slightly modified and reused here with permission from IEEE.

Table 4.1 Number of bending cycles until failure for CFPs with two different chip thicknesses

Chip Thickness (µm)	**Sample no.**	**Bending cycles until failure**
250	1	3654
	2	3873
28	1	12815
	2	6088

Further tests conducted on the other 2 samples also demonstrated similar results confirming that CFPs fabricated by integrating UTCs endured the free-form dynamic bending longer than CFPs integrated with thicker rigid chips, thus proving that the thickness (and therefore the flexibility) of the integrated chip affects the dynamic bending reliability of the CFPs even when the bending axis lies outside the chip area (Table 4.1). Hence, it can be understood that the thickness of integrated chip is a crucial factor determining the dynamic bending reliability of CFPs. The test results confirmed that the dynamic bending reliability of CFPs and thereof the FHE systems can be significantly improved by integrating flexible UTCs instead of thicker, rigid ICs even for quasi-flexible systems.

4.5.2 Thickness of RDL patterns

Thickness of the RDL patterns is another important dimensional factor affecting the dynamic bending reliability of CFPs. Besides, RDL thickness also governs the electrical performance of a system since electrical conductivity is directly proportional to the thickness of a conductor. In order to achieve good electrical performance, RDL patterns with higher electrical conductivity is preferred which can be realized either by increasing the width and thickness of the RDL patterns or by decreasing the length of the RDL patterns. However, increasing the width is normally not preferred due to various problems such as increased risk of defects and signal interference encountered while bringing the RDL patterns closer while decreasing the length is often not possible due to the challenges encountered in integrating the components closer to each other. Hence, improving the electrical conductivity by increasing the thickness of the RDL patterns is often preferred. However, increasing the RDL thickness would reduce its bendability due to the increase in stiffness. Therefore, the effect of RDL thickness on their bendability must be experimentally investigated to quantitatively understand the relationship between the RDL thickness and their dynamic bendability.

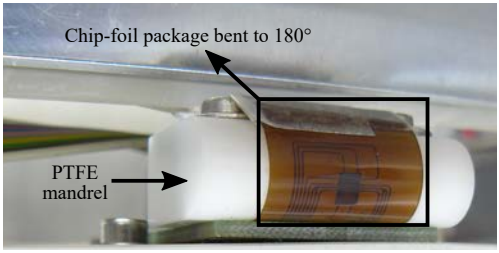

Fig. 4.18 A CFP sample bent to a radius of 5 mm around the PTFE mandrel during 180° dynamic bending tests. Figure originally published in [175]. ©2018 IEEE. Slightly modified and reused here with permission from IEEE.

Test samples

In order to investigate the impact of RDL thickness on the dynamic bending reliability of the CFPs, fixed radius repeated bending tests were performed at a bending radius of 5 mm. Since a bending radius of 5 mm suffices most applications targeting flexible electronics, it was chosen as the bending radius for the tests. The CFPs used for the investigations were fabricated by flip-chip bonding of UTCs with a thickness of 20 µm on UPILEX 50S foils with electroplated copper RDL patterns having thickness of 5 and 10 µm. 4 samples for each

RDL thickness were subjected to 180° compressive bending cycles until failure of the CFPs and a change in the daisy chain resistance was used as the failure criterion. A CFP sample bent around the PTFE mandrel during a bending test is shown in figure 4.18.

Analysis of test results

The obtained test results confirmed that CFPs with thinner RDL patterns having a thickness of 5 µm endured the bending cycles ≈33% longer than CFPs with 10 µm thick RDL patterns. Optical inspection performed on the CFPs upon failure revealed cracks on the RDL similar to figure 4.11. Figure 4.19 presents an SEM image showing the RDL crack. The results of the dynamic bending tests of CFPs with two different RDL thickness are summarized in figure 4.20. Therefore, it can be concluded that the flexibility of the RDL patterns can be improved by decreasing their thickness. Besides, the measured resistance of two daisy chains from the investigated samples with 5 and 10 µm thick RDL patterns revealed only a negligible difference of 16.91% and 11.7% respectively between each other (Figure 4.21). Therefore, it can be plausibly concluded that an RDL thickness of 5 µm is better than an RDL thickness of 10 µm due to better dynamic bending reliability and decent electrical conductivity.

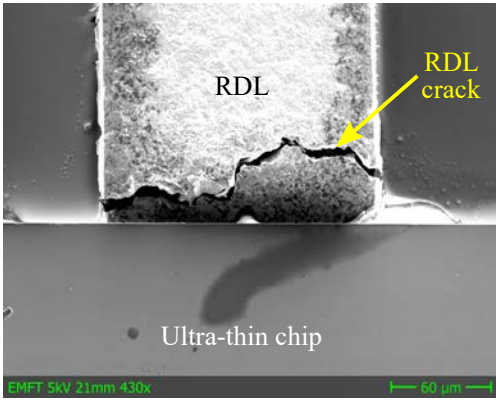

Fig. 4.19 SEM image of a CFP (top view) revealing an RDL crack. Figure originally published in [175]. ©2018 IEEE. Slightly modified and reused here with permission from IEEE.

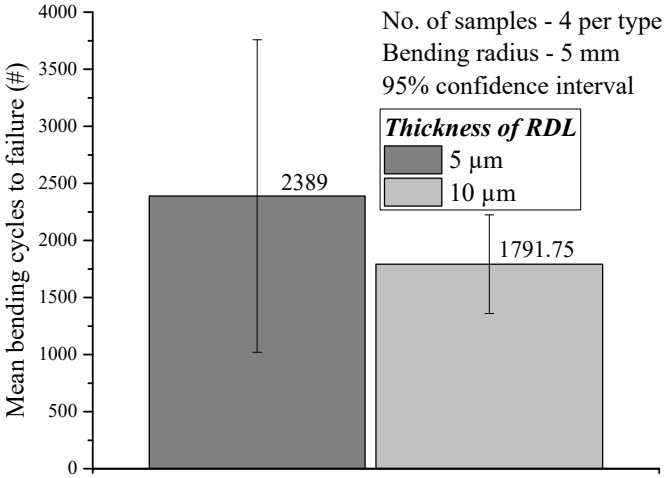

Fig. 4.20 Summary of dynamic bending reliability of CFPs with two different RDL thickness, 5 and 10 µm. Figure originally published in [175]. ©2018 IEEE. Slightly modified and reused here with permission from IEEE.

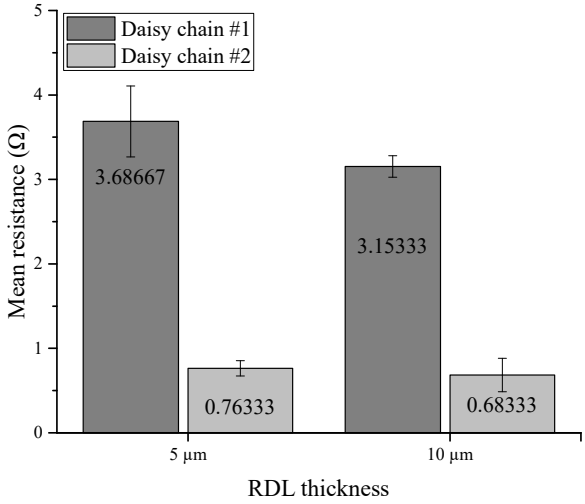

Fig. 4.21 Daisy chain resistance of CFPs with 5 and 10 µm thick RDL patterns

4.6 Strategies to enhance the dynamic bending reliability of the RDL

After identifying that the failure of CFPs during dynamic bending tests was caused primarily due to RDL cracking, two methods to enhance the robustness of the RDL listed below were experimentally analysed in this work.

1. By fabricating *very thin* RDL patterns
2. By fabricating RDL patterns with flexible metals

4.6.1 By fabricating *very thin* RDL patterns

Zhang et al. reported that the decrease in film thickness and/or grain size results in an increase in the number of bending cycles to failure for copper films in the thickness range of 0.2-3 µm [176]. Furthermore, investigations conducted by Wang et al. on copper films in the thickness range of 50 nm-3 µm revealed that a larger strain is required to initiate a failure as the thickness of the films was decreased, thus improving the fatigue life or the number of bending cycles to failure by decreasing thickness of the copper films [172]. Similar effect of film thickness on fatigue life of copper foils have also been observed by Dai et al. at µm scales [177]. These studies qualitatively elucidate that the fatigue or dynamic bending reliability of thin copper films could be enhanced by considerably decreasing the film thickness. However, a quantitative analysis of the improvement in the dynamic bending reliability of the thin copper films due to thickness reduction will complement the aforementioned studies and enable fabrication of reliable FHE components. This section discusses such a quantitative analysis that was performed in this work where dynamic bending tests were conducted on CFPs having RDL patterns that are several times thinner than the samples analysed so far.

Test samples

Investigations performed by Kim et al. on copper films having a thickness of 1 µm on 125 µm thick PI substrate under repeated bending showed that the crack density in the copper films increased gradually up to 50000 bending cycles and beyond 50000 bending cycles no significant increase in crack density was noticed [174]. Furthermore, Sim et al. recommend a thickness of 200-400 nm for thin metal films in order to achieve relatively longer fatigue life [178]. Therefore, RDL patterns with a thickness of 300 nm were fabricated by sputter deposition of copper on PI substrates having a thickness of 50 µm. Then, CFP samples were prepared by bonding UTCs with a thickness of 20 µm following flip-chip bonding processes

described earlier. The CFP samples were then subjected to 180° dynamic bending tests at a bending radius of 5 mm to investigate the improvement in dynamic bending reliability of CFPs fabricated with such *very thin* RDL patterns.

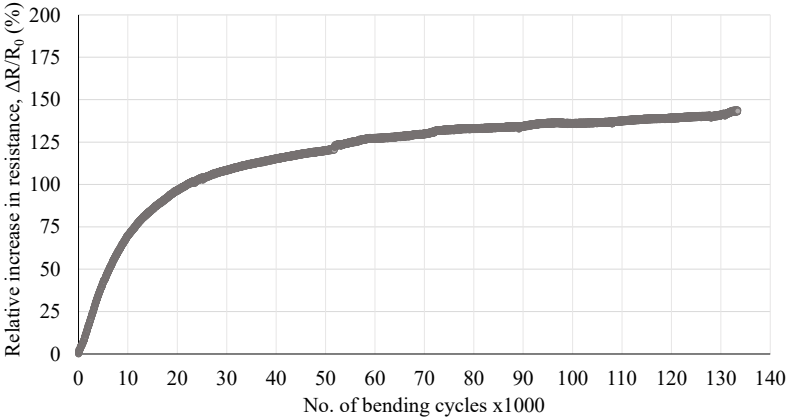

Fig. 4.22 Daisy chain resistance behaviour during fixed radius bending tests of a CFP with sputter deposited copper RDL. Relative increase in resistance, $\frac{\Delta R}{R_0} = \frac{(R-R_0)}{R_0} * 100\%$ where R is the resistance of the daisy chain at the corresponding bending cycle and R_0 is the initial daisy chain resistance at the start of the bending tests.

Analysis of test results

The test results revealed that the daisy chain resistance increased rapidly up to 20000 bending cycles beyond which the daisy chain resistance somehow saturated and showed only a gradual increase even up to 130000 bending cycles (Figure 4.22). A similar behaviour of the resistance during repeated bending has also been reported by Kim et al. [174]. Since no permanent failure characterized by an abrupt increase in daisy chain resistance was observed, further tests were conducted only up to 20000 bending cycles and a relative increase in daisy chain resistance of 100% was defined as the failure criterion. 5 CFP samples were subjected to repeated bending tests and all the samples showed a similar increase in daisy chain resistance up to 20000 bending cycles. The obtained test results are summarized in figure 4.23. It can be noticed in figure 4.23 that no sample reached the defined failure criterion of 100% relative increase in daisy chain resistance and the maximum daisy chain resistance increase was 96.6% with a mean daisy chain resistance increase of 87.6% after

20000 bending cycles. Therefore, it can be concluded that the dynamic bending reliability of RDL patterns can be significantly improved by fabricating thinner RDL patterns.

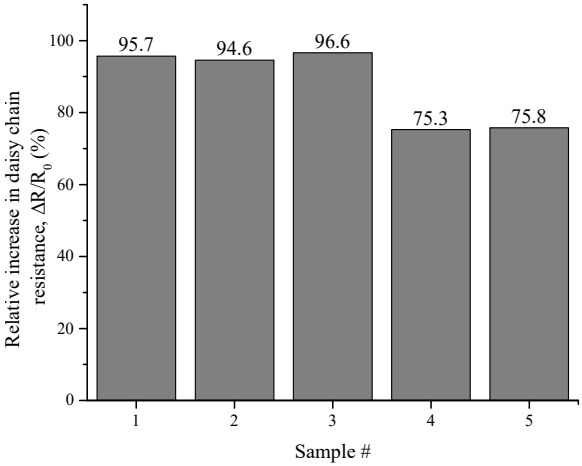

Fig. 4.23 Relative increase in daisy chain resistance of CFPs with *very thin* copper RDL patterns during 180° fixed radius bending tests

Optical and AFM inspections conducted on the samples after failure revealed the presence of a series of hillocks and absence of any crack on the RDL patterns (Figure 4.24(a)). Figure 4.24 also presents a closer view of the hillocks and the AFM section analysis of the hillocks. Hillocks are created in thin metal layers attached to a film substrate primarily due to uneven stress distribution. Such non-uniform stress distribution leading to hillock formation can be caused due to thermal or mechanical stress or both [171, 179–183]. Surface roughening and localised differential stress relaxation that occur during repeated mechanical stress have been reported to induce hillocks in thin metal films [171, 179, 180, 182, 183]. In this work, the dynamic bending tests were performed at room temperature and at a relatively slow speed. Hence, the effect of any local or external heating on the formation of hillocks in the RDL patterns can be excluded. Thus, it can be plausibly concluded that hillocks were created in the RDL patterns solely due to the repeated mechanical compressive stress resulting from the dynamic bending of the CFPs.

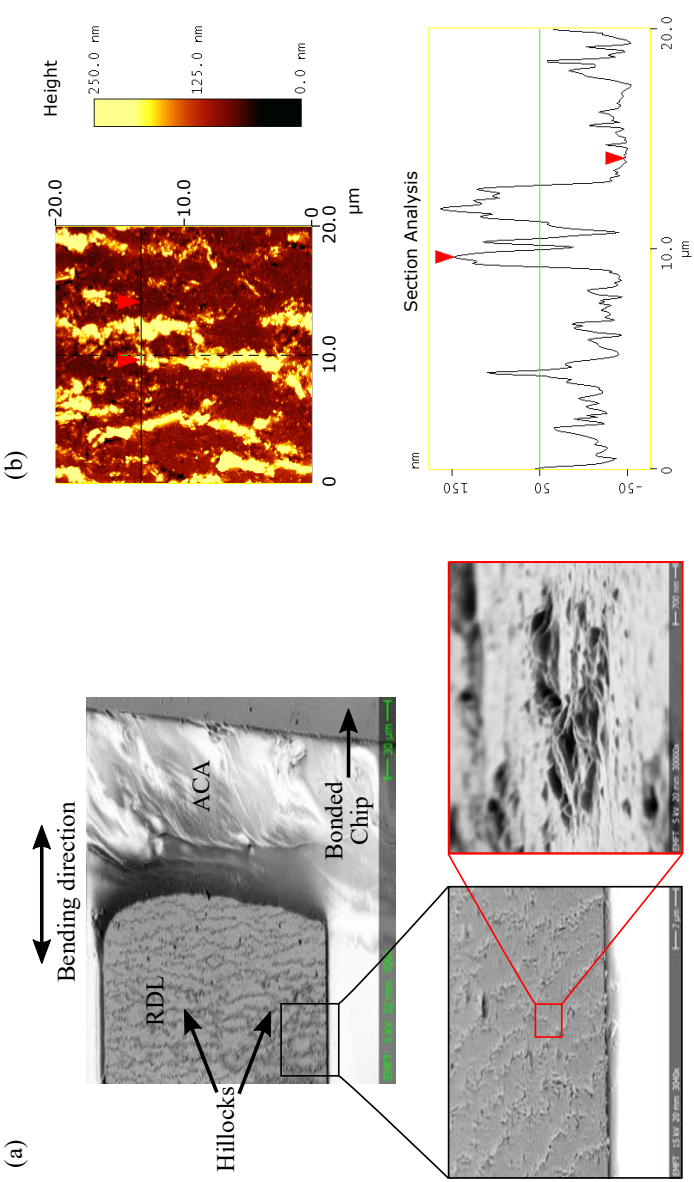

Fig. 4.24 (a) SEM images and (b) AFM section analysis of hillocks formed on sputter deposited copper RDL patterns after 20000 bending cycles [162]. Reused with permission from MDPI.

Although it was experimentally proven that the dynamic bending reliability of RDL patterns can be significantly improved by fabricating thinner RDL patterns, it is known that the electrical conductivity decreases with a reduction in RDL thickness which would in turn affect the electrical performance of the whole system. Therefore, a modular design that involves fabricating very thin RDL patterns at critical locations where bending is expected and thicker RDL patterns elsewhere could be adopted to improve the dynamic bending reliability while achieving decent electrical performance.

4.6.2 By fabricating RDL patterns with flexible metals

Though RDL patterns fabricated with thinner copper films demonstrated massive improvement in the dynamic bending reliability of the RDL, further enhancement can be achieved by using more flexible metals for fabricating the RDL. It is known that the stiffness of metals decrease with decrease in Young's Modulus and increase in Poisson's ratio, thus making them more flexible [184–189].

In order to experimentally verify the influence of flexibility of the metal constituting the RDL on its dynamic bending reliability, dynamic bending tests were performed on CFPs with RDL patterns fabricated from copper, gold and aluminum. Based on their material properties listed in table 4.2, CFPs with aluminum and gold RDL were expected to be more flexible than the CFPs with copper RDL.

Test samples

RDL patterns with a thickness of 300 nm were patterned by sputter deposition of the respective metals on UPILEX 50S foils. Then, the CFPs required for the dynamic bending tests were fabricated by flip-chip bonding of UTCs with a thickness of 20 µm using a commercially available ACA, Delo AC245. The CFPs were then subjected to 180° dynamic bending tests at a bending radius of 5 mm. Figure 4.25 presents the fabricated CFPs with copper, aluminum and gold RDL patterns.

Five CFPs were tested for each RDL metal type and each CFP was subjected to 20000 bending cycles. Owing to the difference in the measured sheet resistance of the metals (Table 4.2), a relative increase in resistance after 20000 bending cycles was used to compare the different RDL patterns and a 100% relative increase in resistance was set as the failure criterion.

Table 4.2 Material properties of metals used for fabricating RDL patterns [162, 190–192]

Metal	**Young's Modulus** (GPa)	**Poisson's ratio**	**Sheet resistance** (mΩ/□)
Copper	132	0.33	64 - 78
Aluminum	69	0.33	102 - 110
Gold	27-43.9	0.42	189 - 226

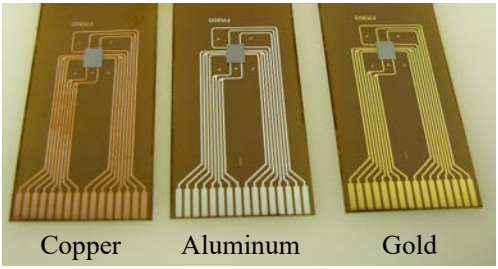

Fig. 4.25 CFPs with copper, aluminum and gold RDL patterns [162]. Reused with permission from MDPI.

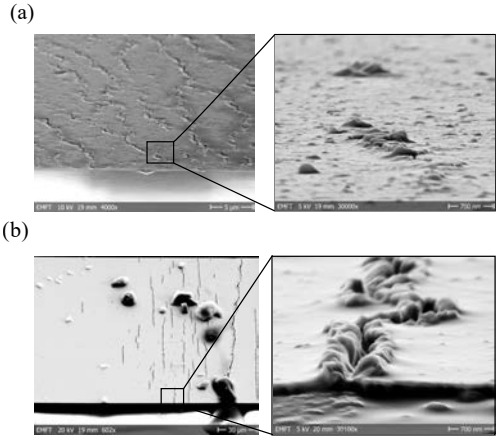

Fig. 4.26 SEM images of the hillocks formed on sputter deposited (a) aluminum and (b) gold RDL patterns after 20000 bending cycles [162]. Reused with permission from MDPI.

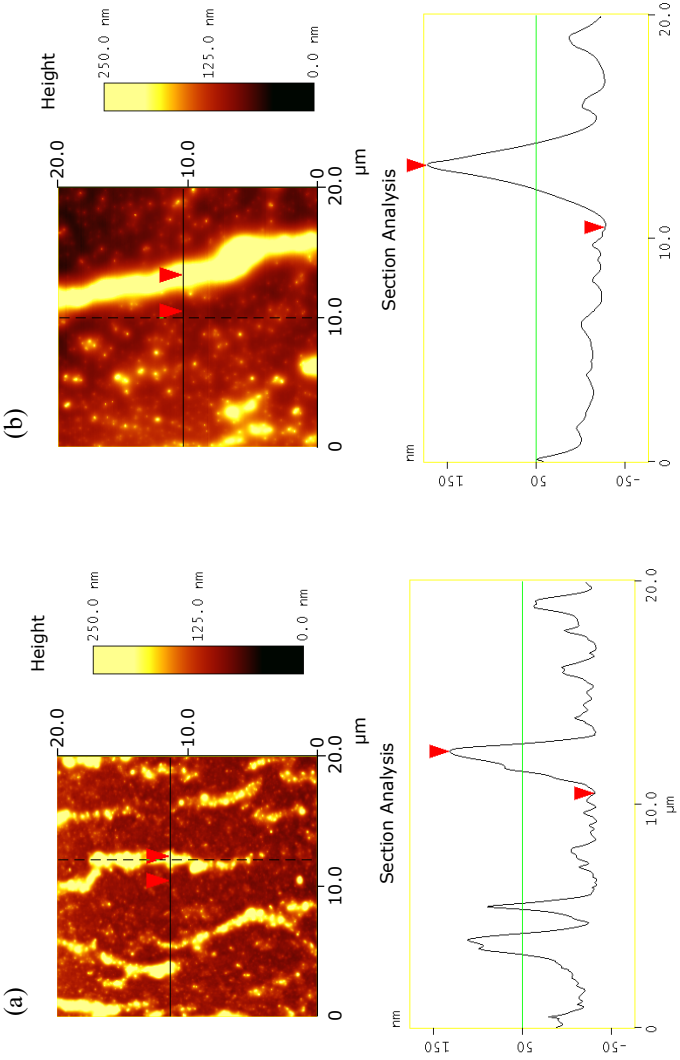

Fig. 4.27 AFM section analysis of a hillocks formed on sputter deposited (a) aluminum and (b)gold RDL patterns after 20000 bending cycles [162]. Reused with permission from MDPI.

Analysis of test results

Optical analysis performed on the samples after 20000 bending cycles revealed that the integrated chip remained intact and the gradual increase in resistance was plausibly caused due to the creation of voids in the RDL patterns characterized by the hillocks formed in the RDL patterns. Figure 4.26 and figure 4.27 present the SEM images of the hillocks and AFM section analysis formed on aluminum and gold RDL patterns after 20000 bending cycles. AFM section analysis performed on the hillocks formed on aluminum and gold RDL patterns after 20000 bending cycles revealed that the height of the hillocks was ≈250 nm. The mean relative increase in daisy chain resistance of the samples during 20000 bending cycles are summarized in figure 4.28. It can be noticed that the mean relative increase in resistance after 20000 bending cycles was less than 100% for all the test samples and hence it can be concluded that no permanent failure occurred on the test samples.

Among the three analysed metals, gold was the most flexible which demonstrated the least increase in mean relative increase in daisy chain resistance of 25.12% followed by aluminum and copper with 47.38% and 87.6% respectively. Therefore, it can be concluded that the dynamic bending reliability of RDL patterns can be further improved by fabricating RDL patterns using a flexible metal like gold instead of a stiffer metal like copper.

4.7 Dynamic bending reliability of face-up direct metal interconnected CFPs

The dynamic bending reliability of CFPs with face-up direct metal interconnected UTCs were also investigated in addition to CFPs with flip-chip bonded UTCs in this work. The CFP test samples were fabricated following the process outlined in Chapter 3. UTCs with a thickness of 20 µm and having the same layout as the ones used for flip-chip bonded CFPs were used to fabricate the face-up direct metal interconnected CFP test samples. 180° dynamic bending tests at a bending radius of 5 mm were conducted on 5 samples. The thickness of the RDL patterns and encapsulation polymer in the CFP were 5 µm and 15 µm respectively. Unlike the CFP samples with flip-chip bonded UTCs, the daisy resistance of the face-up interconnected CFPs demonstrated abrupt increase as early as after ≈50 bending cycles (Figure 4.29).

Analysis of test results

Upon the abrupt increase in daisy chain resistance, the samples were optically inspected and RDL cracking was identified as the cause of failure. However, the mechanism of cracking was different compared to that of CFPs with flip-chip bonded UTCs. Here, cracking of

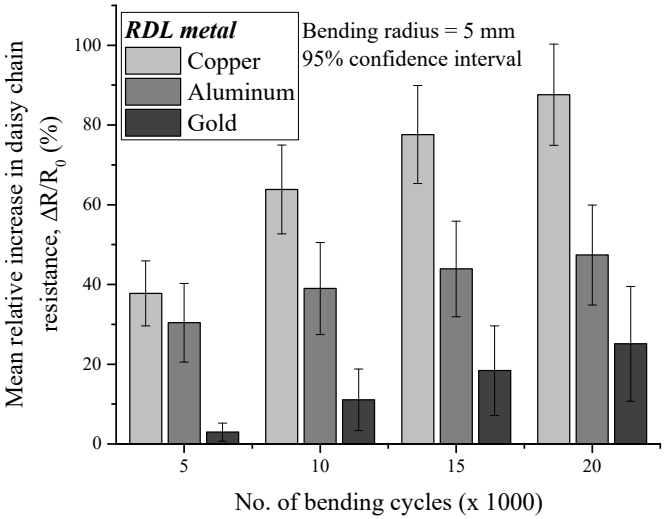

Fig. 4.28 Mean relative increase in daisy chain resistance of CFPs with copper, aluminum and gold RDL patterns during 180° dynamic bending tests at a fixed radius of 5 mm [162]. Reused with permission from MDPI.

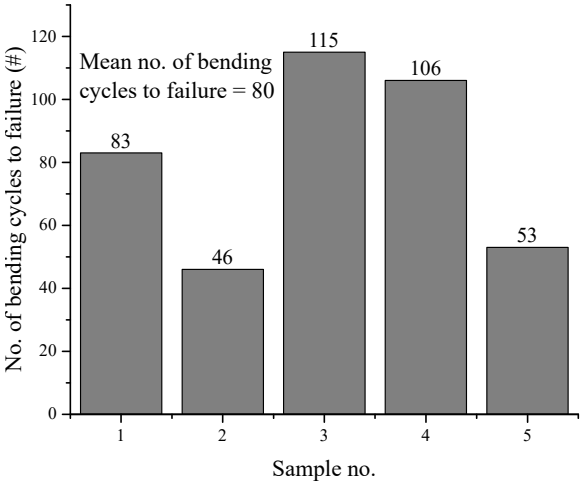

Fig. 4.29 Summary of dynamic bending reliability of face-up interconnected CFPs

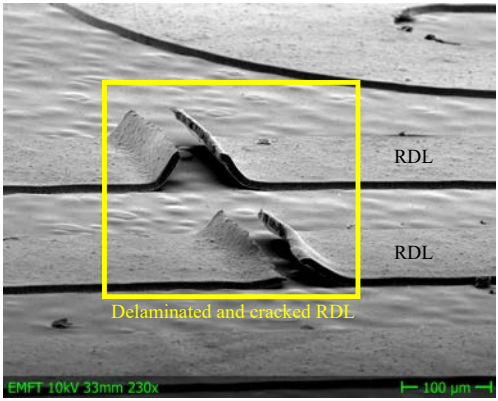

Fig. 4.30 SEM image with the delaminated and cracked RDL patterns

the RDL was first initiated due to delamination of RDL from the polymer surface followed by cracking. Figure 4.30 presents the SEM image revealing the delaminated and cracked RDL patterns. Generally, the adhesion of metal layers on polymers is enhanced by a plasma treatment step. However, it should be noted that the plasma treatment step performed prior to metal deposition did not have a significant effect on the adhesion of the RDL metal layer to the embedding polymer in these samples. Therefore, further in-depth investigations on the improvement of adhesion of RDL to polymers is recommended for future studies. These experiments underline that the novel face-up direct metal interconnection technique is still in its nascent stages of development and meticulous screening as well as analysis of the materials and processes involved in fabricating the samples is essential for fabricating reliable face-up direct metal interconnected CFPs. Thus, it can be concluded that comprehensive investigations on the metal-encapsulation polymer interface to improve the adhesion of RDL metal on to the encapsulation polymer is required for improving the dynamic bending reliability of face-up direct metal interconnected CFPs and at this stage, flip-chip bonding of UTCs is the preferred option for fabricating CFPs.

4.8 Summary

The dynamic bending reliability of CFPs was investigated by conducting repeated bending tests. An ad-hoc test equipment was built to perform the tests which enabled online monitoring of electrical characteristics of the CFP samples during the tests, thus enabling accurate

determination of the instance of failure occurrence. The electrical resistance of the daisy chain patterns of the CFP samples were continuously monitored to identify sample failure.

The tests indicated that the CFP samples are more vulnerable to compressive stress than to tensile stress. Optical inspection performed on the CFP samples revealed that the failure of CFPs during the bending tests was induced solely due to cracking of the RDL patterns. Besides, the RDL cracking mechanism was analysed and a hypothesis has been proposed to explain the RDL cracking. Analyses performed in this work indicate that the cracking of RDL patterns could plausibly be caused due to intergranular fracture. Then, the influence of thickness of the chip and the RDL on the dynamic bending reliability of CFPs was analysed. CFPs with thinner, flexible chips (t = 28 µm) endured the dynamic bending tests 2x longer than CFPs with thicker, rigid chips (t = 250 µm). Furthermore, it was found that CFPs with thinner RDL patterns (t = 5 µm) are 33% more robust to repeated bending than CFPs with thicker RDL patterns (t = 10 µm). Then, two strategies to enhance the dynamic bending reliability have been suggested and experimentally investigated. It was experimentally proven that the dynamic bending reliability of the RDL and therefore the CFPs can be significantly improved by fabricating *very thin* RDL patterns, however at the cost of electrical conductivity. Therefore, by fabricating very thin RDL patterns at critical locations where bending is expected and thicker RDL patterns elsewhere might improve the dynamic bending reliability without deteriorating the electrical performance. Furthermore, it has been experimentally proven that the dynamic bending reliability of CFPs can be remarkably increased by fabricating RDL patterns with flexible metals having lower Young's Modulus and higher Poisson's ratio.

Dynamic bending tests performed on CFPs fabricated using novel face-up direct metal interconnection process revealed that the failure of CFPs was caused due to delamination and cracking of RDL. The obtained test results demonstrated that the adhesion between the RDL and the polymer layer is a major factor influencing the dynamic bending reliability of the CFPs. Future works could focus on enhancing the interfacial adhesion between the RDL and embedding polymer thereby improving the dynamic bending reliability of the CFPs.

Chapter 5

Conclusion

The final chapter is dedicated to the concluding remarks of the thesis that provides a summary of the important findings and contributions. The up-and-coming Internet-of-Things (IoT) framework aims to establish uninterrupted fast communication between almost all physical objects of the world where billions of IoT nodes consisting of sensors and actuators would communicate with each other. Owing to the high performance capabilities of silicon ICs at low power requirements, flexible hybrid electronics (FHE) fabricated by integrating ultra-thin chips (UTCs) in polymer foils is foreseen to play a vital role in the successful implementation of IoT nodes. FHE is still an emerging technology and therefore information available regarding its bending reliability is very limited. This work aims to address this objective by investigating the static and dynamic bending reliability of Chip Foil Packages (CFPs) fabricated by integrating UTCs on polymer foils.

5.1 Key findings and contributions

The significant findings and contributions of this thesis are summarized below.

1. Static bending reliability of Chip Foil Packages (CFPs) were analysed by investigating the robustness of CFPs by performing 3-point-bending (3PB) tests to examine the fracture stress of the integrated UTCs. Fracture stress of the integrated UTCs were determined by calculating the fracture stress of standalone UTCs. Since fracture stress of UTCs can not be calculated using any standard formula owing to the non-linear force-displacement relationship of UTCs at higher displacements, Finite Element Method (FEM) simulations were performed to calculate the fracture stress of UTCs. In order to validate the FEM simulations, fracture stress of thin chips having thickness of 65 and 130 µm were also calculated using FEM simulations and the obtained results

showed very good correlation with the fracture stress values calculated using analytical formula. Though fracture stress of the chips is ideally independent of the thickness, experimental investigations revealed that the fracture stress decreased with a reduction in chip thickness. The mean fracture stress of chips with thickness of 30, 65 and 130 µm were 249, 415 and 516 MPa respectively. The decrease in fracture stress with a reduction in chip thickness underpinned the need to improve the fracture stress of thinner chips. This could be achieved by following advanced dicing and thinning processes such as plasma etching or longer stress relief processes to singulate the chips. Such plasma etching and longer stress relief processes would eliminate almost all of the micro-cracks as well as notches, thus resulting in defect-free edges and chip surface thereby improving the fracture stress of the chips. Alternatively, cost effective methods like embedding of the chips in polymer layers could also be adopted to improve the robustness of chips against external loads.

2. The robustness of UTCs embedded in polymer layers or CFPs and standalone chips were investigated by measuring their fracture force. The test results showed an enhancement of the fracture force of the CFPs due to the increased stiffness resulting from the embedding. The normalised increase in the mean fracture force of CFPs compared to standalone chips was 353,%, 65% and 11% for chip thickness of 30, 65 and 130 µm respectively. Thus, it can be understood that by embedding the UTCs in polymer layers and fabricating CFPs, the robustness of UTCs against external load can be remarkably improved while also preserving their conformability and flexibility.

3. The test results also indicated that the influence of embedding on the fracture strength of CFPs increased as the chips became thinner. Therefore, it can be plausibly concluded that embedding of chips in polymer layers is more crucial for UTCs than for relatively thicker chips.

4. In order to further enhance the robustness of UTCs against external loads, UTCs can be embedded in layers of materials with a higher Young's Modulus such as metal foils. FEM analysis performed on CFPs with Stainless Steel 316 embedding foils showed that the fracture force of UTCs can be immensely enhanced (by up to 16x more than CFPs with Polyimide embedding foils).

5. Acoustic Emission assisted Line-Load Tests were performed on CFPs and standalone UTCs with a chip thickness of 20 µm to analyse the effect of embedding on the dicing induced edge defects on the robustness of the UTCs. The test results showed that the robustness of both wafer sawn and plasma diced UTCs can be augmented by embedding

in foils. However, the influence of embedding on the robustness enhancement was higher for wafer sawn UTCs than for plasma diced UTCs. The mean fracture strength of wafer sawn UTCs was found to increase by 268% due to embedding whereas the plasma diced UTCs showed only 72% increase in fracture force after embedding.

6. Embedding of UTCs in polymer layers also helps to reduce the effect of surface defects created during wafer thinning. Ball-on-Ring tests performed on CFPs and standalone chips revealed that the mean fracture force of CFPs was 155%, 51% and 47% more than standalone chips for chip thickness of 30, 65 and 130 µm respectively.

7. Traditionally followed interconnection techniques like wire bonding is not suitable for UTCs since the high bonding pressure induced on the UTCs during the process would fracture them. Therefore, CFPs were fabricated in this work by following two other interconnection methods namely, (i) flip-chip bonding with Anisotropic Conductive Adhesive (ACA) and (ii) face-up direct metal interconnection. Both these developed processes have been demonstrated to reliably integrate and interconnect UTCs as thin as 20 µm. Besides, the compatibility of these processes with roll-to-roll (R2R) processing and their promising yield make them highly attractive for high volume industrial manufacturing of future flexible hybrid electronic components.

8. The dynamic bending reliability analysis of the electrically interconnected CFPs was investigated with a custom-built test equipment capable of bending the CFP samples either at free-form or at a fixed radius equipped with online monitoring of daisy chain resistance of the CFPs.

9. The CFPs were found to be more vulnerable to compressive bending stresses than to tensile bending stresses. Therefore, further tests in this work were performed only under compressive bending stress.

10. Post failure optical analysis conducted on the CFPs revealed that the failure of CFPs occurred due to cracking of the Redistribution layer (RDL).

11. By correlating the post failure optical inspection and the daisy chain resistance measured during the bending tests, intergranular fracture was identified as the likely cause of RDL fracture and a plausible mechanism for the RDL cracking that is in coherence with other published works has been proposed.

12. Furthermore, the influence of various dimensional factors such as chip and RDL thickness on the dynamic bending reliability of CFPs was analysed.

13. Though fully conformable and flexible FHEs are required for many applications, quasi-flexible FHE are also being developed where SMDs and rigid thicker ICs are integrated on foil substrates to suffice the bending requirements of systems which do not require total flexibility. Dynamic bending tests were conducted on CFPs integrated with rigid chips having a thickness of 250 µm and CFPs integrated with flexible UTCs with a thickness of 28 µm. The experimental results showed that CFPs fabricated with flexible UTCs endured the dynamic bending tests 2x longer than CFPs with thicker, rigid chips having a thickness of 250 µm. Thus, the influence of chip thickness on the dynamic bending reliability of fabricated CFPs becomes evident and it can be confirmed that UTCs are vital for fabricating reliable CFPs, even for semi-flexible systems.

14. Since electrical conductivity increases with an increase in thickness, proper dimensioning of the RDL is crucial for fabricating reliable CFPs. Dynamic bending tests performed with CFPs having thickness of 5 and 10 µm revealed that the thinner RDL patterns demonstrated ≈33% higher dynamic bending reliability.

15. After identifying the cause and understanding the mechanism of failure of CFPs during dynamic bending tests, two strategies to enhance the robustness of RDL during dynamic bending tests have been proposed and experimentally investigated.

    (a) CFPs with *very thin* copper RDL patterns having a thickness of 300 nm showed exceptional improvement in dynamic bending reliability. Furthermore, only a gradual increase in resistance was noticed even up to 130000 bending cycles. Therefore, a relative resistance increase of 100% was defined as the failure criteria. Dynamic bending tests conducted on CFP samples with such *very thin* RDL patterns up to 20000 bending cycles revealed only a maximum resistance increase of 96.6% and a mean resistance increase of 87.6%. Thus, it can be concluded that the CFPs with *very thin* copper RDL patterns are reliable up to 20000 bending cycles at a bending radius of 5 mm. However, such *very thin* RDL patterns would demonstrate poor electrical conductivity, thus hampering the electrical performance of the whole system. Therefore, fabricating *very thin* RDL patterns at critical locations where bending is expected and thicker RDL patterns elsewhere might improve the dynamic bending reliability without degrading the electrical performance of the system.

    (b) The dynamic bending reliability of CFPs can be hugely enhanced by fabricating RDL patterns with flexible metals having lower Young's Modulus and higher Poisson's ratio such as aluminum and gold. Dynamic bending tests performed

on CFPs at a bending radius of 5 mm with 300 nm thin aluminum and gold RDL patterns revealed that the mean relative increase in daisy chain resistance was much less than CFPs with copper RDL patterns. After 20000 bending cycles, the mean increase in resistance was 87.6%, 47.38% and 25.12% for CFPs with copper, aluminum and gold RDL patterns. Thus, it can be concluded that the dynamic bending reliability of CFPs can be significantly improved by fabricating CFPs with flexible metals like aluminum and gold.

16. Dynamic bending tests performed on CFPs fabricated by implementing face-up direct metal interconnection process revealed that the failure of CFPs was caused due to delamination and cracking of RDL. The test results underpinned the need for comprehensive investigations to enhance the interfacial adhesion between the RDL and the embedding polymer.

In conclusion, experimental results obtained from static 3-point-bending tests prove that embedding of UTCs improves the bending reliability of Flexible Hybrid Electronics (FHEs). Also, this thesis has experimentally verified that the dynamic bending reliability of FHEs could be drastically enhanced by fabricating RDL patterns with flexible metals such as gold having a thickness of 300 nm. In short, this thesis complements the state-of-the-art information available for fabricating reliable FHEs with several experimental results that are currently missing in the literature. Such experimental results obtained in this work could serve as guidelines for designing as well as fabricating reliable FHE components and systems capable of delivering high performance.

5.2 Outlook and perspectives for future works

The material properties used for FEM simulations performed in this thesis were taken from the literature. By experimentally determining the properties of actually used materials, process specific material properties can be obtained to achieve even more accurate simulation results. For example, Young's Modulus and Poisson's ratio of silicon that was used in this work would have been determined for complete wafers and these would vary for the UTCs owing to the damages induced in the crystal structure during the thinning as well as dicing processes. Furthermore, static bending tests could be conducted on CFPs by changing their stiffness with a selection of materials with varying Young's Modulus and Poisson's ratio to obtain in-depth experimental validation of the FEM simulation results reported in this work. Extensive 3PB tests could be performed with varying chip thickness below 30 µm for standalone as well as embedded UTCs to further enhance the understanding of fracture

strength of UTCs. The influence of thinning and dicing induced damages on the fracture strength of standalone as well as embedded UTCs investigated in this work are process specific. These investigations could be further widened to include other thinning and dicing processes to identify the most suitable technology for manufacturing reliable UTCs.

The flip-chip bonding and face-up direct metal interconnection processes were developed in this work for a chip pad pitch of 150 µm. However, advanced IC packages require much smaller pad pitches (<50 µm) to satisfy the demands of emerging applications. Therefore, the interconnection processes must be developed further to interconnect chips with smaller pad pitches.

Experimental results obtained in this work showed that the dynamic bending reliability of CFPs can be remarkably improved by fabricating CFPs with *very thin* RDL patterns with a thickness of 300 nm. However, such *very thin* RDL patterns would significantly decrease the electrical conductivity. Therefore, a trade-off between the RDL thickness and the electrical conductivity is required. Comprehensive studies to improve the adhesion between the RDL and the embedding polymer in face-up interconnected CFPs such as varying the embedding polymer, adhesion layer metal and chemical treatments could be performed in a follow-up work. Furthermore, the interconnection reliability for both flip-chip bonded and face-up interconnected CFPs could also be investigated. Finally, further in-depth investigations on vibrational, torsional and thermo-mechanical reliability of CFPs is essential to establish complete cognizance about the mechanical reliability of CFPs.

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Appendix A

Daisy chain test patterns

Daisy chain is a simple circuit pattern that is commonly used in IC packages during process development as a tool to understand the quality of interconnection between the IC and the substrate. Daisy chain patterns are also widely employed in the reliability analysis of the package when new materials are screened and tested. Usually, the measured electrical resistance of the daisy chain is used as the indicator for analysing the quality of the interconnection during process development as well as during reliability analysis. During reliability investigations, the daisy chain resistance is measured before (and sometimes during the test) and after the tests. In case of a failure, the resistance of the daisy chain increases often becoming an open circuit with exponentially high resistance.

A daisy chain circuitry constitutes of one set of daisy chain pattern on the IC complemented by another set on the substrate and the assembly process establishes interconnection between the IC and substrate through the daisy chain circuitry. Therefore, an ideal daisy chain interconnection would establish a short circuit with near zero Ohms resistance.

When a failure is noticed by means of an open circuit or an increase in the resistance beyond a defined threshold (after assembly process and/or during reliability tests), the package is microscopically analysed to identify the cause of failure. Various tools such as Optical Microscopy, Scanning Electron Microscope, X-ray Computed Tomography and Atomic Force Microscopy are usually employed to identify the cause of failure. The results are then used as a feedback to improve the assembly process before ”live devices” are packaged. Thus, daisy chain provides an easy and cost-effective means for assembly process development as well as for reliability analysis.

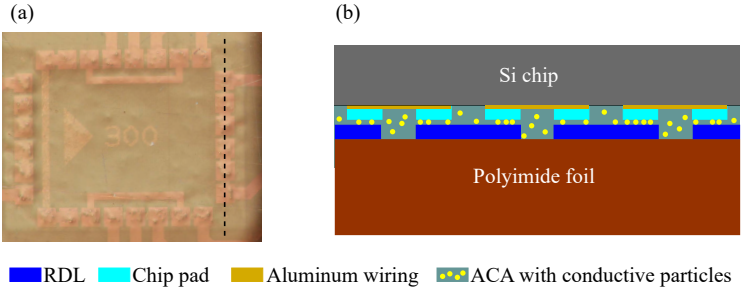

Fig. A.1 (a) Flip-bonded CFP viewed from the rear side through the Polyimide foil and (b) an illustration of the daisy chain with 6 single bonds investigated in this thesis

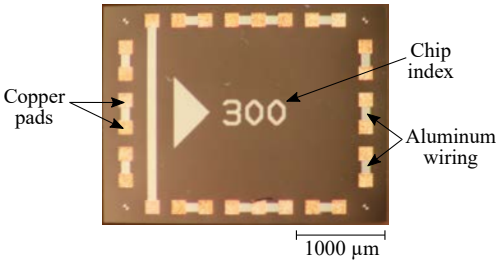

Fig. A.2 Layout of the test chip with daisy chain pattern

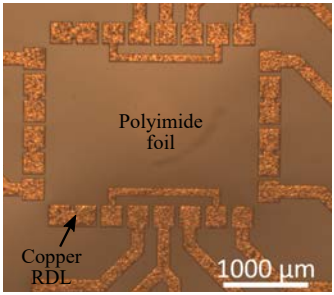

Fig. A.3 Layout of the Polyimide foil with daisy chain pattern

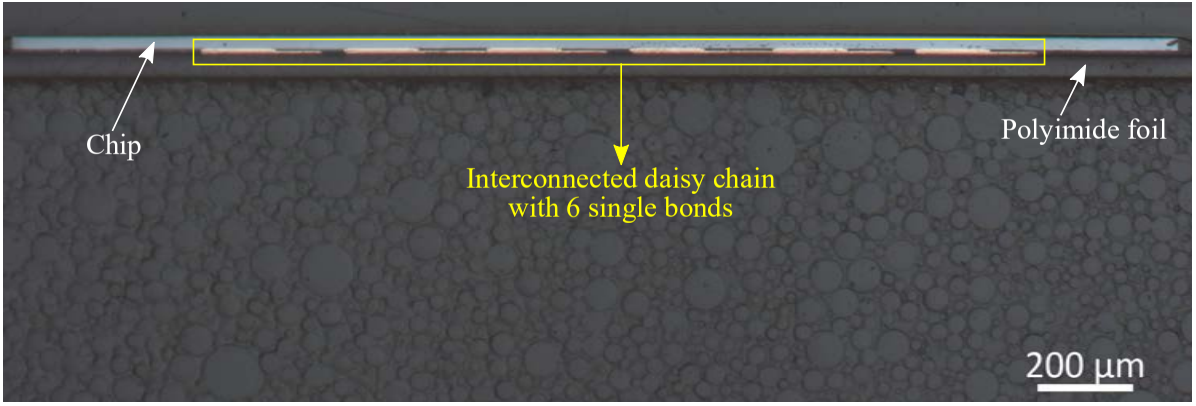

Fig. A.4 Cross-section of the interconnected daisy chain with 6 single bonds

The daisy chain pattern consisting of 6 single bonds between the chip and the polyimide foil investigated in this work during the dynamic bending tests is depicted in figure A.1. The daisy chain patterns on the chip constituted of a pair of 5 µm thick copper pads connected together with aluminum wiring having a thickness of 800 nm (Figure A.2). The complementary 5 µm thick copper daisy chain pattern fabricated on the polyimide foil is presented in figure A.3. The cross-section of the interconnected daisy chain with 6 single bonds investigated in this work is shown in figure A.4.

Appendix B

RDL cracks and hillocks

Dynamic bending reliability investigations performed on the chip foil packages (CFPs) revealed that failure of the samples occurred due to damages created on the RDL. However, two different types of damages depending on the grain size of the RDL were noticed. For CFPs with electroplated RDL patterns with bigger grains, permanent failure characterized by an open circuit occurred due to RDL cracking whereas CFPs with *very thin* sputter deposited RDL patterns revealed hillocks attributed by a gradual increase of resistance even after several thousand bending cycles.

Several SEM images showing the RDL cracks and hillocks in addition to those included in chapter 4 are presented here for further elucidation. It can be observed that the formed hillocks have varying shapes and sizes for different metal. Top view of the hillocks reveal a lot of dark areas next to the hillocks and these darker areas should not be misinterpreted as cracks. Isotropic and side views confirm that these dark areas are mere shadows of the hillocks rather than cracks.

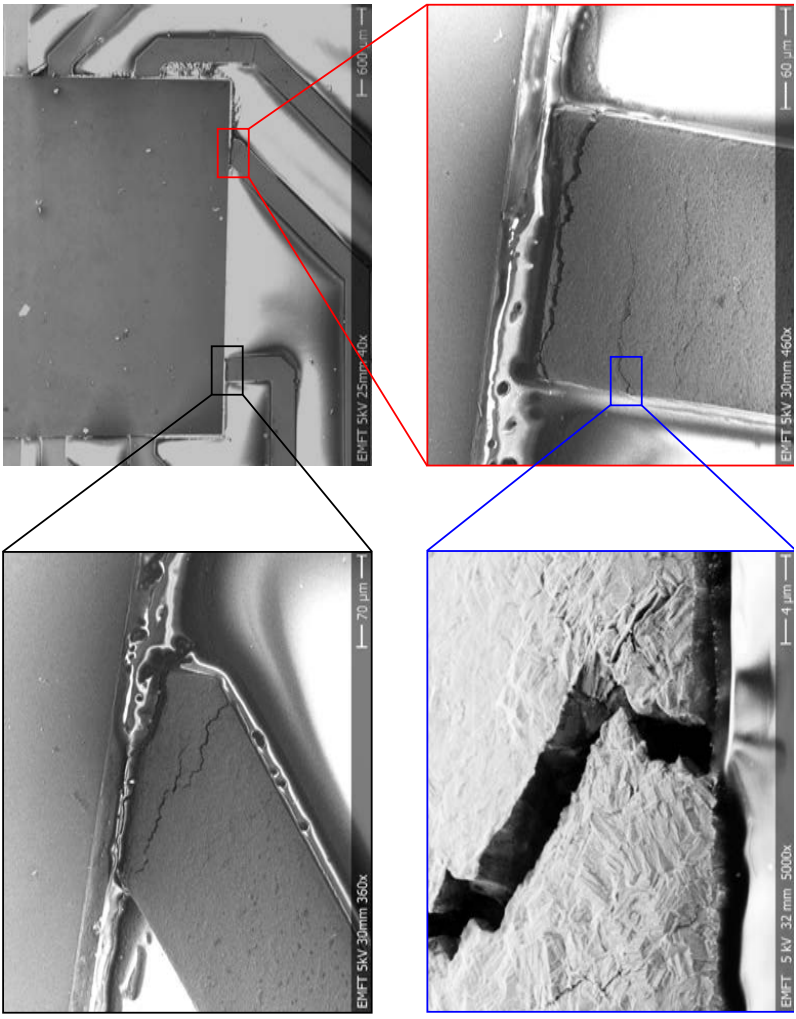

Fig. B.1 Cracks developed on electroplated copper RDL

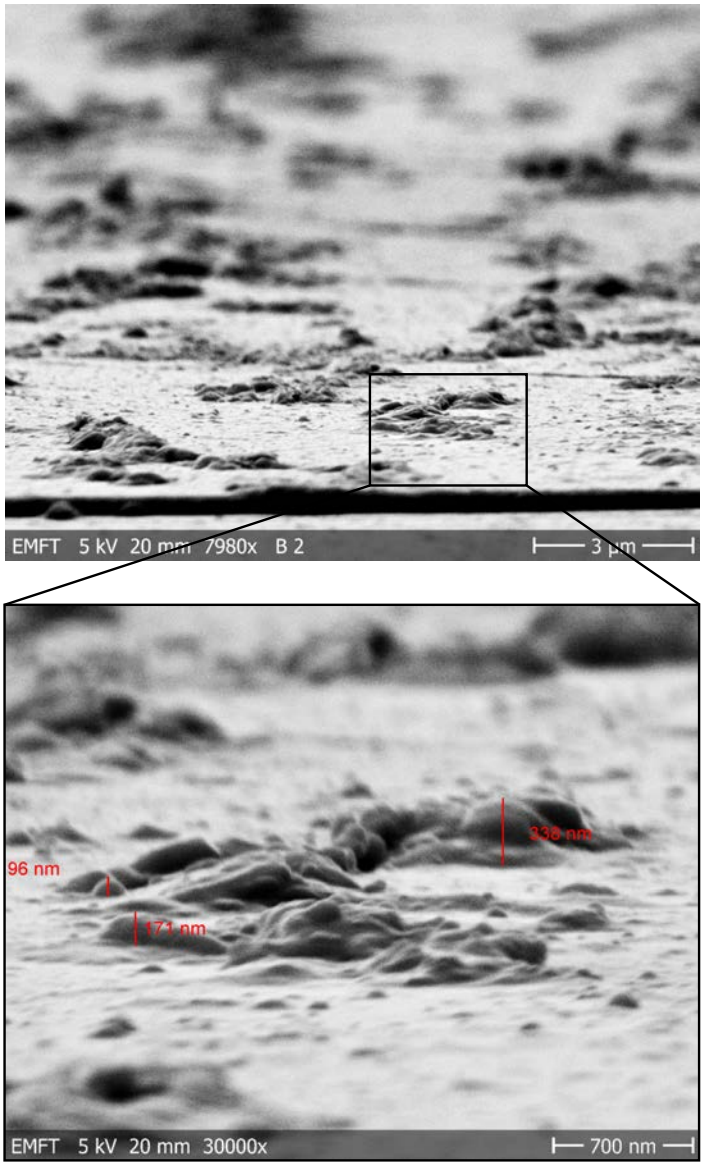

Fig. B.2 Hillocks created on sputter deposited copper RDL

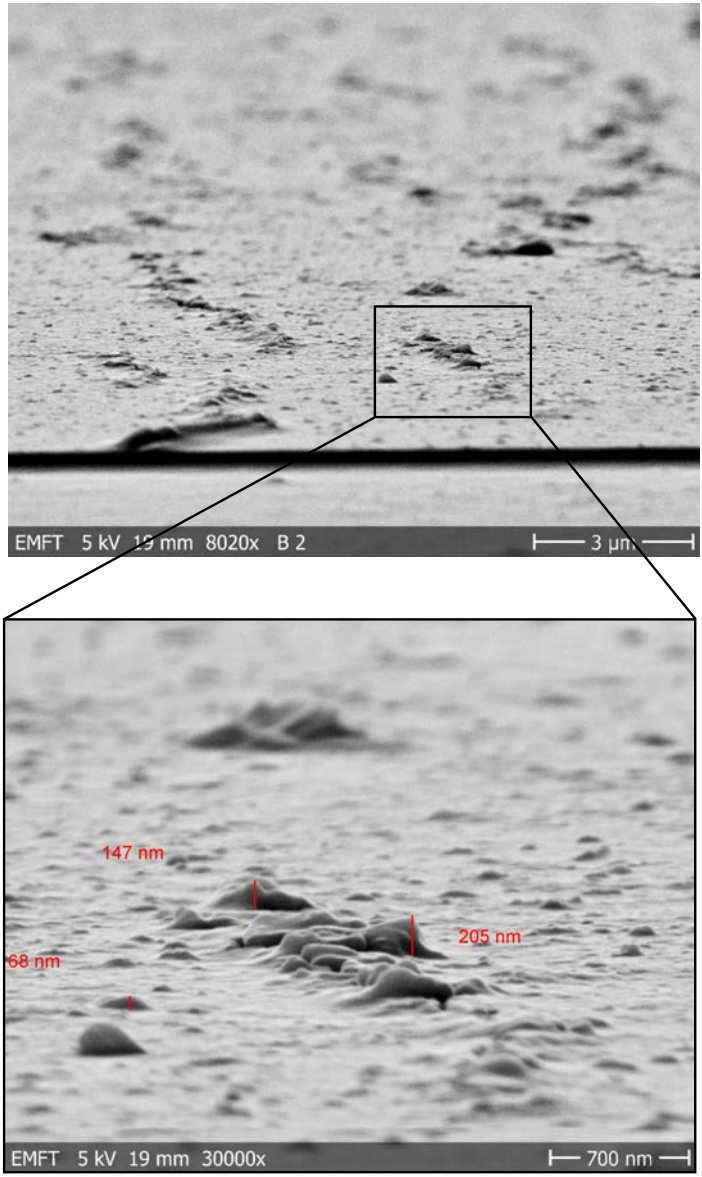

Fig. B.3 Hillocks formed on sputter deposited aluminum RDL

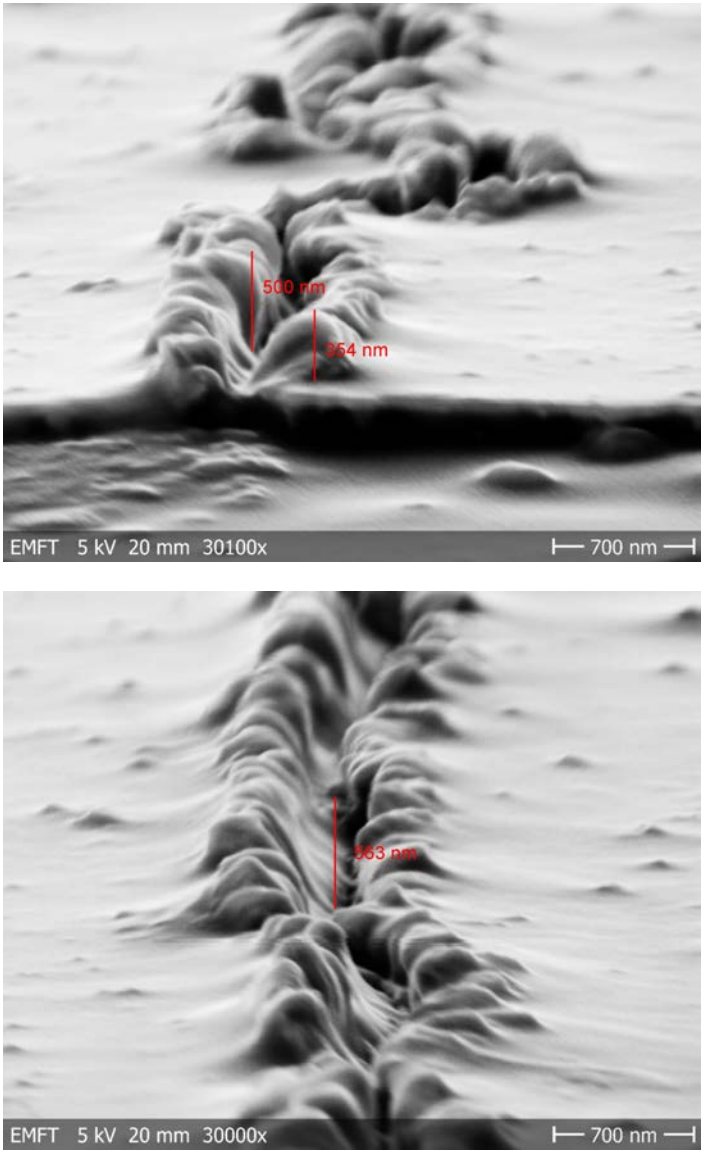

Fig. B.4 Hillocks inflicted on sputter deposited gold RDL