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A MODIFIED DOMINO LOGIC CIRCUIT FOR IMPROVED NOISE IMMUNITY AND DELAY VARIABILITY

RAVIKANT THAKUR[1], AJAY KUMAR DADORIA[2], TARUN KUMAR GUPTA[3]
[1, 2, 3] Electronics and Communication Department, MANIT, Bhopal, INDIA
[1]ravielex55@gmail.com, [2]ajaymanit0@gmail.com, [3]taruniet@rediffmail.com

ABSTRACT

This paper gives an approach for improvement in the reduction in delay variation in a domino logic circuits and it also gives improved noise immunity to the circuit. The improvement in delay observed here is better in the proposed circuit and the noise immunity is also enhanced by a good margin. The simulation process here is done by using Cadence Virtuoso 65nm process technology at 27°C operating temperature and 0.8 V operating supply voltage (V_{DD}) for the circuit.

Keywords: *High speed integrated circuit, dynamic logic circuit, Unity noise gain (UNG), Domino logic circuit, Noise immunity.*

[1] INTRODUCTION

Most of the dynamic logic circuits are used to achieve reliability, high speed, and compact circuits by using least complicated clocking scheme [9], [7]. Domino CMOS logic gates allow a significant reduction in number of transistors required to realize any complex Boolean function. A wide range of circuits where high speed and high performance is taken into consideration, Domino logic circuits are used. Keeper transistor approach is used in various domino logic circuits [6]. Some keeper transistor approach makes the circuit leakage tolerable but costs some performance regarding noise immunity [3], [5]. In Domino logic circuits the high performance is achieved because of the reduced input capacitance, observed by the driver gate [8]. Domino circuits are widely used in high performance microprocessors and DSP circuits, such as high fan-in multiplexer or comparator circuits [10].Section (1) explains some basics of Domino logic circuits. Typical conventional approach has been discussed in section (2). Section (3) gives the brief of proposed circuit for the betterment of the noise margin. Simulation result and conclusion is discussed in Section (4) and Section (5) respectively.

[2.1] CONVENTIONAL APPROACH

The approach used here is to reduce the delay variation associated in the circuit. The Domino logic circuits are highly used for high speed and high performance applications. The problem of delay variation causes mostly in high performance application circuits, so, for Domino logic circuit the delay variation plays an important role. Therefore one should reduce the variation in delay as much as possible.

The previous analysis [1], [2] shows that delay variability in domino logic circuits is almost double compared to static logic circuits. Also it gives two important phenomenon that:-

a) The variability of delay at dynamic node is almost equal to the overall delay variability.
b) Variation in keeper transistor and pre-charge transistor do not significantly contribute to the delay variability at dynamic node.

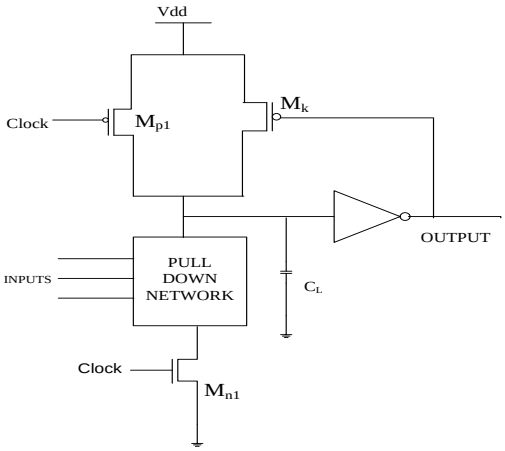

Fig. 1: Simple Domino logic circuit

Therefore the conclusion to maintain the variability is that, the attention must be given to the positive feedback loop implemented by using the keeper transistor and the inverter. The delay variability here has calculated by using Monte Carlo simulation. The ratio of mean value of certain amount of delay sample and the variance of the same amount of sample is known as delay variability.

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[2.2] APPROACH USED

The positive feedback loop analysis:-

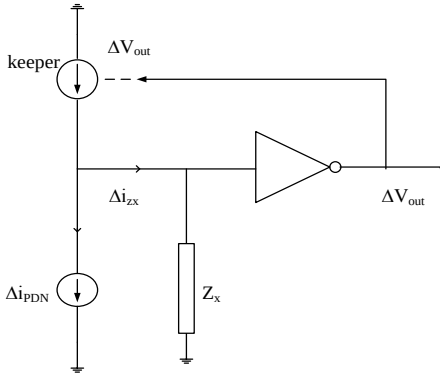

Fig. 2: Feedback loop analysis of Circuit

To calculate the small signal loop gain the pull down network can be considered as a dependent current source and the keeper transistor as an independent current source controlled by ΔV_{out}.

$$\Delta i_{KEEPER} = -G_{m,KEEPER} * \Delta V_{out}$$

$$\Delta V_x = Z_x \Delta i_{zx}$$

$$\Delta i_{zx} = \Delta i_{PDN} - \Delta i_{KEEPER}$$

Therefore the feedback associated keeper transistor having non-inverting loop gain (T) can be given by-

$$T = A_{INV}\, G_{m,KEEPER} * Z_x \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Where A_{INV} = Voltage gain of Inverter

As equation (1) indicates, to reduce the loop gain the reducible parameters can be either A_{INV} or Z_x or $G_{m,keeper}$. In the conventional approach the main focus given is to reduce $G_{m,keeper,}$ so that the loop gain can be minimized. The desired condition can be achieved by –

A) By splitting the keeper transistor into two keeper transistor :-

In the figure the keeper transistor M_{k1} is driven by the transistor and the second keeper M_{k2} here works as a resistor of which the resistance is

$$R \approx [\mu_p C_{ox} \left(\frac{W}{L}\right)_{kp2} (V_{DD} - |V_{tp}|)]^{-1}$$

and

$$G_{m,eff} = \frac{G_{m,M_{kp1}}}{1+G_{m,M_{kp1}} R} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

By observing equation (2) it clearly shows the desired reduction in the trans-conductance, $G_{m,keeper}$ associated in the circuit.

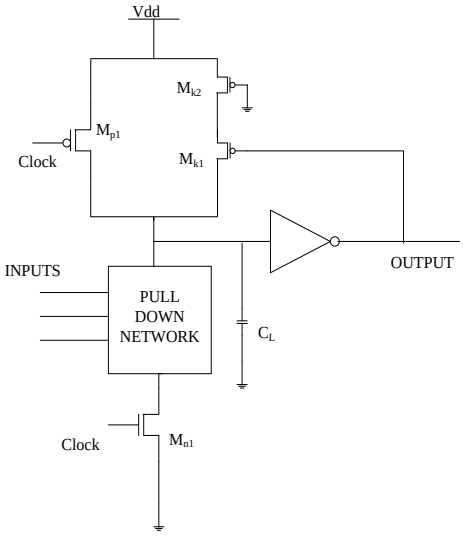

Fig. 3: Domino Logic Circuit with two keeper

Vol 05, Article 08398, September 2014 International Journal of VLSI and Embedded Systems-IJVES
http://ijves.com ISSN: 2249 – 6556

B) By sizing the transistor :-
To provide the same DC current as the basic domino circuit, it is necessary to size M_{kp1} and M_{kp2}. Here the transistors are in series therefore

$$(L/W)_{kp1} + (L/W)_{kp2} = (L/W)_{kp}$$

and hence $W_{kp1}=W_{kp2}= W_{min.}$
& $L_{kp1} + L_{kp2} = L_{kp}$

That equation shows that the overall length for the keeper transistor is the same, therefore the increment in silicon area is negligible.

[3.1] PROPOSED TECHNIQUE FOR A LEAKAGE TOLERANT AND BETTER NOISE MARGIN CIRCUIT

The proposed circuit here is implemented in 65 nm Cadence Virtuoso CMOS technology with the power supply of 0.8 V. The proposed circuit is based on footed domino logic circuit and based on this the proposed circuit is given which is having better leakage tolerance and improved noise immunity. The circuit is shown in Fig. 4 and has been simulated for 2, 4, 8 and 16 inputs OR gate.
To operate the circuit basically there are two modes of operation, namely pre-charge mode and evaluation mode. During pre-charge phase, the dynamic node of all the gates are charged to V_{DD}, which also causes the inverter output to go to 0 V. Now during the evaluation phase the logic signal associated with the pull down network is evaluated and the inverter output perhaps changes from 0 to V_{DD} or some inverter output may remain at ground depending upon the logic signal provided to the pull down network.
In the proposed circuit an NMOS is added as shown in Fig. 4. The main function of this transistor is to draw the contention current of the PMOS keeper and also it helps to speed up the discharging process of the capacitor at the dynamic node. At the beginning of the pre-charge mode the pre-charge device is in active mode. Therefore the voltage at the dynamic node will be at 0 V and hence that will pass through an inverter so the output at the inverter will be V_{DD}. In consequence the extra added transistor will turn on and at the beginning of the pre-charge phase there will be contention of current between the two current derived from the extra added transistor and the keeper transistor because the pre-charge device tries to charge the capacitor C_L and the current due to the added NMOS tries to discharge the capacitor C_L

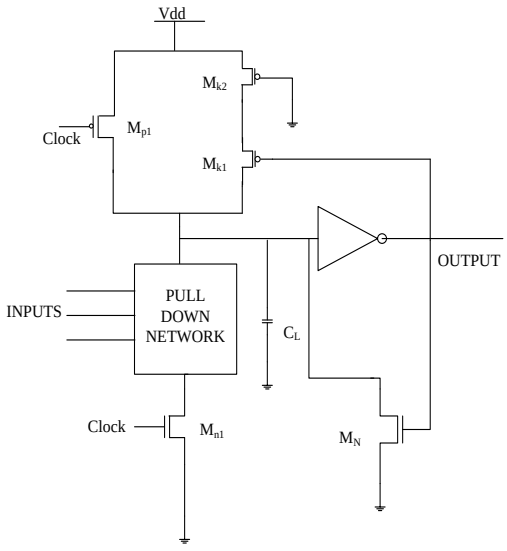

Fig. 4: Proposed modified Domino Logic Circuit

During the evaluation phase the pre-charge device gets OFF because at this time the clock switches from logic '0' to logic '1'. Now the cases where inputs are such that the capacitor C_L must retain the charge, then the output will be zero. Also if the inputs are such that the Pull down network must discharge the capacitor C_L, then the dynamic node voltage will start decreasing. At the beginning of discharging process the inverter output will be at zero, which will cause the extra added NMOS to stay inactive. The extra added NMOS compensates the keeper current and speed up discharging of capacitor C_L.

[3.2] UNITY NOISE GAIN

To check whether the circuit is tolerable to the noise or not, it may be checked by applying a small noise pulse to all the inputs provided to the circuit. That input noise pulse should be given primarily during the evaluation

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phase. To check the noise immunity the metric used here is Unity noise gain. The amplitude of the input (noise input) for which the amplitude of the output is same as the input is known as Unity Noise Gain (UNG). Mathematically it can be presented as

$$UNG = (V_{noise}\ ;\ V_{noise} = V_{out})$$

[4] SIMULATION RESULT

The simulation process here is done by using Cadence Virtuoso Tool 65 nm technology using analog design environment (ADE). The previous analysis shown in the conventional approach is majorly concentrated on the variation in delay in a Domino logic circuit and simulated in both 65 nm and 90 nm technology. In this proposed circuit the comparison of delay with the conventional circuit is done, using 65nm technology only and it is observed that the delay in both the circuits are almost same. In the proposed approach various parameters such as delay, Unity noise gain (UNG) and average power dissipation has been calculated for different-different inputs such as 2, 4, 8 and 16 inputs. The parameters calculated here is obtained by applying supply voltage V_{DD} as 0.8 V and operating temperature as 27^0 C. The result which compares the UNG of proposed circuits with the traditional circuit is shown in Table 1.

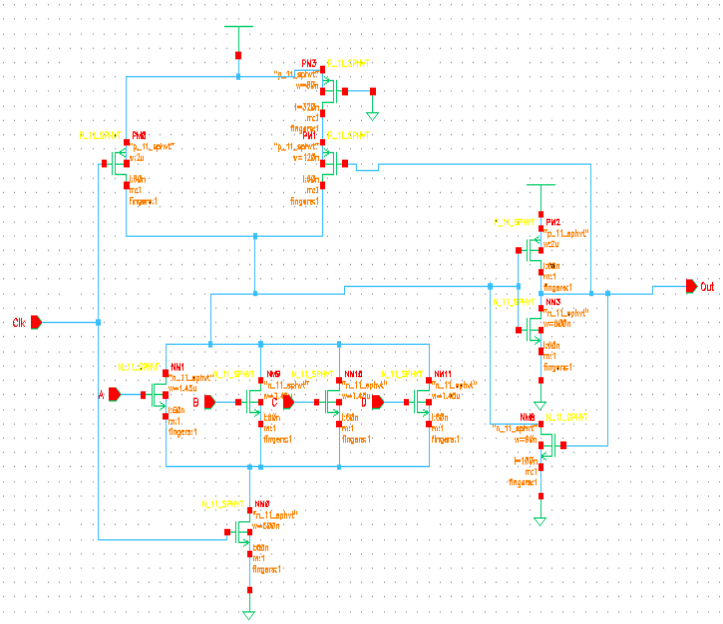

Fig. 5: 4 inputs proposed domino OR logic

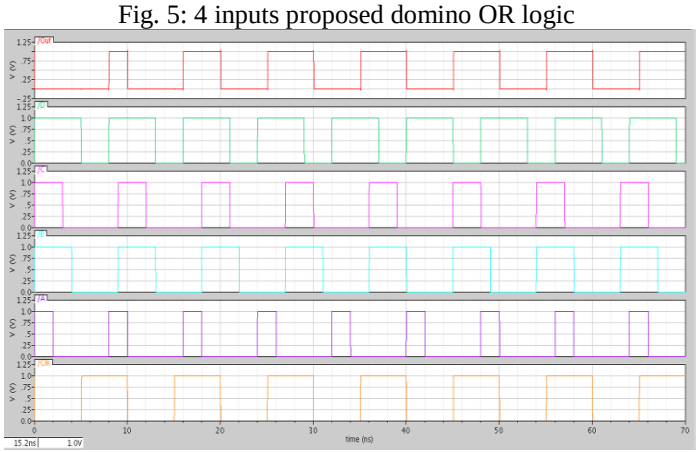

Fig. 6: Transient response of 4 inputs proposed domino OR logic

Table 1: Comparison of UNG

Fan in	UNG of standard Domino	UNG of conditional keeper Domino	UNG of proposed Domino
2	0.218	0.287	0.279
4	0.196	0.263	0.311
8	0.171	0.242	0.334
16	0.132	0.159	0.346

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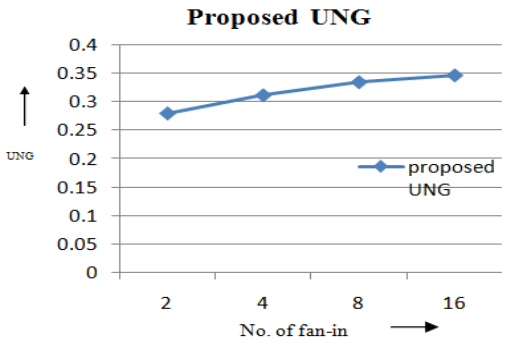

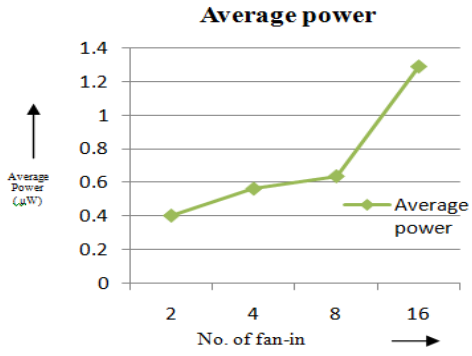

Fig. 7: UNG of the proposed circuit Fig. 8: Average power dissipation of the proposed circuit

[5] CONCLUSION AND FUTURE SCOPE

Domino logic dissipates very low standby power compare to static CMOS logic. In this paper the main objective was to improve the noise immunity and to reduce the average power consumed and delay associated with the circuit. The analysis shows that by proposed circuit it is possible to achieve an appreciable improvement in the noise margin and power consumption and marginal improvement in delay. The whole comparison is based upon 65 nm CMOS technology using Cadence Virtuoso tool at circuit level.

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