3.125 Gb/s Power Efficient Line Driver with 2-level Pre-emphasis and 2kV HBM ESD Protection

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Abstract

The paper presents a power efficient line driver for 3.125 Gb/s operation over FR-4 copper backplannes. The circuit has been implemented in 0.18μm and dissipates 28 mW from 1.8V power supply. Efficient ESD protection has been used that provided 2kV Human Body Model (HBM) reliability.

1. Introduction

High-speed I/O links are key technological elements that determine, to a large extent, the performance, physical footprint and power dissipation of many chip to chip communication schemes. Efficient, integrated circuit implementation of the high speed links is critical to the overall system. Due to modular nature of the communication hardware a typical hardware "box" consists of number of line cards and a dedicated backplane connection between them. A schematic representation of the backplane is shown in Fig.1.

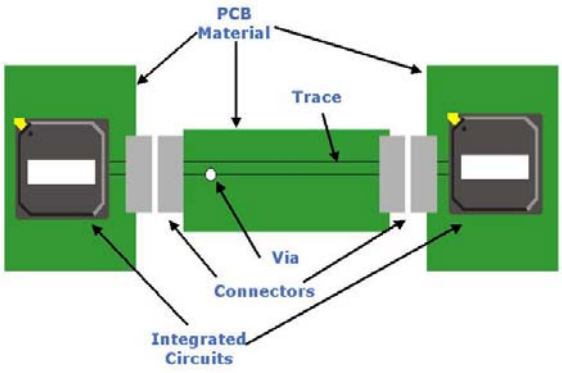

Figure 1 – Backplane connection.

When driving high-speed signals over the backplanes and long copper wires a special consideration must be paid to system impairments that reduce signal to noise ratio (SNR). The major contributors to signal deterioration in most backplane or cable transmission environments are channel loss, crosstalk and reflections.

Channel Loss is a phenomenon where the limited bandwidth of a given channel attenuates high-speed components of a data signal. This attenuation effect creates what is called Inter-Symbol Interference (ISI) which means signal smearing between two sequential bits. Attenuation is strongly dependent on the backplane material used as shown in Fig.2.

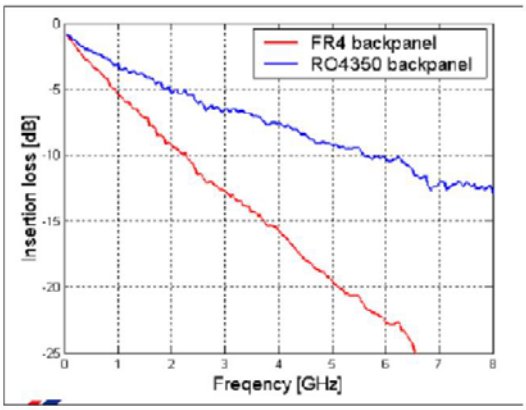

Figure 2 – Measured insertion loss (dB) vs. frequency (GHz) for two 50 cm backplanes.

Crosstalk occurs in any system with two or more conductors. Each wire segment acts individually as an inductor and capacitor, and also as an antenna. Together, they act as coupled antenna due to their mutual coupling. This coupling can be expressed in terms of capacitive and inductive components. Higher speed data transmission is detrimental to the crosstalk problem because coupling increase proportionally to the rate of change of the aggressor. The frequency domain transfer function of Near End Crosstalk (NEXT) and Far End Crosstalk (FEXT) indicate that a major contributor to crosstalk noise is NEXT.

Impedance discontinuities in the channel path is another system impairment that causes signal reflections, which in turn significantly deteriorate the SNR at the receiver. Any time there is a discontinuity in the signal's

propagation path, there is a certain amount of energy that is reflected back toward the source.

In order to deliver large increases in bandwidth over noisy, bandwidth limited channels, it is necessary to define an architecture that deals with signal impairments effectively. While many complex solutions are presented in the literature [1-5] we have developed a simple, pre-emphasis technique with much lower power dissipation compared to reported solutions. The developed circuitry can effectively provide up to 3.125 Gb/s of throughput over lossy and noisy channels over distance of over 50cm of the FR-4 backplane. 4 lanes at 3.125 Gb/s are sufficient to carry the data traffic for 10 Gb/s Ethernet and Fibre Channel applications using XAUI (extended attachment unit interface) as defined by IEEE 802.3ae specification.

2. Pre-emphasis

Pre-emphasis or equalization essentially means that high frequency components are boosted in such a way that the channel loss is compensated for. The term pre-emphasis is typically applied to the transmitting terminal, as implemented here, while the term equalization is used for the receiving end. A concept of the pre-emphasis implementation is shown in Fig. 3. The pre-emphasis is implemented by subtracting a scaled version of the delayed bit from the bit that is currently being transmitted. In the next section we will show how the pre-emphasis is implemented at the circuit level.

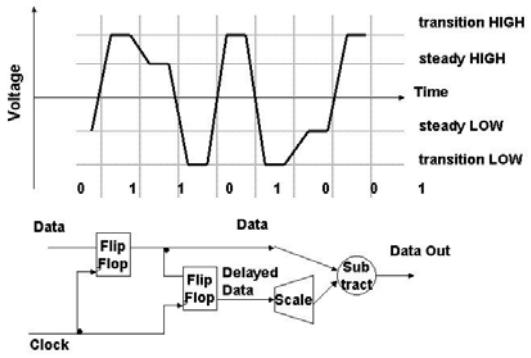

Figure 3 – Pre-emphasis concept and its architectural implementation.

3. Line Driver Circuit Implementation

A typical CMOS driver used for sending very high-speed data uses pseudo-ECL (PECL) structure shown in Fig.4. The tail current is steered by a differential pair N1, N2 either to the left or to the right branch. To achieve 1V peak to peak single ended output swing across 50Ω termination resistor 20mA current source is needed. For 1.8V power supply used in this work 20mA current consumption results in 36mW dissipated power that is largely independent of the switching frequency.

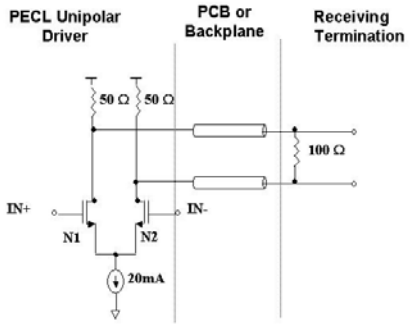

Figure 4 – Unipolar PECL driver.

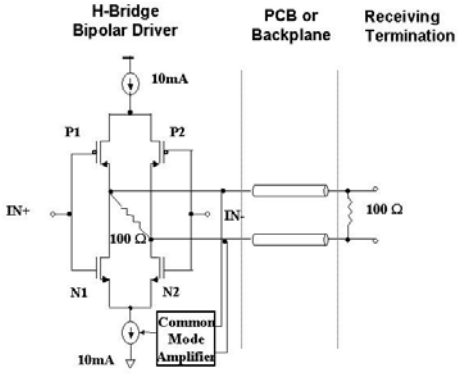

Figure 5 - Bipolar H-bridge driver used in this work.

We have implemented more power efficient solution that is of bipolar nature as it uses both n-channel (N1, N2) and p-channel (P1, P2) devices. This architecture uses two current sources at the top (head) and bottom (tail) with the common mode set up by a common mode amplifier. For the same output swing of 1V only 10mA current source is required resulting in the power dissipation of 18mW, half of the PECL driver from Fig.4. The H-bridge driver is therefore twice power efficient as the standard PECL driver.

To implement the pre-emphasis function two output driver stages are connected as shown in Fig.6. The left (with index 0) represents the current responsible for the output swing of teh current bit while the right (with index P) represents a scaled version of the previous bit. I_P is effectivelu subtracted from I_0. While we have

implemented only 2-level pre-emphasis an extension to more levels is straightforward.

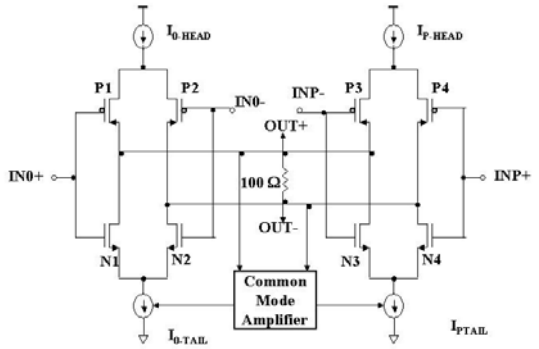

Figure 6 – Pre-emphasis implementation in the H-bridge driver used in this work.

One of the key challenges in design was making the output node to toggle at the frequency of 3.125 GHz as the same driver was used for both clock and data transmission. Through extensive simulation of the driver structure, parasitic components of the package and the entire backplane channel we have found that capacitive loading by the ESD protection devices and bonding pads are important to achieve 20ps rise/fall edges required by the design. In the next section we will show how low capacitive loading by the ESD structures was achieved while maintaining good ESD performance.

4. ESD Protection

Electrostatic Discharge (ESD) is generally recognized as an increasingly important issue for modern integrated circuits. Thinner gate oxides, complex SOC chips with multiple power supplies and mixed-signal blocks, larger chip capacitances and faster circuit operation all contribute to increased ESD-sensitivity of advanced semiconductor products.

Despite this importance it is remarkable that many research reports do not provide any information about ESD testing results or in some extreme cases no ESD protection devices are included on the chip, either for simplicity or to artificially enhance the performance.

To provide robust ESD performance while not degradating high-frequency performance an efficient ESD protection structure with low capacitive loading is required. The ESD circuitry used in this work is shown in Fig.7. It exploits a well known property of the snapback MOSFET operation: NMOS transistor enters the snapback mode earlier if its gate voltage is above the threshold voltage due to assisting function of the MOSFET that is parallel to bipolar npn [6].

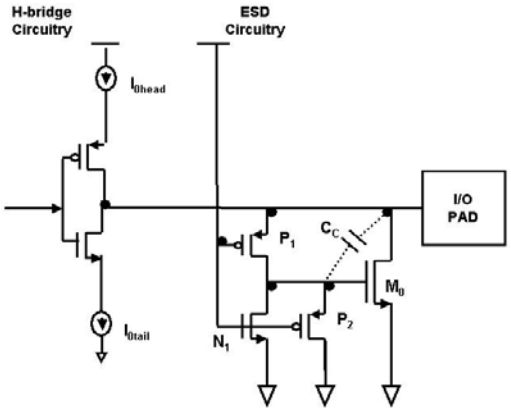

Figure 7 – ESD protection circuitry for the pre-emphasis line driver.

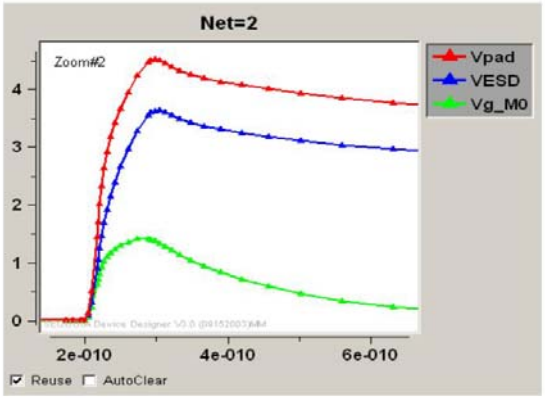

Figure 8 – Transient waveforms during 2kV HBM event simulated using SEQUOIA ESD simulator.

The ESD protection network shown in Fig.7 operates as follows [7]. During an ESD event, transistor N1 is off while transistors P1 and P2 are on providing a biasing path for the gate of the ESD NMOS to be charged as determined by relative sizing of P1 and P2. In this scheme the gate voltage of the ESD NMOS M0 follows the output voltage as shown in Fig.8. As a result during the ESD event the gate voltage of M0 increases above 1V helping in triggering the snapback of M0 and clamping the voltage at the I/O pad below 4.5V. A mixed-mode ESD simulation has been performed using a physical circuit simulation tool SEQUOIA ESD [8].

ESD NMOS has been laid out in a multiple finger configuration with a total effective width of 120µm and uses both ESD implant and silicide block to provide balancing resistance on its drain terminal. Due to

efficient ESD design the obtained capacitive loading of 0.28pF is smaller than typical loading levels of 0.5 to 1pF. The device passed 2kV Human Body Model (HBM) and 500V Charge Device Model (CDM) ESD testing.

5. Measured Performance Data

The XAUI line driver from Fig.6 with the ESD protection from Fig.7 has been implemented in a standard 0.18µm CMOS process. The entire driver occupies 0.14mm^2, uses 1.8V power supply and consumes 22mW of power. The power dissipation is very competitive compared to solutions reported in the literature and is half of the PECL driver implemented in the same 0.18µm process in our earlier work [9].

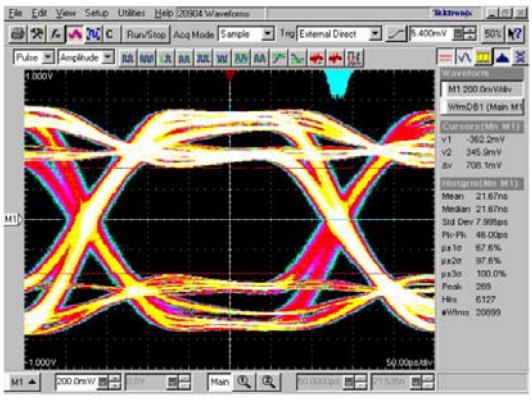

Figure 8 – Transmitting data eye pattern for PRBS-23 data pattern.

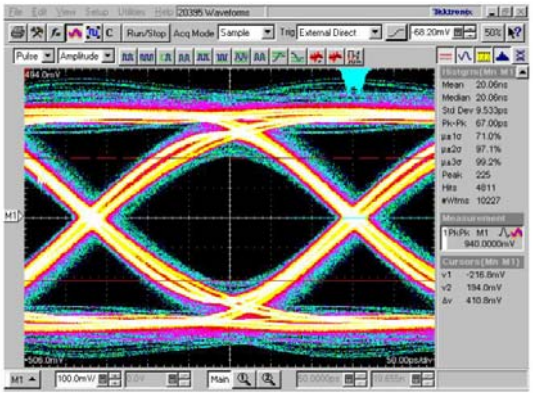

Figure 9 – Receiving data eye after 50cm of FR-4 backplane. Measured data for PRBS-23 pattern.

The driver has been tested in the backplane configuration shown in Fig.1 for backplanes widths up to 50cm. A pseudo-random bit sequence generator PRBS-23 has been used to generate random data patterns. A typical eye diagram at the transmitting end is shown in Fig.8 and after 50cm backplane in Fig.9. As can be seen the pre-emphasis circuitry has performed very well for this backplane channel. The transmitting data eye has peak to peak (p-p) jitter of 39ps while that of the receiving data eye of 68ps. The driver is compliant with XAUI IEEE 802.3ae specification with lower output swing for reduced power dissipation

6. Conclusions

We have designed a power efficient line driver with 2-STEP pre-emphasis for sending Gigabit per second (Gb/s) signals over backplanes and copper wires. The driver was implemented in 0.18µm CMOS process and is capable of data transmission up to 3.125 Gb/s. Its power dissipation of 22mW compares favourably against similar drivers presented in the literature. Due to efficient ESD protection structure the driver can sustain 2kV HBM ESD testing.

7. References

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