Front-End Receiver Architecture for Miniaturised Ultrasound Imaging

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Abstract - The design and measured results for an I/Q synthetic aperture beamforming front-end are presented. The system targets a highly portable ultrasound imaging applications such as wearable/portable devices and capsule endoscopes. Synthetic aperture beamforming is carried out in the baseband in order to minimise the bandwidth and power consumption. A single-channel analogue front-end (AFE) demodulates RF signals into I/Q components. The FPGA-based beamformer dynamically apodises and focuses the data by interpolating and applying complex phase rotations to the I/Q samples. The entire system is pipelined using a synthetic aperture protocol through a single, multiplexed channel in order to reduce the cost and complexity of the system and minimise the area. The AFE consumes 7.8mW and occupies 1.5 $mm \times$ 1.5 mm in AMS 0.35μm CMOS. The digital beamformer is implemented on a Kintex-7^{TM} FPGA and consumes $262mW$ for a frame rate of 4Hz. Measured results using real ultrasound data reveal that comparable image quality may be attained to the case when full RF beamforming is used. Future work includes integration of analogue/digital components on a single chip.

Keywords: analogue front-end, digital beamformer, FPGA, ultrasound imaging

1. Introduction

Point of care ultrasonography has been the focus of extensive research over the past few decades. Advances in transducer technology, beamforming algorithms and electronics have paved the way for the development of efficient, flexible and portable ultrasound imaging systems. Ultra-miniaturised, wireless systems have been proposed such as capsule endoscopes [1], implantable ultrasound devices [2] and wearable ultrasound devices [3]. However, the translation of these ideas into practical hardware is exceedingly difficult due to the inherent area, power and bandwidth constraints of such systems. This paper proposes a design for a front-end architecture that performs synthetic aperture beamforming (SAB) on demodulated I/Q signals. Extensive literature has been published on various SAB methods, their applicability in small-scale systems [4], and on the utility of beamforming in the baseband [5]. The primary focus of this paper is on the translation of theoretical I/Q SAB constructs into practical hardware, with the target applications being wearables, portable devices and capsule endoscopy. The proposed design combines SAB with I/Q demodulation to reduce the hardware complexity, cost and power consumption, at the expense of a lower frame rate. In section 2, the theoretical framework is discussed, followed by the design of the analogue front-end and digital beamformer in section 3. Finally, measured results are presented in section 4.

2. Baseband Synthetic Aperture Beamforming (SAB)

In this work, synthetic receiver aperture (SRA) [6] and synthetic transmit aperture (STA) [7] beamforming are combined by serialising the formation of both transmit and receive apertures, so as to maximise the SNR and reduce hardware complexity. A single element is excited to ensonify the region of interest. Transmission is carried out n times for all receive elements, and only a single receive channel is required to process the reflection signal. The result is n low-resolution images which are combined to form a higher resolution image. Spatial compounding is then used to increase the SNR: the entire process is repeated for Nt different transmit positions, such that the final image is an average of the higher resolution images. The obvious disadvantage of this approach is a reduced frame. However, hardware complexity is greatly reduced as only a single channel is required.

Beamforming is usually carried out in the RF domain. However, by demodulating the data first, the bandwidth and sampling rate may be decreased, leading to a substantial saving in power. I/Q demodulation is used to extract the in-phase

and quadrature components, I*(t)* and Q*(t),* from the reflected RF signal. Next, time delays for beamforming are calculated and linear or quadrature interpolation is used to determine the delayed I/Q values at the time delays. These values are then phase-rotated by multiplying the amplitudes by sine or cosine reference signals, and then summed to yield the pixel value. Dynamic apodisation is also applied to keep the F-number (*F#*) constant as a function of imaging depth. As described above, the low-resolution images are combined dynamically to form a high resolution image.

Table 1: Summary performance for the analogue front-end.

Parameter	Performance
Supply voltage	3.3 *V*
Static supply current	4.5 *mA*
Transducer center frequency	2.5 *MHz*
I/Q bandwidth	1.25MHz
Gain	(37 - 52) ± 6 *dB*
Input referred dynamic range at 1 *kHz*	61 *dB*
Input referred noise floor	15 *μV*

3. Hardware Design

The proposed system is comprised of an analogue front-end (AFE) and digital beamformer. A block diagram of the AFE is shown in Fig. 1. RF signals are switched through an analogue multiplexer, according to the SAB protocol described above. The first stage in the AFE is a fully differential preamplifier/low noise amplifier (LNA) which performs time-gain compensation (TGC) to account for exponential tissue attenuation. The signal is then downconverted using two passive mixers into I and Q components, and then amplified by a programmable gain amplifier (PGA) and filtered by a Butterworth lowpass filter. The layout of the AFE circuit is shown in Fig. 2, and a summary of the performance is presented in table 1.
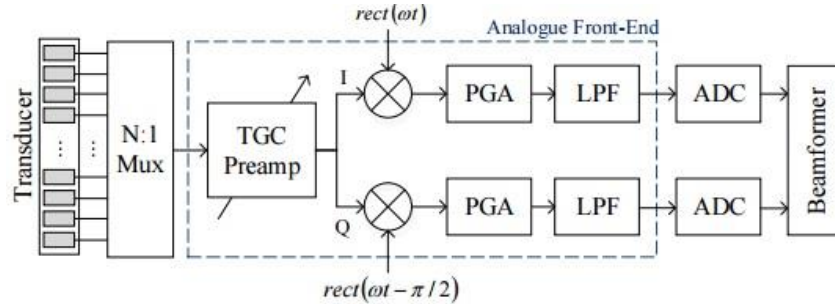

Fig. 1: Block diagram of the analogue front-end (AFE) and interfacing circuitry. RF ultrasound signals are multiplexed through the AFE, which performs time-gain compensation (TGC) and demodulates the RF signals into I/Q components using a switching mixer and lowpass filter (LPF). After analogue to digital conversion (ADC), I/Q data are processed by the digital beamformer to form a 2D image.

The Verilog beamforming algorithm was tested on a Kintex-7[TM] FPGA (XC7K325T-2FFG900CFPGA). A 62.7% device device utilisation is reported for the following parameters: f_{clk} = 20*MHz*, pixel resolution = 64 × 352, frame rate = 4 *Hz*. The total power consumption is estimated to be 262*mW* by the Xilinx Vivaldo power estimator. Increasing the clock frequency allows for a higher image quality/frame rate at the expense of increased power consumption.

4. Results and Discussion

Raw ultrasound data were captured on a Verasonics Vantage 256[TM] system using a P4-1 phased array (central frequency at 2.5*MHz*). The synthetic aperture method was used, and RF signals were sampled at 10*MHz*. The medium contained a hyperechoic phantom and had an attenuation rate of 0.7*dB*/*cm*/*MHz*. The RF signals were multiplexed through the AFE using an arbitrary waveform generator (Picoscope 5442B). Beamforming was carried out on FPGA and the image was transmitted to a PC. Finally, envelop detection was carried out in MATLAB and the image was

logarithmically compressed. In Fig. 3, B-mode images of the phantom are compared for RF-domain beamforming and quadrature beamforming. The normalised root-mean-square-error (NRMSE) may be used as a quantitative measure of image quality. The NRMSE is computed on a scan-line/columnwise basis by comparing each pixel in the RF-beamformed image, $g_{j,k}$ to that of the quadrature image, $f_{j,k}$, as follows:

$$NRMSE = \frac{1}{K} \sum_{k=1}^{K} \frac{\sqrt{\frac{1}{J} \sum_{j=1}^{J} \left(f_{j,k} - g_{j,k}\right)^2}}{max\left(g_{j,k}\right) - min\left(g_{j,k}\right)} \tag{1}$$
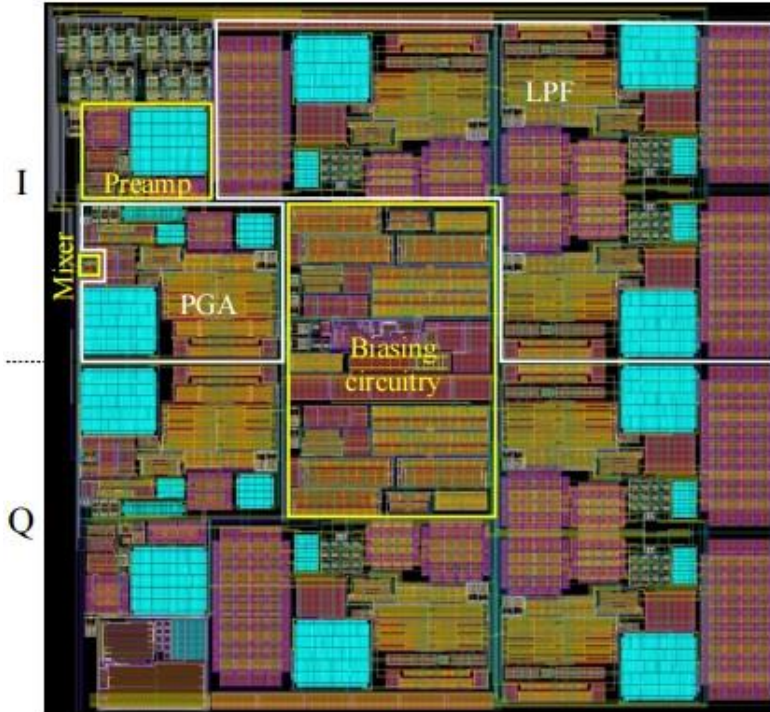

Fig. 2: Layout of the AFE in AMS 0.35μm CMOS technology. The dimensions of the AFE are 1.35mm × 1.35mm, and the power consumption is 7.8mW for a 3.3V power supply.

where max $(g_{j,k})$ and min $(g_{j,k})$ represent the maximum and minimum values of each column in $g_{j,k}$ respectively. For N_t = 48, the NRMSE is 13%, confirming that the two images are closely comparable. When decreasing the number of transmissions to 15, the NRMSE increases to 14.5% due to a reduction in the SNR caused by larger sidelobes and increased speckle noise. The reduction in image quality is evident in Fig. 3(c). However, for the same frame rate, a threefold reduction in N_t leads to a proportional decrease in power consumption, since the system clock frequency may be decreased or the area reduced as fewer pixels are calculated in parallel. The multidimensional tradeoff in the design must be balanced to achieve the desired image quality/frame rate, given the application. The proposed system consumes $269mW$ (excluding ADC and transceiver power consumption), and targets an application requiring low frame rates ($4Hz$). Other state-of-the-art beamforming solutions such as the ultrasound system-on-chip (SOC) in [8] support more advanced imaging techniques with high frames rates ($30\ f\ ps$), but at the expense of increased power consumption ($1.2W$) and area ($27\times27mm^2$). Alternatively, Memon *et al*. further miniaturised an ultrasound front-end by integrating a micromachined transducer with a beamforming ASIC for capsule endoscopy [9], but measured power consumption and image quality in this work are not published.
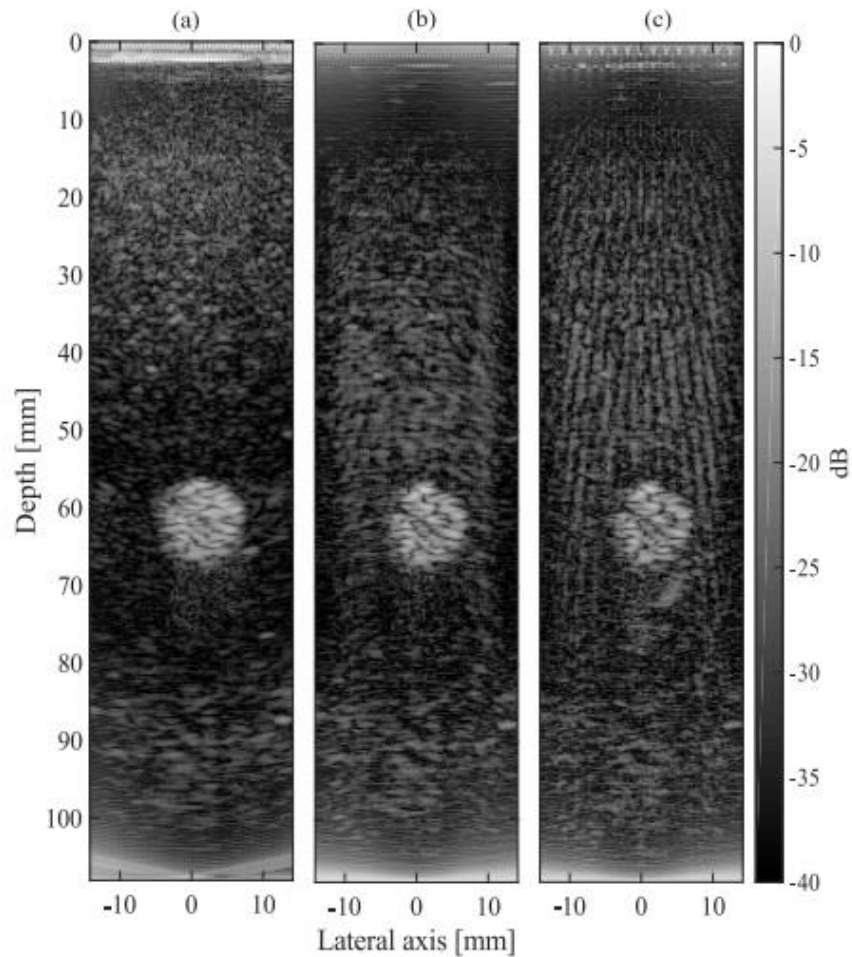
Fig. 3: Images of a phantom containing a hyperechoic cycst. In (a), beamforming is carried out in the RF domain with 48 transmissions and $F\# = 2.5$. In (b)-(c), quadrature beamforming is carried out with 48 and 15 transmissions respectively ($F\# = 2.5$).

5. Conclusion

The design of an integrated beamforming front-end for wireless capsule endoscopy is presented. The AFE demodulates RF ultrasound signals into I/Q components in order to decrease the bandwidth and power consumption. The AFE consumes $14.9mW$ and occupies $1.5mm \times 1.5mm$ in AMS $0.35\mu m$ CMOS when demodulating RF signals centered at $2.5MHz$. I/Q signals are multiplexed through a single channel, and dynamic focusing is carried out in the baseband using a synthetic aperture approach. The FPGA beamformer consumes $262mW$ for a frame rate of $4Hz$. The image quality and frame rate may be tuned by varying the degree of spatial compounding. Experiments using real ultrasound data reveal that the proposed front-end may achieve appropriate image quality, with reduced complexity and power consumption. Future work will involve integrating the analogue and digital subsystems into a single chip, and incorporating analogue-to-digital conversion, transmission and transceiver functions into the system.

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