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The Effect of Die Attach Voiding on the Thermal Resistance of Chip Level Packages

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ABSTRACT

During semiconductor manufacturing, voids are easily formed in the die attach bond layer and are found to form, grow and coalesce with thermal cycling. The presence of such voids is known to adversely affect the package thermal resistance, but to this point, not enough data exists to precisely analyze the effects of void size, configuration and depth. Using an innovative experimental method the present study investigates these effects with a carefully controlled void geometry. The results show that the thermal resistance increases linearly with void percentage for random voids, but increases exponentially for contiguous voids.

INTRODUCTION

The presence of voids in the die bond layer of semiconductor packaging is often the primary contributor to the overall thermal resistance of the packaged chip. Increased thermal resistance leads to increased device operating temperatures and reduced Mean Time to Failure (MTTF) [1] and possible catastrophic failure of the device. High throughput dispensing feeds and speeds [2], changes in deposit surface structure for stencil printing [3], and re-flow processing for lead-free solder joints [4] can all lead to void formation during manufacturing. Voids are also found to form, grow and coalesce with thermal cycling [5, 6] and thermal stressing [7] particularly for large chips [8].

Voids are typically categorized as small, randomly-distributed voids or large, contiguous voids [9, 10] and just as void formation is difficult to control, the type of void formed is also difficult to experimentally control. Previous experimental investigations have relied on the imaging and characterization of already existing void patterns through ultrasonic microscopy scanning techniques [2, 7, 11] or through photothermal interface microscopy [12]. In these studies, since the void geometry can not be precisely controlled, the effect of void geometry on thermal resistance can not be accurately determined.

While not precise, these studies do provide some insight into the effects of void configuration on package thermal resistance. For example, the data for small random voids suggests a roughly linear relationship of thermal resistance and void area, which becomes stronger with an increasing number of thermal cycles [7]. Voids which occur directly below the power source are found to increase device surface temperature increase from 10-16% for voids which cover up to 20% of the die attach area [5,6, 13] but that the junction temperature is proportional to the void area only if a package dependent coefficient is used [14].

To the author's knowledge, the only previous work which allows the control of the void geometry is that of Hu et al. [15] in which voids are simulated in the die bond layer using low conductivity spherical polymer inclusions. This technique allows the control of the void size, but not void location. In

addition, the void size is limited to that of the polymer particles, 200 µm

Although these studies shed light on the relationship between package thermal resistance and voids in the die bond layer, not enough data exist to analyze the exact effects of void size, configuration and depth on the package thermal resistance. A tight control of the void characteristics should permit a more precise study of the relationship between void geometry and thermal resistance. The present study allows the experimental investigation of these effects in carefully controlled void geometry using an innovative experimental method. The results are expected to significantly enhance the ability of the packaging engineer to evaluate the effects of die bond resistance on the thermal response of the entire package.

In this experiment, the voids are etched to a depth of 0.0127 cm (5 mils) directly into the backside of the silicon chip, rather than being created in the die bond layer itself. By using a carefully controlled bonding process, the only voids between the silicon chip and the die bond layer are those precisely etched in the chip in a particular geometric pattern. A complementary numerical study is completed to show that the voids located in the chip backside have an effect on the package thermal resistance which is equivalent to that of voids located in the die bond layer. The technique presented in this paper allows the study of the effects of void configuration (contiguous versus random), void size, void location and void percentage ($V_{\%}$) on thermal resistance. This data will provide the basis for an accurate representation of void geometry effects on thermal resistance, providing guidelines for the development of die bond processes and in improving the overall reliability of the packaged device.

EXPERIMENTAL CONFIGURATION AND ANALYSIS

A schematic of a cross-sectional center slice of the experimental package configuration is shown in Figure 1. A void pattern is etched to a depth of 0.0127 cm (5 mils) into the backside of a 0.60 cm by 0.62 cm by 0.038 cm thick silicon chip and resistors are fabricated on the front side of the wafer using NiCr thin film deposition and photolithography. Each chip is mounted onto a 1.8 x 1.8 cm by 0.159 cm thick beryllia (BeO) substrate using 0.005 cm (2 mils) of solder paste. The beryllia substrate is soldered onto a 2.54 x 2.54 cm by 0.238 cm thick nickel-plated cold-rolled steel TO-3 package. The package is mounted on a black, anodized aluminum heat sink.

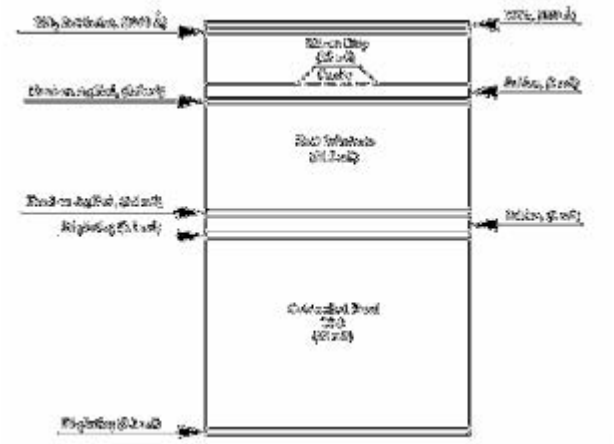

Figure 1: Cross-Sectional Schematic of Package

The void geometry is varied in type (random or contiguous), in size, and in void percentage, $V_{\%}$ (fraction of the interface that is occupied by voids). Contiguous voids take the form of one large, square, centrally-located void and "random" voids are modeled as a 5 x 5 matrix of evenly spaced square voids with the same total void area as the contiguous voids. A control chip is fabricated with no voids. The void pattern geometry is listed in Table 1.

Each photomask design yields 8 dice of each geometric pattern from Table 1, except pattern C0 which is formed without the backside void mask. The wafers are diced into individual chips of size 0.60 cm by 0.62 cm using automatic sawing equipment. For most experiments, a constant power of 7.5 watts is applied to the package and steady-state is achieved in about 10 minutes. The void patterns are illustrated in Figure 2.

Pattern Name	Pattern Type	Void Side Length (cm)	# Voids	Total Void Area (cm^2)	$V_{\%}$
C0	Control	0	0	0	0
C1	Contiguous	0.262	1	.0686	18.5
R1	Random	0.053	25	.0702	18.9
C2	Contiguous	0.371	1	.138	37
R2	Random	0.0737	25	0.136	36.6
C3	Contiguous	0.452	1	.204	55
R3	Random	0.091	25	0.207	55.7
C4	Contiguous	0.523	1	0.274	73.6
R4	Random	0.104	25	0.270	72.8

Table 1: Void Patterns

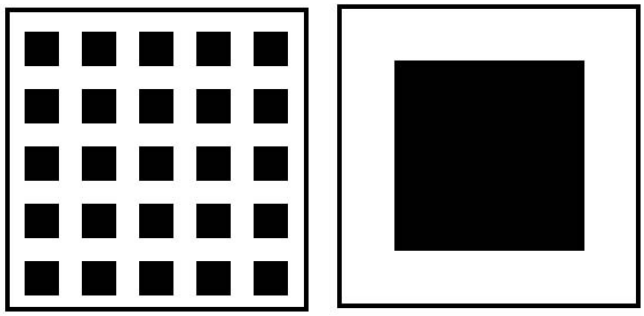

Figure 2: Void patterns R2 (left) and C2 (right)

The surface temperature and temperature distribution of the package are monitored using thermal imaging with a spatial resolution of 15 microns and a temperature resolution of 0.1°C. The thermal resistance between the heat source (the resistor) and the package is determined by $q_{jc} = (T_j - T_c)/P$, where T_j is the junction temperature, T_c is the case temperature measured at the package bottom using type T thermocouples, and P is the applied power computed using measured resistance and current values. The junction temperature of the device is determined using the average temperature from the thermal image within a 0.109 cm x 0.109 cm area in the center of the chip. This size is slightly larger than the largest random void size.

NUMERICAL MODEL DEVELOPMENT

An experimentally validated numerical model is used to confirm that the voids located in the chip backside have an effect on the package thermal resistance which is equivalent to that of voids located in the die bond layer. A ¼ symmetry model of the package is developed using the IcePak 4.1 CFD software package. The layers used in the model development are shown in Table 2 with their thermal conductivies. The voids are modeled as trapped air pockets. The computational domain consists of 46,255 nodes and the results are checked for grid independence by comparison to a model with 77,376 nodes.

Material	Thermal Conductivity (W/mK)
Silicon Oxide Chip Coating	1.29
N-Type Silicon Chip	70 (doped silicon properties)
Void	0.0261 (air)
Solder Layer 2 (80Pb-20Sn)	37
Fired on Silver Pad	427
BeO Substrate	260 at T=273 K (temp dependent curve used)
Fired on Silver Pad	427
Solder layer 1 (80Pb-20Sn)	37
Nickel plating	91.7
Cold Rolled Steel T0-3 package	46

Table 2: Thermal Model Layers from Bottom to Top

The analysis is double-precision, non-linear, steady-state, with the power modeled as a volumetric heat generation occurring in the occurring in the coating layers on the top of the chip, simulating the NiCr thin film resistors. The boundary conditions on the top and side surfaces are natural convection and radiation to the surroundings at 291 K but the primary mode of heat transfer in this case is conduction to the anodized aluminum heat sink. The dominance of conduction results from the relatively high level of thermal resistance from the die-to-ambient for natural convection and radiation as compared to the die-to-heat sink thermal resistance.

The boundary condition at the bottom of the package is approximated as a constant temperature boundary where the temperature is that of the anodized aluminum heat sink, T_c. This approximation is valid in this case because the heat source is relatively far from the heat sink and the heat is uniformly distributed when it reaches the heat sink. Additionally the package is smaller than the heat sink resulting in a small contact area between the package and the heat sink and a thus only a small thermal gradient across the contact area.

The initial set of models replicates the experimental conditions in order to validate the model. In this case, the heat sink temperature is chosen to match the recorded heat sink temperature, T_c, from the experimental runs, which varies from 22 to 42 °C depending on the case. In later models, the conditions are standardized to T_c = 25 °C.

The initial models replicate the geometry of the experimental package for validification purposes while later models vary the geometry in order to verify that the voids located in the chip backside have an effect on the package thermal resistance which is equivalent to that of voids located in the die bond layer.

In the experimental validification models, the silicon chip has voids of 0.0127 cm depth patterned in the chip backside and is bonded to the package with solder 0.005 cm thick. In this case, the void has greater depth than the solder layer, so it is not possible to numerically replicate an identical void in the solder layer to gauge the thermal effects of void location. Therefore, for the second set of models, the solder layer is increased to 0.0127 cm thickness and a void of 0.0127 cm depth is modeled first in the chip and then in the solder. This void model reflects a void of similar depth in each case for comparison. However, in this case, the void in the solder layer is a through-void, with the void depth equal to that of the solder depth. The void in the chip is not a through-void, so the behavior may not be equivalent. Therefore, for completeness, a third set of geometric models reflects a 0.038 cm thick chip with a 0.038 cm thick solder layer. A 0.0127 cm deep void is modeled first in the chip and then in the solder. This void model reflects a void of similar depth and similar style in each case for comparison.

RESULTS AND DISCUSSION

Experimental Results: Effects of Applied Power, Void Style and Void Percentage

The initial studies focus on the effects of applied power to determine any power specific results. The void pattern remains the same while the applied power is varied from 5 to 9 watts. Two different void patterns are considered, one contiguous and one random (R3 and C3). The results are shown in Table 3. For the random void pattern (R3), the thermal resistance varies less than 5% over the power range. For the contiguous void pattern, the thermal resistance is higher than for the random configuration at the same power level, but again varies only 5-7% as power level increases from 5 -9 W. As the effects of applied power are small, a constant applied power value of 7.5 W is selected for the remaining studies.

Package	Applied power (watts)	T_{jc}
R3	4.97	1.84
R3	6.21	1.93
R3	7.52	1.94
R3	8.90	1.93
C3	5.03	3.40
C3	6.26	3.24
C3	7.50	3.15
C3	8.87	3.25

Table 3: Effect of Applied Power on Thermal Resistance

Once the effect of power level is shown to be small, the effects of void pattern on the thermal resistance of the package are investigated. Power level remains constant at 7.5 W and the void pattern is changed to each of the 8 void patterns detailed in Table 1. The results can be seen in Figure 3. It is clear that increasing the void percentage increases the thermal resistance. When void percentage is below 20% as studied previously [5,6,13], the increase in thermal resistance is small for both the random and contiguous void patterns. But, as $V_{\%}$ increases past the previously studied regime, a distinct difference in thermal behavior can be seen for the random and contiguous void patterns. The thermal resistance of the random void patterns continues to increase almost linearly to a maximum increase of 30% with 73% voids, and is well-correlated by $q_{jc} = 0.007V_{\%} + 1.499$. However, for the contiguous void pattern, the same void percentage leads to a much higher increase in thermal resistance of 200% to a final value of 4.7 °C/W and is well-correlated by an exponential fit: $q_{jc} = 1.43e^{0.154V_{\%}}$.

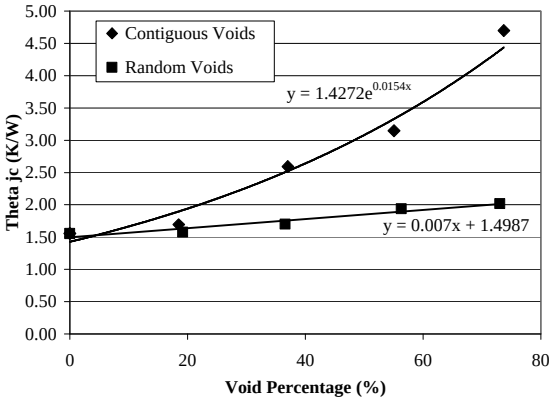

Figure 3: Variation of Thermal Resistance with Void Percentage

The difference in the thermal resistance behavior for random and contiguous void patterns can be qualitatively explained through the effects of spreading resistance and the effect of the thermal conductivity of silicon on the overall thermal resistance. Thermal resistance in the silicon chip above the void area is primarily comprised of two components: axial resistance from the heat generating source above the void, $?_v$, and a lateral spreading resistance from the region above the void to the surrounding non-voided areas, $?_L$. For chips with voids in the die attach area, spreading resistance becomes dominant as the heat is forced to flow laterally in the chip around the void region. The high thermal resistance through the void itself hinders heat flow in the axial direction. For equivalent void percentage, lateral spreading resistance increases more for contiguous type voids because at any point above a contiguous void the length of the heat flow path to a nonvoided area is longer than in random void configurations.

Figure 4 shows a map of surface temperature for a random and a contiguous void pattern of similar void percentage. The underlying void pattern can be easily distinguished as it is qualitatively reproduced in the surface temperature contours. This temperature distribution is similar to that described as a "hot void" by Carlson et al. [16] in which the heat flow is restricted to the non-void areas, creating a hot spot above each void.

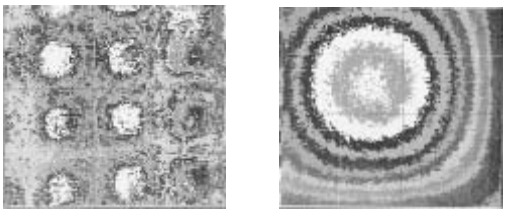

Figure 4: Image of chip surface temperature distributions for random and contiguous void percentage of 56%.

Table 4 shows that the junction temperature increases significantly with void percentage and again, the rise is higher for contiguous voids than for random voids due to the higher spreading resistance. For the 20% contiguous void configuration, the junction temperature increases 13.7%, which corresponds well to the previously observed 10-16% [5, 6, 13] for this void percentage validating the results.

Void Pattern	dT (Case To Chip)	% Increase From No Voids
C0	11.7	- - -
C1	13.3	14%
C2	19.6	67%
C3	23.6	102%
C4	35.5	203%
R1	11.8	0.8%
R2	12.7	8.5%
R3	14.6	25%
R4	15	28%

Table 4: Effect of Void Percentage on Junction Temperature Rise

Numerical Model: Effects of Void Location

The numerical model is used to verify that the voids patterned in the chip backside have an effect on the package thermal resistance which is equivalent to that of voids located in the die bond layer. The numerical model is first validated against the experimental data with the voids modeled in the chip backside, replicating the experimental conditions. Figure 5 shows that the model data, scaled to include the effects of interfacial resistance, matches the experimental data and the numerical model is validated.

The effect of void location is studied by modeling patterned voids in the chip backside in accordance with the experimental analysis and then modeling the same package with an identical void now located in the solder layer. As discussed in the numerical model development, this is done first for a 0.038 cm chip, 0.0127 cm solder layer and 0.0127 void creating a through solder void, and then repeated for a 0.038 cm chip, 0.038 cm solder layer and 0.0127 cm void creating an encapsulated solder void.

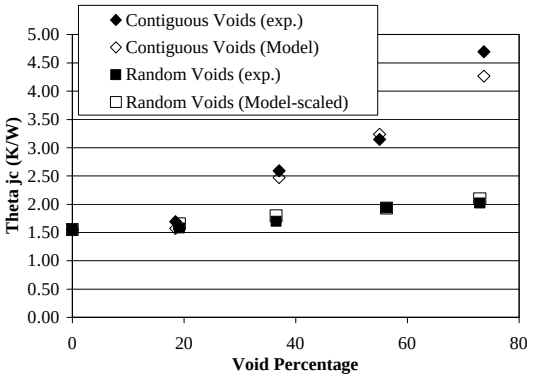

Figure 5: Numerical Model Validification

Figure 6 shows the case of the solder through-void. This graph shows the raw model output, uncorrected for interstitial resistance in the random void case. However, the slope of the relationship for the random void case will be similar when corrected for interstitial resistance, just slightly offset from the model results. It can be seen that moving the void location from the chip backside to the solder from the chip has an effect on $?_{jc}$ for the contiguous voids, but not for the random voids. $?_{jc}$ is higher for contiguous voids when the void is patterned in the chip. The same effect can be seen in Fig. 7 for the encapsulated void case.

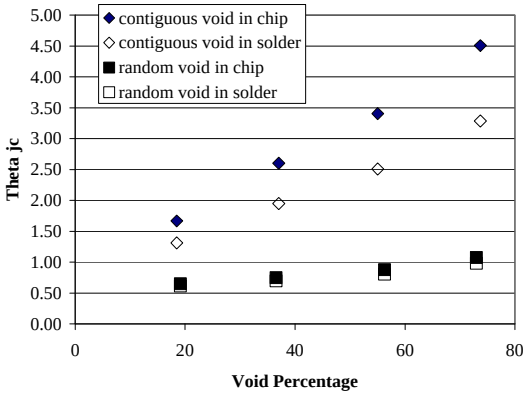

Figure 6: Effect of Void Location, Solder Through-Void

The discrepancy results from the different thermal conductivities in the chip and solder layers. The thermal conductivity of the chip is greater than that of the solder, so placing the void in the chip replaces a high thermal conductivity region with an extremely low thermal conductivity void. The effect on thermal resistance is not as great when the lower conductivity solder layer is replaced with a low conductivity void. However, the bands created by the two data sets for the void in the chip and the void in the solder represent the highest and lowest possible values of $?_{jc}$ with the actual $?_{jc}$ for any physical situation falling in between these two bands. The slight overprediction of $?_{jc}$ by the patterning in the chip backside is a small price to pay for the precise creation of void geometry allowing a much greater in-depth understanding of the effects of die bond voiding on package thermal response as seen in Fig. 3.

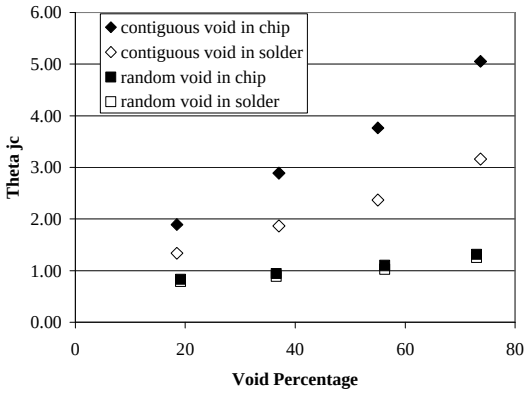

Figure 7: Effect of Void Location, Solder Encapsulated Void

CONCLUSIONS

This study permits the tight control of the void style and geometry to allow a precise investigation of the relationship between void geometry and package $?_{jc}$. Voids are patterned in the backside of a chip and the resulting package is studied in detail. It is seen that the package $?_{jc}$ increases as the void percentage increases. For random voids, the thermal resistance increases linearly with void percentage up to a maximum of 30% at 73% voiding, but significantly, package $?_{jc}$ increases exponentially for contiguous voids, reaching a 200% increase for 73% voiding. The void type also exerts a strong influence on the behavior of the chip surface temperature as the underlying void pattern is qualitatively reproduced in the surface temperature contours. The increase in junction temperature rise for 20% void percentage contiguous void is 13.7%, which corresponds well to previously reported results. As void percentage continues to increase, the junction temperature rise reaches as high as a 200% increase from the zero void case.

The numerical model is well validated by the experimental results. The model verifies that experimentally patterning the void geometry in the chip backside is an appropriate way to simulate die-bond voiding while precisely controlling the void characteristics. These results are expected to significantly enhance the ability of the packaging engineer to create more realistic models which accurately reflect the effects of die bond resistance on the thermal response of the package.

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