

Innovation to Overcome Limitations of Test Equipment

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Abstract

In this contribution, we describe current developments in the Automatic Test Equipment (ATE) industry with respect to the hardware and software. For testing mixed-signal interface devices, such as Digital-to-Analog and Analog-to-Digital Converters (DACs and ADCs) the standard test setups are examined. In particular, limitations are identified that lead to exponentially increasing test time for high-resolution converters. Examples of innovative approaches to keep this test cost increase at bay are outlined.

1. Introduction

Purely relying on ATE suppliers to provide test equipment that outperforms the devices which are tested is not sustainable. For digital circuit testing, this realization has led to a paradigm shift from functional test to fault-oriented test. The core of this shift is the realization that the task of test is not to prove functionality, but to identify excessive performance degradation caused by on-chip error sources, such as unintended shorts and opens.

Following this paradigm shift, innovative approaches of Design-for-Test (DfT) and Built-in Self Test (BiST) were developed. The essence of these approaches is to enable device measurements that ease the observation of the on-chip error sources. These developments have eased the strain put on the ATE.

For mixed-signal devices, a similar development is required. However, it is clear that testing for unintended shorts and opens is insufficient as error sources of more subtle nature already lead to device performance degradations which need to be screened out by test.

One of the major difficulties in analog and mixed-signal (AMS) test is to provide high-quality test signals and to capture the device response accurately. The development of ATE is reviewed in Sec. 2, establishing the trends

in hard- and software to address these difficulties and highlighting the limits of these developments.

The example of testing data converters is representative for the difficulties manufacturers are facing. In Sec. 3, we review the standard test configurations for DAC and ADC testing, highlighting the difficulties and opportunities that come with the industry trend towards multi-site testing.

In Sec. 4, the concept of model-based testing is outlined; describing it as a paradigm shift from full functional test to error source oriented test. With this shift, we highlight the opportunities in DfT used in conjunction with the model-based test approach to overcome ATE limitations such as measurement noise which otherwise leads to test times growing exponentially with converter resolution.

Error source oriented test is to be distinguished from structural test. The latter attempts to break up the circuit into structural elements whose functionality is established individually. Error source oriented test evaluates error sources, e.g. the mismatch between two structural elements, and tests for violation of the high-level device functionality requirements, i.e. specifications, as a result of the effect of all error sources combined.

2. ATE developments

The current trend in digital ATE development is towards massive parallel test. The number of DUT-sites tested in parallel is growing from 64 in 2003 to 256 in 2010 as shown in Table 1 which is extracted from [4, Tab. 22a]. Massive parallel test is becoming particularly pervasive for digital test applications with DfT and BiST which typically require eight clock and power supply sources being available at a test site.

As multi-site testing significantly reduces the cost of test for digital circuits, the pressure to reduce the cost of test for analog and RF circuits is increasing—in particular for SoC applications. Current analog and RF test methods are based on full functional test. Parallelizing such tests would require multiple data source and capture resources; conse-

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quently, the number of sites tested in parallel lacks behind digital ATE as shown in Tab. 1.

Especially for SoC applications, there is a major drive for DfT and BiST developments for analog/ mixed-signal and RF devices. If this aim can be fulfilled, the ITRS projects that even AMS/RF device test can benefit from massive parallel test of up to 256 sites in the long-term.

2.1. Electronics

Key parameters for the ATE electronics are channel bandwidth, noise-floor and clock jitter. These parameters are projected by the ITRS to develop for ATE instruments as shown in Tab. 2

In the seven years between 2003 and 2010, the source bandwidth doubles for both low- and high-frequency analog instrumentation. However, the noise-floor numbers of the low-frequency analog instruments are approaching physical limits and are, therefore, expected to level off at $-165 \text{ dB}/\sqrt{\text{Hz}}$. Note that the high-frequency sources need to catch up with the low-frequency sources in terms of noise performance. Requirements for digital clock sources will also become more stringent reaching 0.1 ps rms-jitter in 2010.

2.2. Software and DSP

Major developments of the ATE software interface include:

- Software tools for test development which are independent of a specific ATE platform;
- Circuit simulations (including the DUT, DIB and ATE instruments) are used to verify test programs before silicon;
- DSP comes as part of instrumentation, e.g. FFT computation in the capture instrument reducing the load on the ATE processor for multi-site testing.

3. Mixed-signal interface test

3.1. Standard DAC and ADC test

The standard DAC test setup, shown in Fig. 1, uses a Device Interface Board (DIB) which customizes the ATE platform to the requirements of the Device Under Test (DUT). The setup shown allows one to stimulate the DUT by loading an input code c and to measure its response, the DAC

	2003	2005	2010	Remark
#(sites)	64	128	256	digital
	4	8	16	AMS/RF
Clocks & PSU	8	8	8	per site

Table 1. Multi-site test capability of ATE as projected by ITRS in 2003.

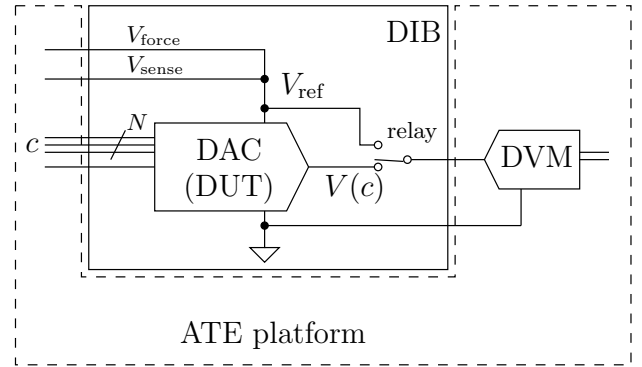


Figure 1. Standard production setup for testing an N -bit DAC.

output voltage V_{out} , using the digital voltmeter (DVM) of the ATE.

With the setup shown, typical DAC specifications, such as offset error, gain error, Differential and Integral Nonlinearity (INL and DNL) can be determined [1]. Typically, the INL/DNL test is most time-consuming as this test requires one to measure the output voltage for each of the 2^N input codes for an N -bit DAC.

Multi-site testing, i.e. accommodating multiple DUTs on the same DIB requires multiple power/reference voltage supplies and multiple DVMs. In most ATEs, the number of DVMs is limited; only one or two high-resolution meters are available. In this case, multiple DAC outputs can be multiplexed by on-DIB relays to the limited number of DVM resources.

In such a scenario, multi-site testing is beneficial only when the portion of device test time consumed by DAC linearity test is small, e.g. in an SoC application. An example is a video encoder [7], for which a large portion of the device test is dedicated to testing the digital core that implements the Digital Signal Processing (DSP) needed to facilitate a variety of video signal formats.

Carrying out the digital test for multiple devices in parallel will increase the pressure to reduce the analog portion of the device test which cannot be parallelized due to the limited number of DVMs available citeMMWK+04:ICTW.

Specification	2003	2005	2010	Remark
Bandwidth (MHz)	30	50	60	low-frequ.
Noise ($\text{dB}/\sqrt{\text{Hz}}$)	-155	-155	-165	analog src
Bandwidth (GHz)	1.2	1.5	3.0	high-frequ.
Noise ($\text{dB}/\sqrt{\text{Hz}}$)	-135	-135	-155	analog src
Clock jitter (rms)	0.5 ps	0.2 ps	0.1 ps	

Table 2. Projected requirements for specifications of analog and digital sources on mixed-signal ATE [4, Tab. 29a].

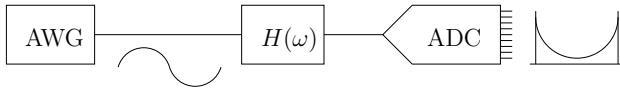


Figure 2. Standard ADC test setup: the Arbitrary Waveform Generator (AWG) provides the ADC stimulus and the digital outputs are captured and post-processed by the ATE.

The standard ADC test setup, shown in Fig. 2, provides the ADC under test with sinewave input, produced by an Arbitrary Waveform Generator (AWG). The digital response of the ADC to the input is captured by the ATE.

Typically, an active filter stage $H(\omega)$ is used to condition the stimulus signal before it is passed to the ADC input. Signal conditioning is often required to accommodate the load that the DUT represents; a switched capacitor ADC input, for example, draws significant current spikes which a general purpose AWG cannot handle without severe signal distortions.

The output codes of the ADC are post-processed by the ATE. As depicted in Fig. 2, the number of times each code is output by ADC can be counted to form a histogram from which the INL and DNL performance can be deduced at every code [3] and can be compared against the test limits on INL and DNL.

Multi-site testing is rarely limited by the amount of digital capture resources; but rather by the ability to fan-out the sinewave signal. In the previously mentioned case of a switched-capacitor ADC input, the current spikes generated at the sampling instant can propagate to other on-DIB circuitry, e.g. through the ground plane. Thus, when multiple test sites sample the sinewave at the same time, such effects can limit the number of ADCs that can be tested in parallel.

The ITRS [4] highlights as an “Important Area of Concern” for mixed-signal testing:

“The analog/RF/microwave signal environment seriously complicates load board design and test methodology. Noise, crosstalk, signal mixing, load board design,... will dominate the test development process and schedule.”

For the particular case of the SC-ADC, where one conversion cycle is broken up into twenty clock cycles [12], the sampling instances of twenty devices to be tested in parallel can be staggered up—leaving sufficient time for the crosstalk signals to die out. With this innovative approach the difficulty of crosstalk suppression is moved from DIB design to writing the test program which has to handle the ADC outputs becoming available at twenty different time slots; however, twenty ADCs are measured in effectively the same time as previously a single ADC.

3.2. Impact of increasing DUT resolution

Testing for a specification, such as INL of a data converter, should be based on a performance measurement with a resolution of 10% of the specification limit.

DAC testing. In order to test an N -bit DAC for linearity specifications of ± 1 LSB, the DVM shown in Fig. 1 should have at least $N + 4$ -bits of resolution. A DVM, such as the Agilent 3458A with $8\frac{1}{2}$ digits or 28-bit of resolution is, therefore, adequate to test high-resolution DACs.

Let us assume that a 10-bit DAC is tested based on measuring its output voltage at all $2^{10} = 1024$ codes. The repeatability of each voltage measurement is 0.05 LSBrms for an aperture time setting of 20 μ s for the DVM. This entails an all-codes measurement time of $20 \mu\text{s} \times 1024 = 20.48$ ms, which can be considered acceptable.

For a 12-bit DAC, the number of codes quadruples, and in order to achieve 0.05 LSBrms repeatability (which in absolute voltage terms is four times lower!), the aperture time needs to be increased by a factor of $16 = 4^2$. Thus, the all-codes measurement time increases by a factor of sixty-four to 1.3 s, a trend which starts to raise serious concerns in a production test environment.

Continuing this trend to a 16-bit DAC, the measurement time would increase to ninety minutes, which is clearly unacceptable. In order to cap this trend, manufacturing test resorts to *short-codes* techniques, such as “Major Carry Testing [1].” Instead of testing the linearity specification at all-codes, the INL and DNL is measured only at converter mid-scale, quarter-scale,... down to the LSB. For a 16-bit converter, operating sixteen binary weights, only 32 measurements of the DAC output voltage are required for this test.

While such a test approach obviously reduces test time, the coverage of this test is questionable and highly dependent on the converter architecture. An example of short-codes testing is mentioned in [5]. In this industry example, test time was reduced from twenty-two minutes for an all-codes measurement to thirty seconds. In this reported example, the aperture time for the DVM measurement was set to 20 ms, indicating that the manufacturer had selected 1500 codes in order to achieve sufficient test coverage.

ADC testing. The setup shown in Fig. 2 yields an all-codes measurement of the ADC’s INL characteristic. Test time is determined by the ADC’s conversion cycle time times the number of conversions required for a test.

With increasing increasing resolution of the ADC under test, the conversion cycle time typically increases. The number of conversions required to achieved a target repeatability of the INL/DNL measurement can be determined as described in the IEEE Standard 1241. The formulas in [3] suggest that for increasing the resolution by one bit, the number of conversions required quadruple. Thus, we are fac-

ing a similar trend of exponentially increasing test times for ADCs as described above for DACs.

Short-codes testing for ADCs is not as straightforward as it is for DACs, unless an alternative measurement setup is used [6].

4. Overcoming limitations

4.1. Selecting test conditions

The standard approach to testing mixed-signal interfaces is based on full-functional test, i.e. testing that the DUT functions in each mode of operation as specified. This is an impossible test target to attain, and in fact, only a subset of the specified modes of operation is ever tested in production.

For example, device operation is typically specified over a range of ambient temperatures and a range of supply voltages. In production test, it is often only feasible to test at one ambient temperature and one setting of the supply voltage. Selecting the test condition used in production can be viewed as adding information to the test such as “if a device passes the selected test with performance better than a test limit l_{test} the device is unlikely to fail the specification limit l_{spec} over all specified operating conditions.”

The difference $l_{\text{test}} - l_{\text{spec}}$ is referred to as guardband. Using guardbands in this manner enables the manufacturer to trade-off test costs and test quality [9].

The procedure of selecting the test condition and test limit exploits the fact that the device architecture contains a set of error sources which determine performance for the selected test condition and for the range of operating conditions specified on the data sheet.

Let us use a finer grain for the term “mode of operation.” For the example of DACs, each input code can be viewed as a mode of operation. With this view, the “short-codes” test referred to in Sec. 3.1 is simply an extension of the above mentioned selection of a test condition: the error sources, which determine the INL/DNL performance of the DAC at the selected subset of codes and over all-codes, are the same; thus, a performance test at the selected set of codes (with appropriate guardbanding) can guarantee that the DAC meets performance specifications over all-codes.

For this approach to test cost reduction to work, we need to establish that the selected test (condition) exercises all the error sources which contribute to device performance degradations over the range of specified modes of operation, including all-codes, all supplies and all temperatures. If one of these error sources is not exercised under the selected test condition, this error source can lead to the DUT being passed but failing to meet data sheet specifications, i.e. lead to a test escape, irrespective of the guardbands.

4.2. DAC short-codes test

While testing all possible error sources seems a difficult task in its general formulation, model-based testing is a paradigm which was first suggested for streamlining DAC short-codes testing in the early eighties by researchers at the National Institute of Standards and Technology (NIST) [8]. At the core of this strategy, a model is built that characterizes the relationship between the performance degradation exhibited over all modes of operation and the error sources associated with the device architecture.

Model-based principle. For an N -bit DAC, let us denote the INL measured at all-codes by a vector $b \in \mathbb{R}^{2^N}$. This INL characteristic is the sum of contributions from various on-chip error sources, such as circuit element mismatches. Since there is a finite number of error sources (due to the fact that there is a finite number of circuit elements) one can represent each error source by a model characteristic.

For convenience, let us write these model characteristics as columns of a matrix A with 2^N rows. Then, the device characteristic can be decomposed into a weighted sum of model characteristics by solving the linear system of equations

$$b = Ax, \quad (1)$$

where the vector $x \in \mathbb{R}^n$ represents the weights.

The aim of INL testing is to establish that the worst-case INL value, i.e. $\|b\|_\infty$ is less than a prescribed specification limit l_{spec} . In the paradigm of model-based testing, one can avoid measuring b by determining the model weight vector x . Typically, the number of elements in the vector b is much larger than the number n of elements in the vector x . Theoretically, one would only need to select n equations of the system (1), thus, measure only the corresponding elements of b in order to determine a unique set of weights x .

Once the elements of x are determined, one can predict the all-codes INL characteristic as $\hat{b} = Ax$ and perform a test of

$$\|\hat{b}\|_\infty < l_{\text{test}} \quad (2)$$

where l_{test} denotes the test limit, which is smaller than l_{spec} in order to guardband for measurement noise influences and model inaccuracies. Such nonidealities lead to $\|\hat{b} - b\|_\infty$ being non-zero which is termed the model’s prediction error.

Short-codes test application. For the example of an 11-bit DAC, model-based testing has been implemented in a production test environment [7]. Instead of measuring the INL of the DAC at $2^{11} = 2048$, the production test is based on measuring 72 codes. The prediction error has been shown to be less than 0.15 LSB which can be guardbanded for by tightening the specification limit of 3 LSB accordingly.

For the example of a 16-bit DAC, a model-based short-codes test approach is reported in [2]. Instead of measuring all 65,536 codes, the model requires one to measure the INL

at only 120 codes. Yet, the prediction error which needs to be guardbanded for is less than 0.1 LSB.

This indicates that the benefit of short-codes testing is the larger the higher the resolution of the device under test. Thus, model-based short-codes DAC testing allows manufacturers to address effectively the trend (highlighted in Sec. 3.1) of exponentially-increasing test times for high-resolution DACs.

4.3. Model-based ADC test

As highlighted in Sec. 3.1, testing ADCs using the sinewave histogramming method does not lend itself to a short-codes test approach. However, considering the model-based test approach, which solves a linear set of equations (1) in the least-squares sense in order to estimate the model weight vector x , an opportunity arises of suppressing the influence of measurement noise by exploiting the properties of the least-squares solution.

In [10], a 12-bit ADC is considered. A production type measurement of the all-codes INL characteristic requires guardbanding for the measurement noise-induced error of 0.26 LSB. Using the model-based approach, the guardband can be reduced to 0.064 LSB. This reduction of the measurement noise influence becomes vital when testing a higher-resolution version of the ADC used as a test vehicle.

In Sec. 3.1, we indicated that when using the same test setup, increasing the converter resolution by two bits entails that sixteen-times more samples need to be converted in order to reduce the noise-induced measurement error by a factor of four, i.e. scaling it with the reduction in LSB size. In the above example, model-based testing achieves a reduction of the noise influence by a factor of $\frac{0.26}{0.064} = 4.06$. Thus, model-based testing the 14-bit ADC requires no more conversion cycles than the standard approach to testing the 12-bit ADC. The ability of the model to reduce the influence of measurement noise primarily depends on the measurements taken to estimate the model weight vector x . In [11], a DfT-feature is evaluated which applied to segmented charge-redistribution ADCs. A reconfiguration of the digital control logic enables measurements of the ADC from which the model weight vector can be estimated. The number of conversion cycles is the same as in the above example, but the noise reduction factor increases to seventeen, instead of four when using the model-based test approach without the added DfT feature. With this improvement, model-based testing a 16-bit ADC can be achieved in the same test time as testing a 12-bit ADC using the standard histogram method.

5. Conclusions

The rate at which ATE performance enhances over time is too low for continuing the brute-force test method of functional testing AMS devices, such as data converters.

We have presented the error source oriented test approach of model-based testing in order to overcome ATE limitations such as measurement noise. Within this approach, the goal of Design-for-Test is to ease error source identification. Results suggest that this approach can significantly reduce test costs, as for example a 16-bit ADC can be tested in the same test time using the same test setup as a 12-bit ADC using the traditional method.

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