Domino Gate with Modified Voltage Keeper

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Abstract

Using both the modified supply voltage and body voltage, an optimized keeper technique is presented in this paper to tradeoff the performance of domino OR gates. The simulation results show that the novel technique can highly improve power/speed efficiency and robustness to noise. In addition, because of employment of body biased voltage, the optimized keeper technique enables to minimize effect of the strong process parameter variation.

1. Introduction

As a common logic in high speed-performance chip design, high fan-in domino OR circuits or like structures are commonly employed in register and cache array bit lines design to achieve simple and fast structures [1]. However, robustness is a major inherent concern for domino OR gates because the parallel evaluation transistors in a domino OR gate could leak charge from the evaluation node easily [2-4].

Conventionally, the robustness of a standard OR domino gate can be improved by a weak keeper, with little performance penalty. However, as the technology scales down below 65 nm node, the scaling of threshold voltage (V_{th}) and gate oxide thickness (t_{ox}) results in exponential increase of leakage current and thus keepers must be upsized to offset the worst-case leakage through the pull-down network, which reduces the performance advantage of dynamic gates over other circuit structure. Also, continued device scaling makes the robustness problem worse due to the increase in cross-talk noise between adjacent wires [5]. Furthermore, the increasing process variations[6], which are introduced during chip device fabrication steps, also have a significant effect on the robustness of high fan-in OR domino circuits.

Therefore, there exist the need to investigate effective techniques to improve the robustness of high fan-in OR domino gates. An effective forward body biased keeper circuit technique is proposed in [2] for enhanced robustness of domino logic, but it suffers form the speed and power consumption overhead. Considering the stacking effect of NMOS transistors, an alternative domino design technique is proposed in [3] to achieve a great improvement in performance and noise immunity, but this technique leads to considerable penalty of power consumption. Diode-Footed Domino in [4] exhibits considerable improvement in robust to noise as compared to the standard domino circuits, but this technique, as well as other techniques mentioned above, fails to consider the robustness to parameter variations and therefore they could not solve the robustness problem completely.

There is, therefore, a tradeoff between high power/speed efficient operation and robustness to noise and parameter variation exists in high fan-in domino OR logic. In this paper, we propose a novel robustness aware high fan-in OR domino design for improving overall performance effectively.

2. Proposed high fan-in domino gates

Fig.1 shows the conventional domino OR structure and the proposed domino OR circuit, respectively. In the proposed design, the low supply voltage keeper technique (LSK) and the low body voltage keeper technique (LBK) are applied, where $V_{ddL}<V_{dd}$ and $V_b<V_{ddL}$.

A.. Low supply voltage keeper technique (LSK)

LSK provides two significant benefits over conventional domino OR gates. First, as indicated in Equation (1), both switching and leakage components of power consumption have a super-linear relation to supply voltage (V_{dd}), so lowering V_{dd} can reduce the total power consumption effectively. Second, LSK could reduces the contention current provided by the keeper to charge the evaluation node while the pull-down NMOS network is attempting to discharge the evaluation node, which provides significant improvement of the delay time compared to the conventional domino logic. Therefore, from the high-speed/energy efficient operation perspective, V_{ddL} should be set as small as possible.

$$P = P_{switching} + P_{leak} = \alpha f C_L V_{dd} V_{swing} + I_{leak} V_{dd} \quad (1)$$

where α, f, and I_{leak} are switching activity factor, clock frequency and leakage current of the dynamic node of the gate, respectively. C_L is the capacitive load at the evaluation node.

However, these significant benefits, comes at the cost of the degradation of noise immunity, which results in two problems. On the one hand, in the evaluation phase, if the inputs are all low, the high logic of evaluation node must be maintained by the keeper. But the keeper with LSK would have inferior strength to maintain the logic and therefore it may cause logic swing at the output. So too low supply voltage of the keeper would induce the logic error. On the other hand, even if V_{ddL} is large enough to maintain the output swing within acceptable level, the power consumption may be actually increased due to the charging and discharging of the evaluation node during the unnecessary logic swing, as can be seen from Fig.2.

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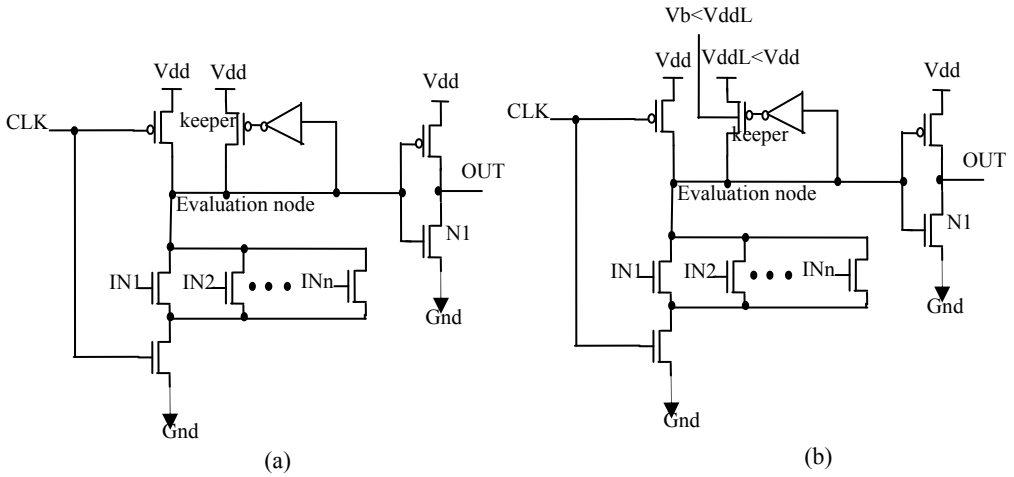

Fig. 1. N-input OR domino gates. (a) standard OR dominos (b) proposed OR dominos

B. Low body voltage keeper technique (LBK)

To improve the degraded noise immunity induced by LSK, LBK is applied to our design. As V_b decreases below V_{dd}, Vth of the keeper will be reduced (Equation (2) [7]), increasing the contention current as compared to a zero body biased keeper with the same physical dimensions. Keeper with low body voltage, therefore, improves the noise immunity characteristics as compared to conventional domino logic with the same keeper physical size. However, contrary to LSK, LBK would increase the contention current due to the low Vth, thereby increasing both the power consumption and delay time of a domino OR gate.

$$V_{th} = V_{th0} + \gamma(\sqrt{|-2\phi_F + V_{sb}|} - \sqrt{|-2\phi_F|}) \qquad (2)$$

where Vth0 is the threshold voltage when Vsb=0, γis the body effect coefficient, 2ψF is the silicon surface potential at the onset of strong inversion, Vsb is the source to body voltage.

From the analysis above, we can see that utilizing LSK in conjunction with LBK (LSBK) has the potential to improve the overall performance of high fan-in OR domino gates by (1) first reducing supply voltage of keeper to improve the power and speed characteristics and (2) then applying LBK to enhance the robustness to noise.

Furthermore, LSBK can compensate for parameter variations. In this scheme, V_b is lowered below VddL, therefore the keeper is forward body biased, known as FBB. FBB has the desirable result of reduction in Vth roll-off and DIBL, thereby reducing sensitivity to critical-dimension variation.

In next part, we investigate the effectiveness of LSK, LBK and LSBK for improving overall performance of high fan-in OR domino gates.

3. Simulation results

To evaluate the effectiveness of the proposed technique, delay, power consumption, noise immunity and robustness to parameter variations are measured for the new proposed 16-input domino OR gate and is compared with the conventional OR domino gate. Each domino gate drives a capacitive load of 8fF. HSPICE simulation results were obtained for CMOS 45nm BSIM4 models [8] with the power supply of 0.8V. The simulations were performed at 110°C where power consumption, delay, and noise immunity are all more critical than at low temperatures. All OR gates were turned to operate at 1GHZ clock frequency and the keeper to pull-down network equivalent transistor width radio (KPR) [9] is two for all circuits.

The noise immunity is defined as the signal amplitude at the inputs the induced a 10%-V_{dd} drop in the voltage at the output of domino OR gate. The noise signal is assumed to be a wave with 500 ps duration and 80% duty cycle [7].

A. Effectiveness of LSK

Fig. 2 shows the waveform of output for 16-input domino OR gate varies as a function of the supply voltage of keeper. In our simulation, we assume the logic margin is 10%-V_{dd} at the domino output; that is, as long as the logic swing at the output is below 80mV, the output will be reliable. It can be seen that, to keep the logic reliable, V_{ddL} must be large than 0.5V. The effectiveness of LSK in improving the power consumption and speed characteristics is shown in Fig. 3. It shows that the delay time is reduced with the decreasing of V_{ddL}. Especially, as the V_{ddL} decreases from 0.8V to 0.7V, the delay time could be reduced quickly. As also can be seen from Fig. 3, when V_{ddL} achieves 0.7V, due to the unnecessary logic swing, the power consumption will actually increase with the decreasing of V_{ddL}. To achieve low power and high speed design, therefore, the minimum V_{ddL} in our design is 0.7V. However, when V_{ddL} varies from 0.8V to 0.7V, the noise immunity will degrade greatly, as shown in Fig.4 (a).

B. Effectiveness of LBK

Table 1 lists simulation results of 16-input domino OR gate with LBK, which shows that there is obvious power and delay penalty when V_b is reduced. However, the noise immunity is enhanced with the decreasing of V_b, as shown in Fig 4 (b). It also can be seen that when V_b achieves 0.2V and

continues to decrease, the noise immunity will not be further improved. This is because when V_b is below 0.2V, the keeper will the forward biased strongly and produce enough drain-to-body diode current to oppose the drain current of the keeper, thereby lowering the voltage of the evaluation node and ending enhancement of noise immunity as well [2].

Based on the simulation results, we can conclude that LSK can be applied in conjunction with LBK to improve the overall performance of high fan-in OR domino gates.

C. Proposed domino OR gate with LSBK

To better investigate the tradeoff among the power consumption, delay time and noise immunity, we define the overall performance (OP) of OR dominos as

$$OP = \frac{Power * Delay}{Noise\_immunity} = \frac{PDP}{Noise\_immunity} \qquad (3)$$

Obviously, when OP value is minimized, the circuits would achieve optimal overall performance. We simulate the OP value of 16-input domino OR gate with LSBK by varying V_{ddL} from 0.7V to 0.8V and V_b from 0.1V to 0.8V. The results are shown in Fig 5 and the optimal condition (V_{ddL}=0.74V and V_b=0.6V) with minimum OP value is obtained. As also can be seen from Fig 5, as V_b is less than 0.2V, OP value will increase greatly with the decreasing of Vb. This is because the significant decreasing noise immunity (Fig 4(b)) is the decisive factor as compared to the power consumption and delay time.

Also, we analyze the robustness of the proposed design to process variations. In the experiment, 1000 Monte Carlo simulations are done to evaluate the impact of variations in the most important parameters gate length (L_{gate}), channel doping concentration (N_{ch}), and t_{ox} and each parameter is assumed to follow a Gaussian statistical distributions, with a three sigma (3 σ) variation of 10% [10-11].

Fig.6 shows the power-delay product (PDP) distribution curves of 16-input domino OR gates with conventional technique and proposed technique, which indicates that the proposed technique is preferable to reduce PDP in majority of the samples under process parameter fluctuations, which is similar to the analysis at the normal corner.

TABLE 1

Vb /V	0.1	0.2	0.3	0.4
Power/ W	4.78e-03	8.29e-04	7.78e-05	3.14e-05
Delay/S	4.73e-10	4.94e-10	4.98e-10	4.94e-10
Vb /V	0.5	0.6	0.7	0.8
Power/ W	2.88e-05	3.02e-05	2.98e-05	2.94e-05
Delay/S	4.87e-10	4.97e-10	4.92e-10	4.86e-10

SIMULATION RESULTS OF 16-INPUT DOMINO OR GATE WITH LBK

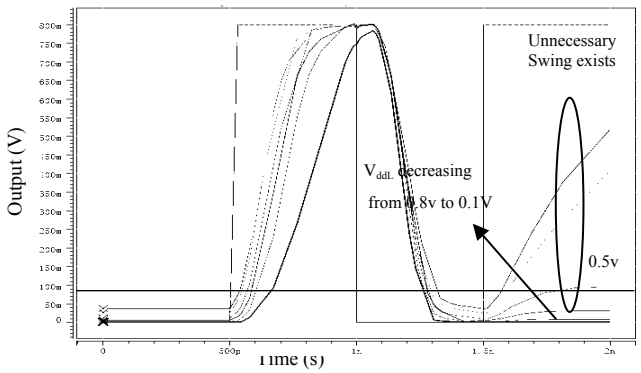

Fig. 2. Transient output of 16-input domino gate with LSK

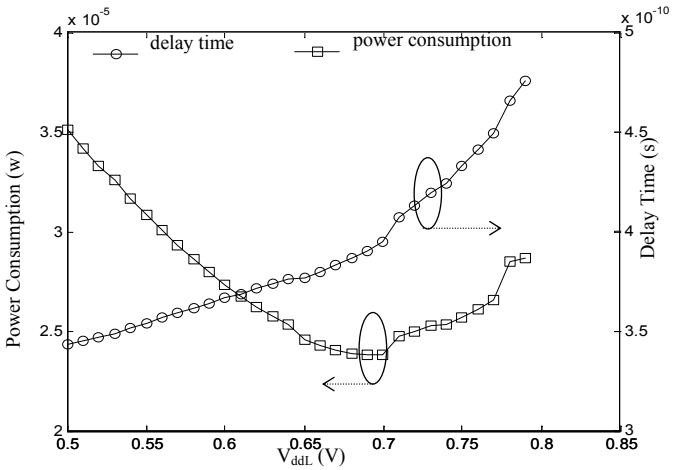

Fig. 3. Power and delay of a 16-input OR gate with LSK

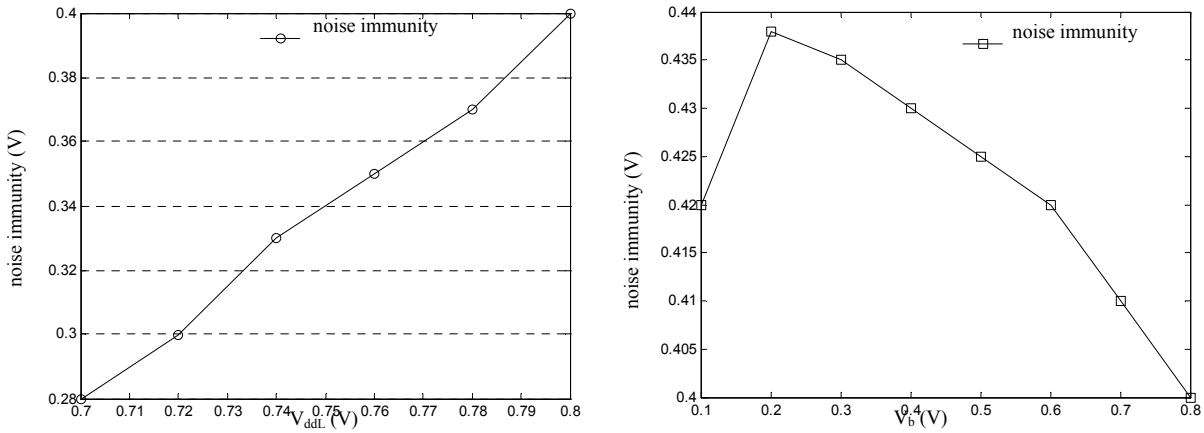

Fig. 4. Noise immunity of a 16-input OR gate (a) with LSK (b) with LBK

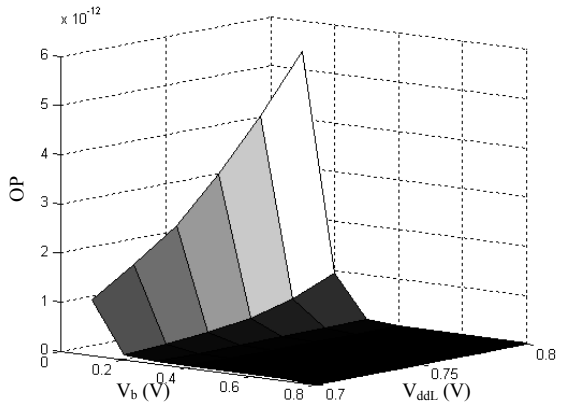

Fig.5. OP value of 16-input domino OR gate with LSBK

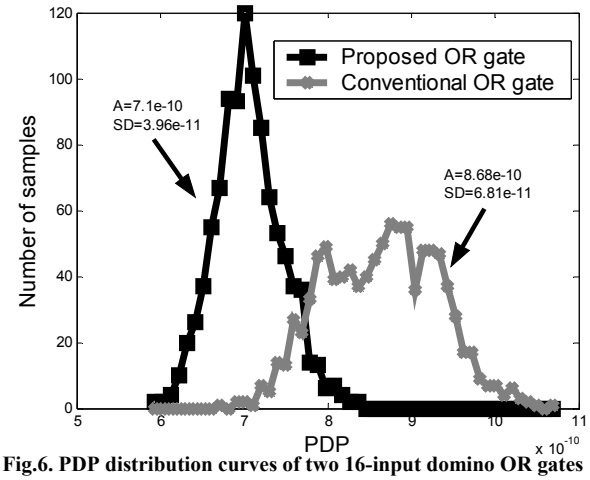

Fig.6. PDP distribution curves of two 16-input domino OR gates

To evaluate the impact of the process variation on PDP of proposed 16-input domino OR gate and conventional 16-input domino OR gate, we compare the parameter uncertainty (SD/A) [12] and it shows that the uncertainty of PDP for proposed OR gate (SD/A=3.96e-11/7.1e-10=0.056) is much less than the uncertainty of PDP for conventional gate (SD/A=6.81e-11/8.68e-10=0.078), as shown in Fig. 6. Therefore, the proposed domino OR gate is more robust to parameter variation as compared to conventional OR gate.

4. Conclusion

Design tradeoffs of power consumption, speed and robustness exist in high fan-in OR domino gates. In this paper, a novel design combining the low supply voltage keeper technique and the low body voltage keeper is proposed to address this dilemma. Simulation results show that the proposed technique can improve the overall performance and the high fan-in domino OR logic is taken to a new level of high-speed, low-power and robust operation. Thus, high fan-in domino OR logic may still be employed in the deep submicron technologies where robustness to noise and process variations is becoming an increasingly limiting issue. The significant improvement, however, comes at the cost of additional complexity as multiple supply voltage and bias generators are necessary, as well as a more complex algorithm for determining the optimum set of supply voltage and bias voltage of keeper.

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