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FPGA BASED DESIGN & IMPLEMENTATION OF ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING TRANSCEIVER MODULE USING VHDL

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ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels that are then allocated to users. However, OFDM uses the spectrum much more efficiently by spacing the channels much closer together. This is achieved by making all the carriers orthogonal to one another, preventing interference between the closely spaced carriers. The OFDM modem developed in this work consists of development of serial to parallel converter, 4-QAM modulator, IFFT logic which is built using 64 point radix-4 butterfly structure, FFT logic, 4-QAM de-modulator, and parallel-to-serial converter. The OFDM modem core is simulated by considering 31 sub-carriers. The whole design has been implemented using Xilinx Spartan-3AN XC3S700AN FPGA. The FFT/IFFT module that has been implemented makes use of CORDIC algorithms as an alternate for multipliers. This makes better usage of FPGA resources and the performance is more due to the usage of CORDIC algorithms instead of multipliers.

Keywords: OFDM, QAM modulator, FFT/IFFT, CORDIC

I. INTRODUCTION

Nowadays, the wireless telecommunication technology has become very advanced. It encompasses various types of fixed, mobile, and portable two-way radios, cellular telephones, personal digital assistants and wireless networking. The OFDM component is present in different kinds of wireless equipments which include Wireless LAN modems, 3G Cellular systems, Digital Video Broadcast systems, ADSL modems, etc. OFDM is a special form of Multi Carrier Modulation

and the OFDM time domain waveforms are chosen such that mutual orthogonality is ensured even though sub-carrier spectra may over-lap. With respect to OFDM, it can be stated that orthogonality is an implication of a definite and fixed relationship between all carriers in the collection. It means that each carrier is positioned such that it occurs at the zero energy frequency point of all other carriers. The sinc function, illustrated in Fig. 1 exhibits this property and it is used as a carrier in an OFDM system. The OFDM core consists of both OFDM transmitter and OFDM receiver logic implemented together on a single FPGA. The OFDM core has been tested by considering the loop-back mode, that is, the IFFT outputs of the transmitter are taken as inputs to the FFT in the receiver module.

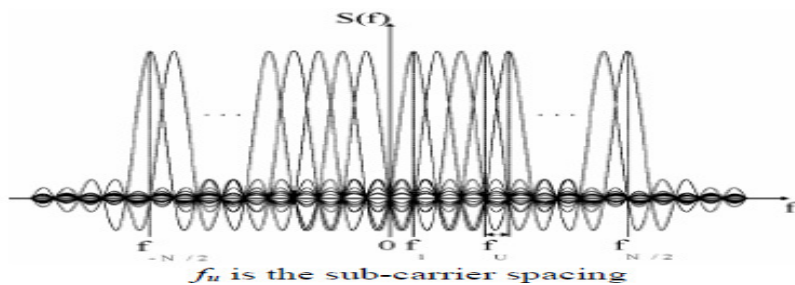


Fig. 1 The sinc function

II. LITERATURE REVIEW

Nasreen Mev and Brig. R.M. Khaire ^[1] proposed Orthogonal Frequency Division Multiplexing (OFDM) transmitter and receiver design using Quartus II tool and Simulation have been carried out using Altera Modelsim simulation tool. By using channel coding & decoding methods and error detection & correction methods synthesis and analysis has been done and how exactly OFDM system works, is verified.

Rajesh S. Bansode, Dr. B. K. Mishra and Aqsa M. Temrikar ^[2] proposed the design and implementation of OFDM system along with SLM implementation to reduce PAPR and a detailed simulation of the OFDM system with 16-QAM. OFDM transceiver is implemented using FPGA Spartan6 kit. The hardware results show a detailed study of RTL schematics and Test Bench. In this paper, the software simulation results show 2dB reduction in the peaks.

Ahmed Saeed, M. Elbably, G. Abdelfadeel, and M. I. Eladawy ^[3] explain the implementation of radix-22 single-path delay feedback pipelined FFT/IFFT processor. This attractive architecture has the same multiplicative complexity as radix-4 algorithm, but retains the simple butterfly structure of radix-2 algorithm. The implementation was made on a Field Programmable Gate Array (FPGA) because it can achieve higher computing speed than digital signal processors, and also can achieve cost effectively ASIC-like performance with lower development time, and risks. The processor has been developed using hardware description language VHDL on an Xilinx xc5vsx35t and simulated up to 465MHz and exhibited execution time of 0.135 μ S for transformation length 256-point.

M.Santhi and G.Lakshminarayanan ^[4] presented paper; a novel scheme is proposed which comprises the advantages of asynchronous pipelining techniques and the advantages of FPGAs for implementing 200Mbps MB-OFDM UWB transmitter digital backend modules. In asynchronous pipelined system, registers are used as in synchronous system. But they are controlled by handshaking signals. Since FPGAs are rich in registers, design and implementation of asynchronous pipelined MBOFDM UWB transmitter on FPGA using four-phase bundled-data protocol is considered in this paper.

Nirav J. Chauhan et al. [5] developed FFT processor for some particular OFDM application. In order to achieve this goal, several steps need to be followed. The first step is to find the Specifications for this FFT processor, which is determined on the basis of the application for which the FFT processor is to be designed. After defining the specifications, optimized FFT algorithm and architecture should be used for these specifications. There are a large number of FFT algorithms and architectures in the signal processing literature. Therefore, the state of art algorithms and architectures should be analyzed and compared. Based on different algorithms and architectures, different power consumptions, area and speed of the processor will be achieved.

Manjunath Lakkannavar and Ashwini Desai [6] focused on the core processing block of an OFDM system, which are the Fast Fourier Transform (FFT) block and the Inverse Fast Fourier Transform (IFFT). The work also includes in designing a mapping module, serial to parallel and parallel to serial converter module. The 8 points IFFT / FFT decimation-in-frequency (DIF) with radix-2 algorithm is analyzed in detail to produce a solution that is suitable for FPGA implementation. The FPGA implementation of the project is performed using Very High Speed Integrated Circuit (VHSIC) Hardware Descriptive Language (VHDL).

III. THE PROPOSED SYSTEM

The OFDM modem can be fully implemented in digital form. The OFDM Modem including the OFDM transmitter and OFDM receiver can be integrated into a single FPGA. As shown in figure 2, there is a need for blocks of 2-port RAMs for the implementation of the FFT, so Xilinx Spartan-3AN FPGA was chosen, as they contains the features required. More specifically, we used the Spartan 3AN FPGA XC3S700AN as the device. Description of each block is as follows.

1) **The Constellation Encoder & Decoder:** The constellation encoder maps m_n bits of the channel at a point in $a_n + j b_n$ constellation of the modulator. The decoder receives this point and remaps as m_n bits which are transmitted. That the encoder input are binary numbers of m_n bits, and generates the two binary numbers as outputs, 1 binary number is in one phase, and another is in quadrature, whose sizes are defined by the IFFT. It is therefore necessary to define a threshold for the decision that can be made about the particular point in this constellation that represents the received signal.

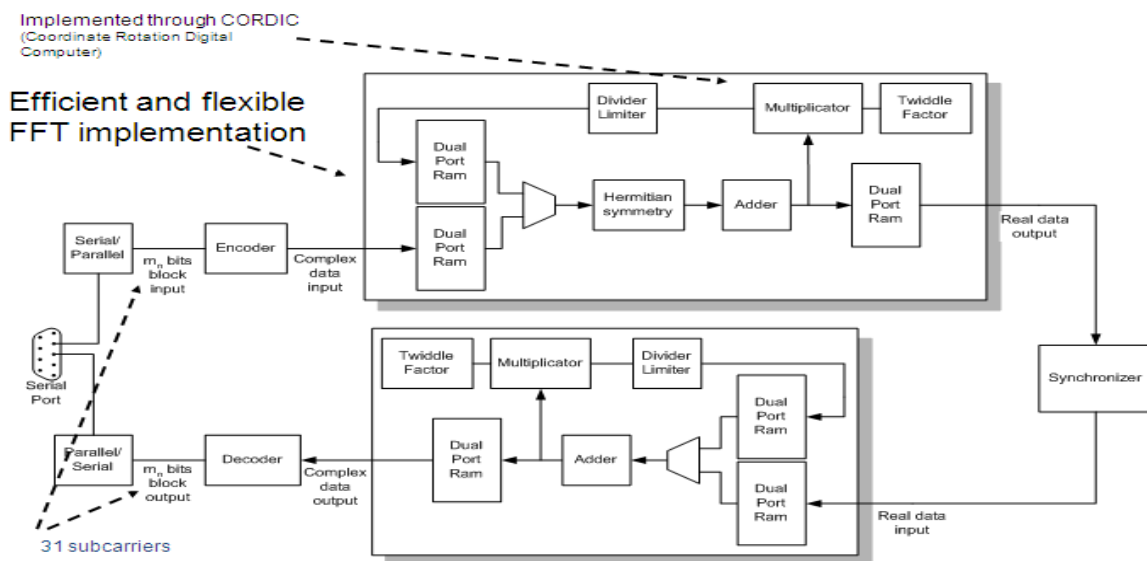


Fig. 2 Proposed System Block Diagram:

2) **The Design of Hermitian Symmetry:** After mapping of the N channels, we apply the Hermitian symmetry. The modulation can be done by an IFFT. If there are N channels, the Hermitian symmetry generates 2N + 2 channels in symmetry. At the receiver, after FFT processing, only the N channels are sent to the decoder, eliminating the channels generated due to the Hermitian symmetry.

3) **The Design of FFT/IFFT:** The modulation of MCM can be made through an IDFT. You can use the quick implementation of the IDFT by implementing the IFFT, shortening the design time and the hardware utilization. Demodulation can be made by the using DFT, or rather the FFT, and with their effective implementation.

The FFT computes the DFT with a large reduction in the number of operations, removing several existing redundancies in the calculation of the direct DFT. This efficiency is achieved at cost of an additional step to re-sort the data in order to determine the outcome end. This additional step, since it is effectively implemented, will not increase the computational complexity. As a result, the FFT is an extremely efficient algorithm that provides a good implementation in hardware.

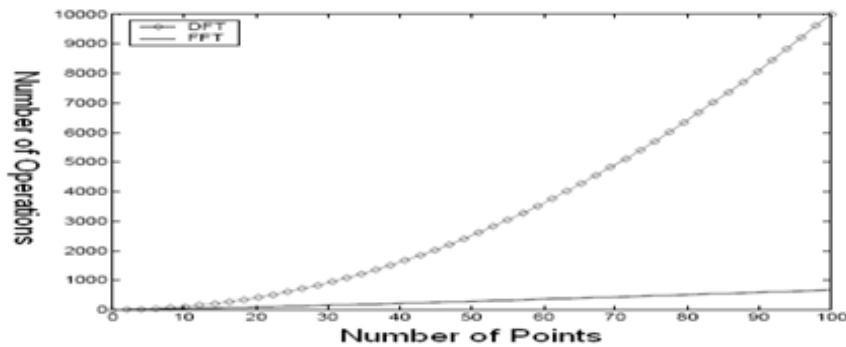


Fig. 3 Compression between DFT and FFT

4) **The Design of Butterfly Structures:** The most popular algorithms are the FFT radix-2 and radix-4. Radix-4 decimation in frequency based butterfly structure.

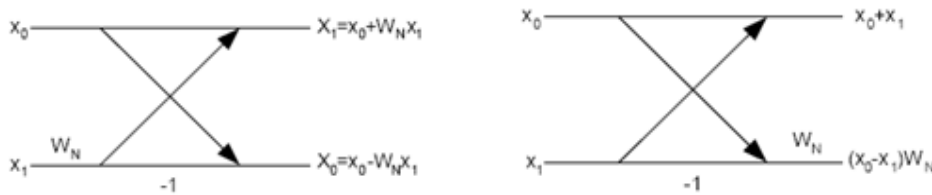


Fig. 4 Design of Butterfly Structures

In the FFT butterfly, the complex multiplication made between a complex number, (a + jb), and W_N^q

$$(a+jb)(\cos(2\pi\frac{q}{N})-j\sin(2\pi\frac{q}{N}))\dots\dots\dots(1)$$

$$(a\cos(2\pi\frac{q}{N})+b\sin(2\pi\frac{q}{N})+j(-a\sin(2\pi\frac{q}{N})+b\cos(2\pi\frac{q}{N})))\dots\dots\dots(2)$$

Similarly, in the IFFT, complex multiplications and made and the number of complexes are given by W_N^{-q} obtaining:

$$(a\cos(2\pi\frac{q}{N})-b\sin(2\pi\frac{q}{N})+j(a\sin(2\pi\frac{q}{N})+b\cos(2\pi\frac{q}{N})))\dots\dots\dots(3)$$

5) **The Design of CORDIC Pipeline:** Basically there are two methods to do the multiplication: store in a table the values of sine and cosine or calculate its value at the time through the CORDIC.

The CORDIC algorithm based multiplication is used .A way to implement the multiplications shown in equations (2) and (3) is by making use of CORDIC (Coordinate Rotation Digital Computer) based technique. The (2) can be rewritten as:

$$(R + j I) = (a \cos (2\pi \frac{q}{N}) + b \sin (2\pi \frac{q}{N}) + j (-a \sin (2\pi \frac{q}{N}) + b \cos (2\pi \frac{q}{N}))) \dots \dots \dots (4)$$

The (R +j I) term can be represented in matrix form, separating the real from the imaginary:

$$\begin{bmatrix} I \\ R \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} b \\ a \end{bmatrix} \dots \dots \dots (5)$$

Where $\theta = 2\pi \frac{q}{N}$

Similarly, the eqn(3) can be rewritten as:

$$(R + j I) = (a \cos (2\pi \frac{q}{N}) - b \sin (2\pi \frac{q}{N}) + j (a \sin(2\pi \frac{q}{N}) + b \cos(2\pi \frac{q}{N}))) \dots \dots \dots (6)$$

And can also be represented in matrix form:

$$\begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \dots \dots \dots (7)$$

Therefore we can consider the complex multiplications in equation (2) and equation (3) as a rotation of the angle of a + jb. The rotation of an angle θ can be performed in several steps, using a recursive method, in which each step is a small rotation of angle θ_n , which makes up the vector full rotation. The CORDIC uses this recursive procedure to make the rotation vector. Thus, you can only use rotation, adders/subtractors and comparators, which can be easily implemented in hardware. For this reason it can be implemented very efficiently in an FPGA. Isolating $\cos (\theta_n)$ rotation matrix in eqn (7), we get:

$$\cos \theta_n \begin{bmatrix} 1 & -\tan\theta_n \\ \tan\theta_n & 1 \end{bmatrix} \dots \dots \dots (8)$$

Making the angle of each step, θ_n , such that $\theta_n = \arctan(1/2^n)$, it is possible to replace the tangent of the rotation matrix in Equation(8) by a simple rotation operation to the right of the binary number, as it will be a power of 2.

The sum of all the steps of generating a rotation angle of rotation θ is given by:

$$\sum_{n=0}^{\infty} (S_n \theta_n) = \theta \dots \dots \dots (9)$$

Where, $S_n = \{-1, +1\}$, then we obtain

$$\tan\theta_n = S_n 2^{-n} \dots \dots \dots (10)$$

Applying Equation (10) in Equation (8), we obtain:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos\theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix} \dots \dots \dots (11)$$

Where, X_{n+1} and Y_{n+1} is the next step of X_n and Y_n , respectively. In Equation (11) there is still $\cos\theta_n$ left alone. The calculation will be iterated using several multiplications, which can be grouped as:

$$K = \frac{1}{P} = \prod_{n=0}^{\infty} \left(\cos(\arctan (\frac{1}{2^n})) \right) \dots \dots \dots (12)$$

Where, n is the number of iterations. Performing this calculation, it appears that from the 14th iteration, the value of K tends to remain a constant value, as shown in figure 5, which can be approximated to 0.6073. The value P will be approximately 1.6468. So, from that point we can replace the multiplication of several cosine terms Equation (12) by multiplication by a constant value of P, 1.6468.

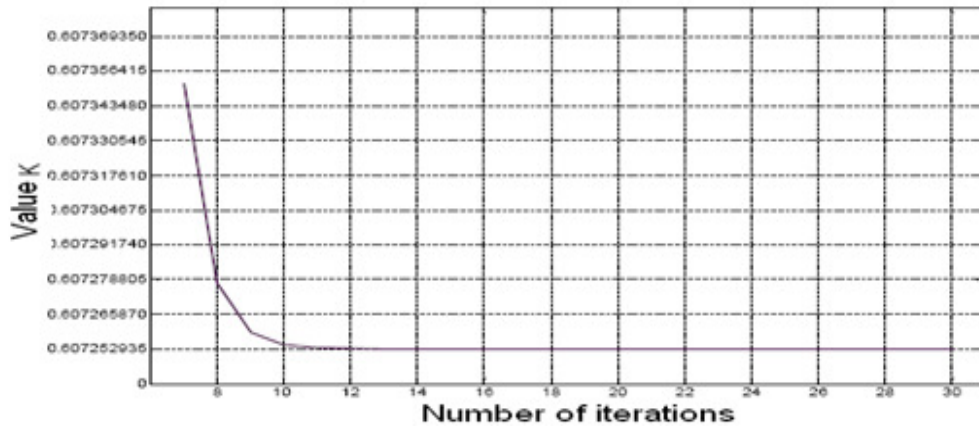


Fig. 5 the variations of value k with no. of iteration

3) **The Design of Radix-4 Butterfly:** In implementing radix-4, the basic block is a four-point butterfly as shown in fig. 6. It consists of four inputs and four outputs. Internally, it makes three complex multiplications and four complex additions.

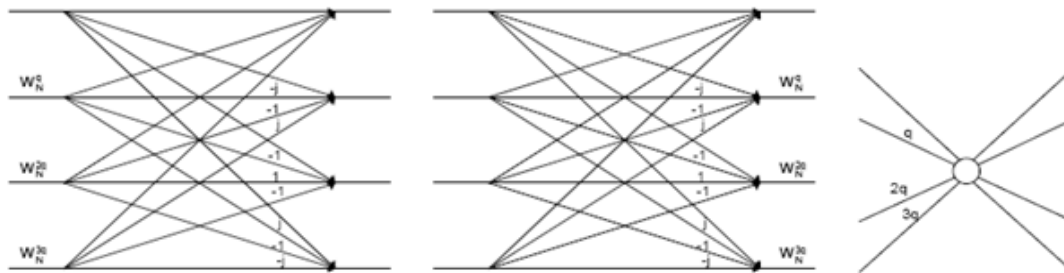


Fig. 6 Design of Radix-4 Butterfly

With the FFT using radix-4, it is shown that the calculation requires $(3N / 8) \log_2 N$ multiplications and $(3N / 2) \log_2 N$ complex additions. It is interesting to note that the sum of the butterfly is made in two steps, the number of items falls from 12 to 8. The number of complex additions gets reduced to $N \log_2 N$, which is identical to a radix-2 FFT. Therefore, with the radix-4 FFT, a 25% reduction in the number of complex multiplications is required, making the calculations much faster than radix-2 FFT.

6) **The Memory Usage:** Basically, the algorithm is to take the data of FFT/IFFT through the memory elements (4 memory elements considered for radix-4), do the butterfly calculations and then return the calculated data to the memory. Once the input data has already been processed by the butterfly, there is no more reason to guard them. So we can save the processed data in the same position of the same memory element. Thus, the amount of memory needed will be fixed. To solve the problem of cyclic-prefix, we can put output data to store in a RAM. So for the system to continue to function, we need the input memory to double its size and its contents separated into two parts, so that while reading the FFT, it should be possible to write in the other memory

and vice versa. Also, there is a need to add another RAM memory for later reading of the FFT data. This configuration is shown in Fig.7.

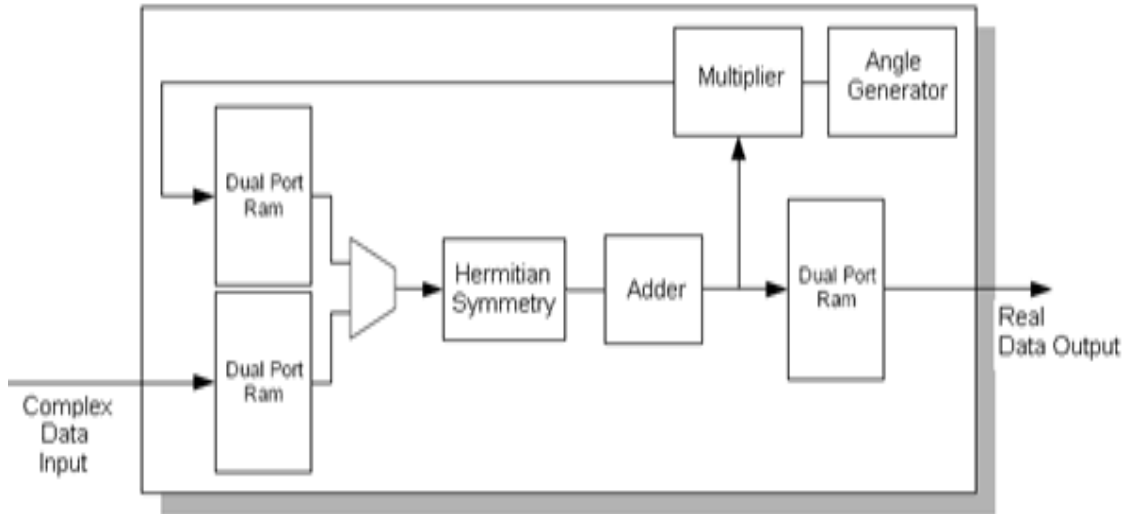


Fig. 7 Block Diagram of FFT Implementation Using 3 Rams

7) **Design of Cyclic-Prefix:** The inclusion of the cyclic-prefix at the transmitter is made very easily by parallel-serial converter. Just read the converter output bits that belong to cyclic-prefix two times and read the buffer RAM of the IFFT two times. The exclusion of the cyclic-prefix in the receiver is also made simple by simply removing the v bits that belongs to the cyclic-prefix during the FFT operation.

IV. DESIGN OF OFDM TRANSMITTER AND RECEIVER

1) OFDM TX:

The serial to parallel converter receives the M -serial bits to be transmitted and divides into N sub-blocks of m_n bits each, which are then mapped by the encoder at a point as $a_n + jb_n$ in the constellation of the modulator. It is Important to note that this mapping is done only by converting the bits in to the phase it represents. The modulation is not made at this time as in the case of QAM. For this, as we have seen in the IFFT, after mapping the N channels, and then applying the hermetian symmetry, $2N + 2$ channel complex symmetry is generated. The IFFT receives the $2N + 2$ channel complex symmetry generated by the hermetian symmetry and then does the modulation. At the end of IFFT processing, the output will only be the real part of the numbers. The parallel to serial converter serializes the data, however it serializes v twice for the same outputs of the IFFT, thus adding the cyclic-prefix, and generating $2N + 2 + v$ words to be converted to analog signal by using digital to analog converter. Note that the inclusion of the cyclic-prefix is made very easily by using parallel to serial converter.

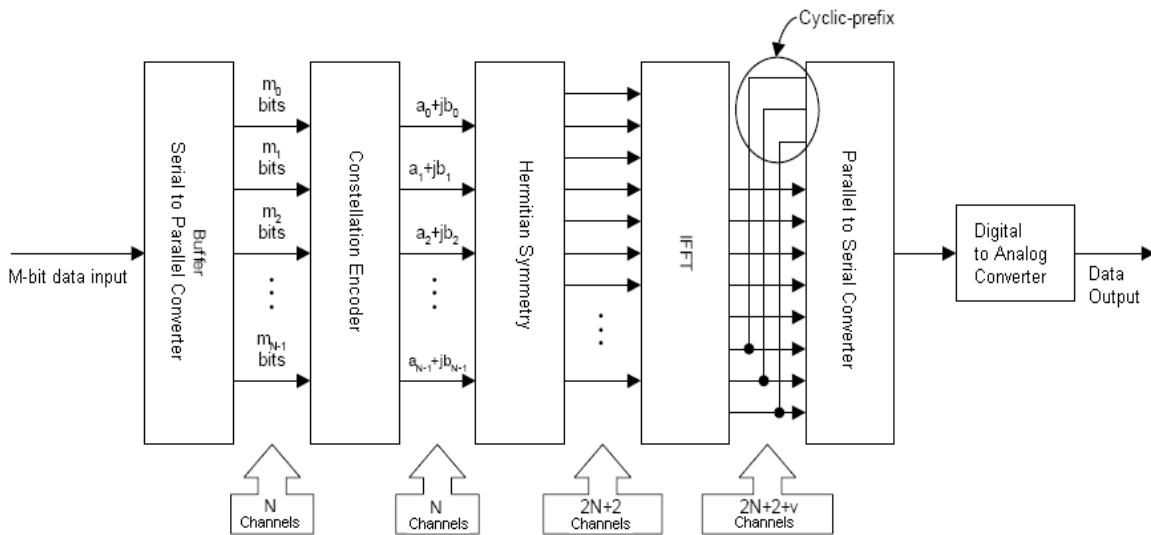


Fig. 8 OFDM Transmitter Module

2) **OFDM RX:**

In this system the analog-digital converter samples the signal from the channel, generating $2N + 2 + v$ serial samples. So the serial to parallel converter generates $2N + 2 + v$ parallel channels. The FFT receives only $2N + 2$ real channels, thus eliminating the v channels generated due to the cyclic-prefix. The FFT also demodulates the signal generating $2N + 2$ complex outputs. After FFT processing, the bits are sent to only N -channel complex decoder, eliminating the channels of hermitian symmetry in the same way that eliminated the cyclic-prefix. The decoder makes the decision about the binary sequence that represents the received signal and then again generates the block of M -bits that are transmitted.

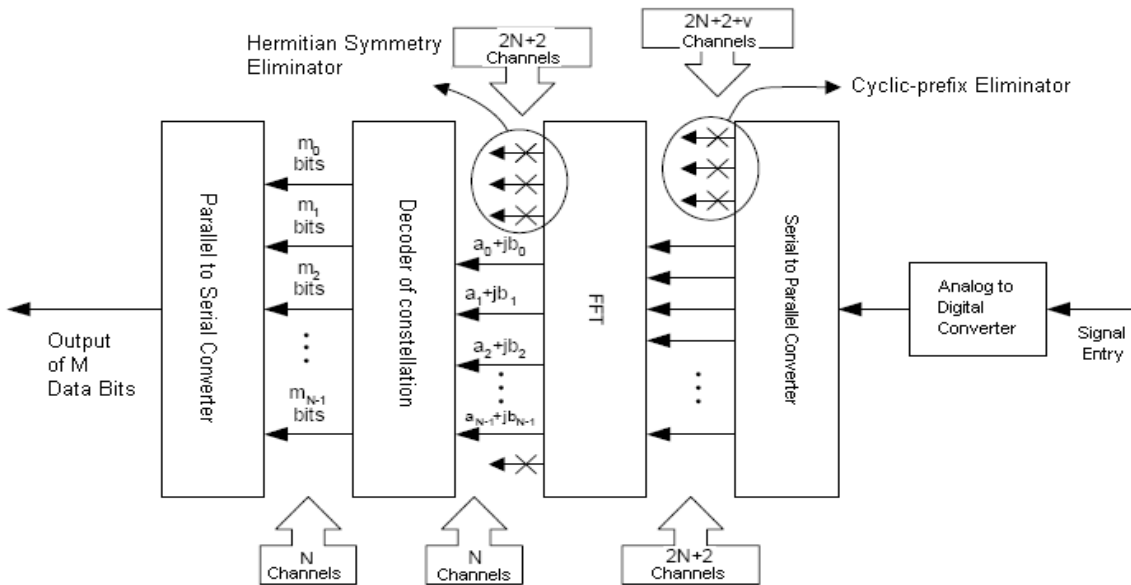


Fig. 9 OFDM Receiver Module

V. RESULTS AND DISCUSSION

The synthesis of OFDM Modem core was performed using Xilinx ISE software and the results are as shown below. Fig. 10 shows the synthesis results of OFDM MODEM top module. The OFDM modem consists of TXMODEM, TXRX and RXMODEM modules is as shown in figure 11.

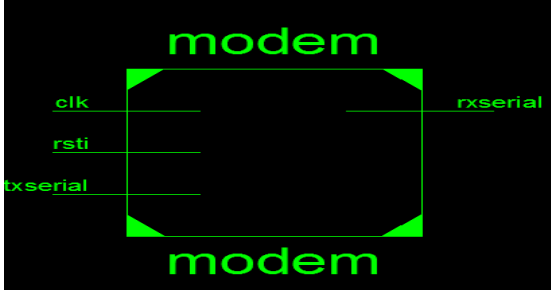


Fig. 10 OFDM Modem Top Module

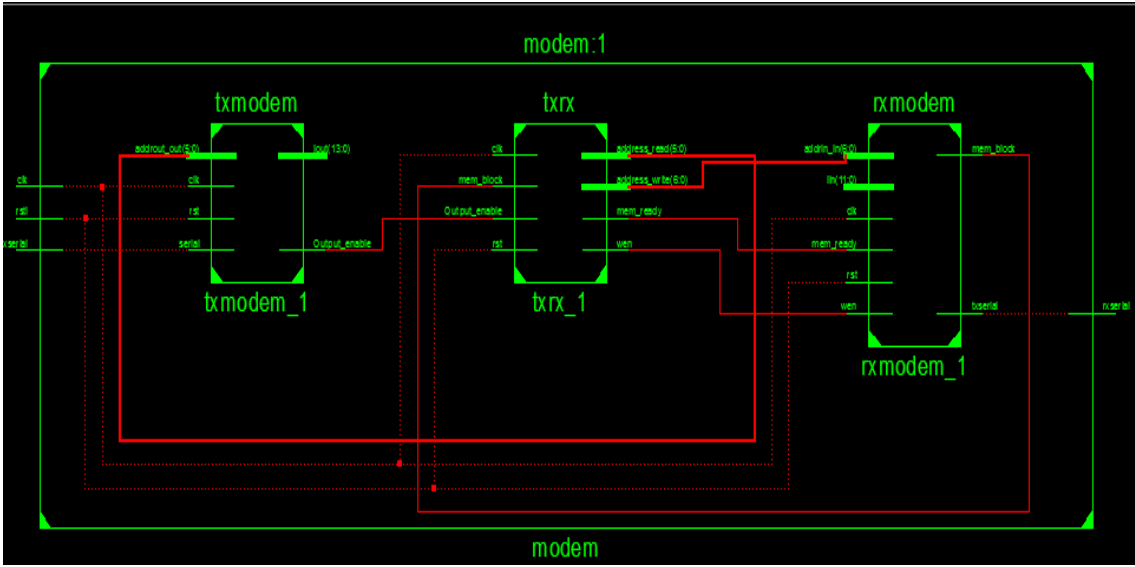


Fig. 11 OFDM Modem consisting of TXMODEM, TXRX Interface and RXMODEM modules

1) Results of OFDM modem top module

When the reset pin (rsti) = '1' and when txserial, which is the serial input pin = '1', then rxserial, which is the output of the receiver module = '1'. This is shown in figure 12. At these time instants, the outputs of IFFT module that is the iin pins are also zeros.

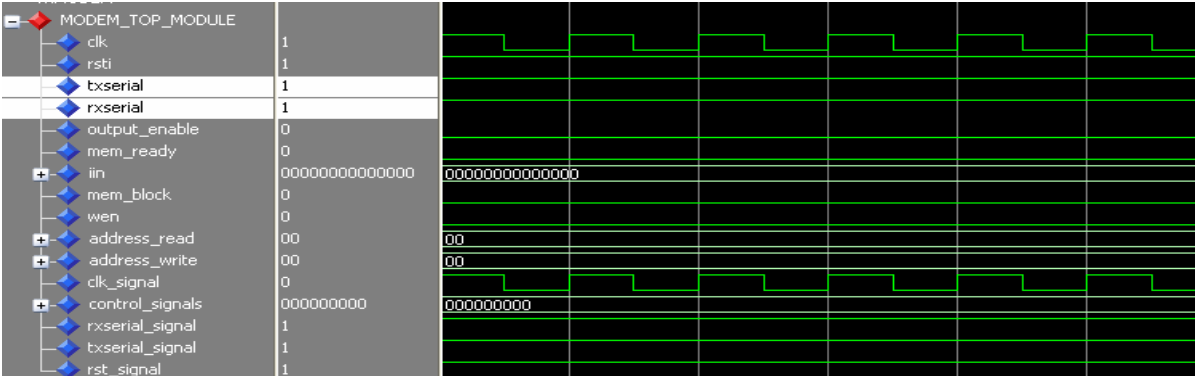


Fig. 12 Simulation Results of OFDM Modem Top module when rsti = '1'

In fig. 13, when reset pin, rsti = '0', and when txserial is made '0', then IFFT in transmitter and FFT in receiver starts processing data. The output enable starts sending small pulses to indicate that the output is valid at those time instances. The iin signals also start changing. Note that the rxserial pin becomes '0', which is the output of the receiver.

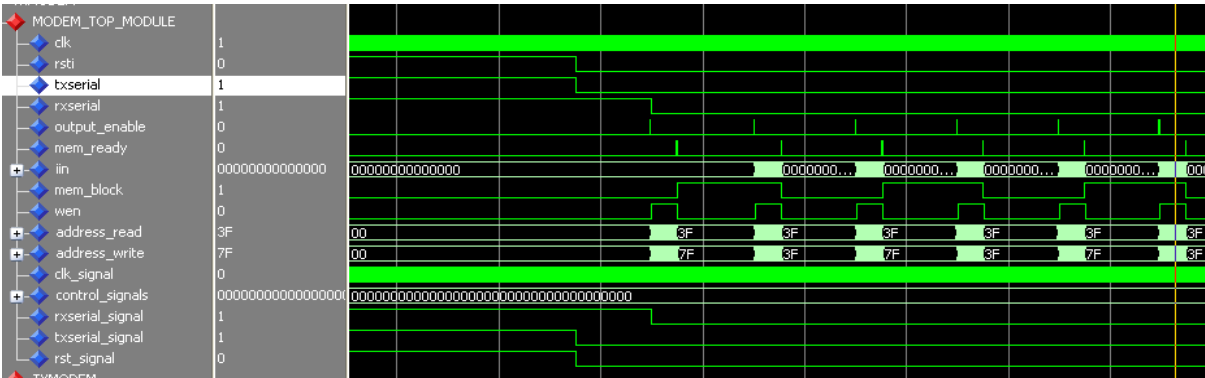


Fig. 13 Simulation Results of OFDM Modem Top module when rsti = '0'

In fig. 14, the input data, txserial = '1' and after several clock cycles, the receiver output, rxserial becomes '1'

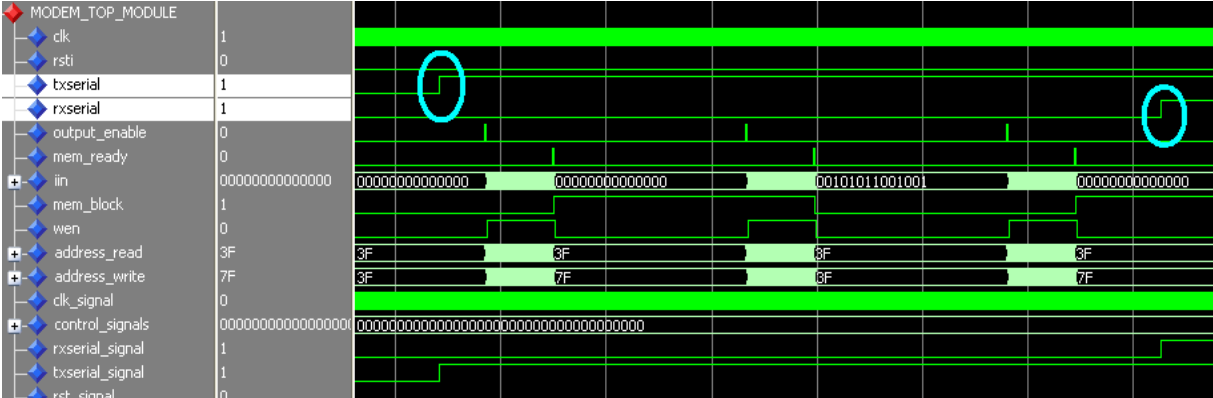


Fig. 14 Simulation Results of OFDM Modem Top module if txserial = '1'

2) **Results of TXSERIAL module**

In fig. 15, the input data, serial = ‘0’ and rst = ‘0’. The IFFT in transmitter does the processing of data and hence there are changes in iout signals. The output_enable signal has pulses of small time durations, indicating that the value on iout signals are valid at those time instants. The mem_block signal keeps changing with respect to time. When mem_block is ‘0’, then the one of the RAM at the input side is selected and if mem_block is ‘1’, then the other RAM at the input side is selected. Note that I and Q output signals of 4-QAM modulator are “000010000000” respectively if serial signal is ‘0’.

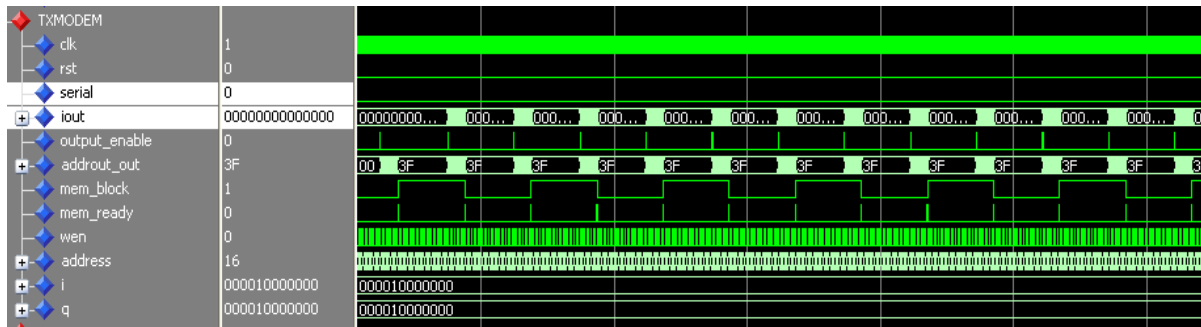


Fig. 15 Simulation Results of TXSERIAL Module when input serial is ‘0’

In fig. 16, the input data, serial = ‘1’ and rst = ‘0’. The IFFT in transmitter does the processing of data and hence there are changes in iout signals. The output enable signal has pulses of small time durations, indicating that the value on iout signals are valid at those time instants. Note that I and Q output signals of 4-QAM modulator are “110100000000” respectively if serial signal is ‘1’.

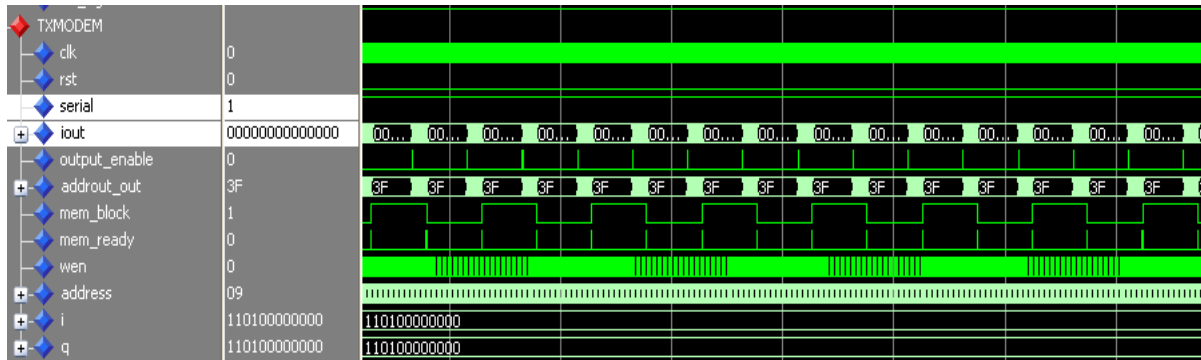


Fig. 16 Simulation Results of TXSERIAL Module when input serial is ‘1’

3) **Results of TXMODEM module**

In fig. 17, the input data, serial = ‘1’ and rst = ‘0’. The IFFT in transmitter does the processing of data and hence there are changes in iout signals. The output_enable signal has pulses of small time durations, indicating that the value on iout signals are valid at those time instants. The waveform shown is zoomed in to indicate that the outputs of iout has 64 variations with respect to time, indicating that the IFFT/FFT does the 64 point transform

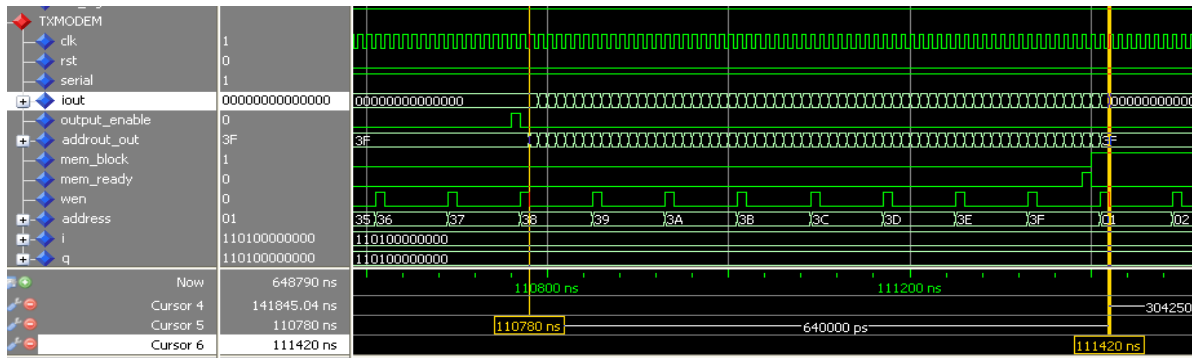


Fig. 17 Simulation Results of TXMODEM Module when input serial is ‘1’

4) Results of INPUT module

In fig.18, the input data, serial is changed from ‘0’ to ‘1’. Since this module is a 4-QAM modulator, note that the outputs I and Q are “000010000000” when serial signal is ‘0’ and I and Q are “110100000000” when serial signal is ‘1’



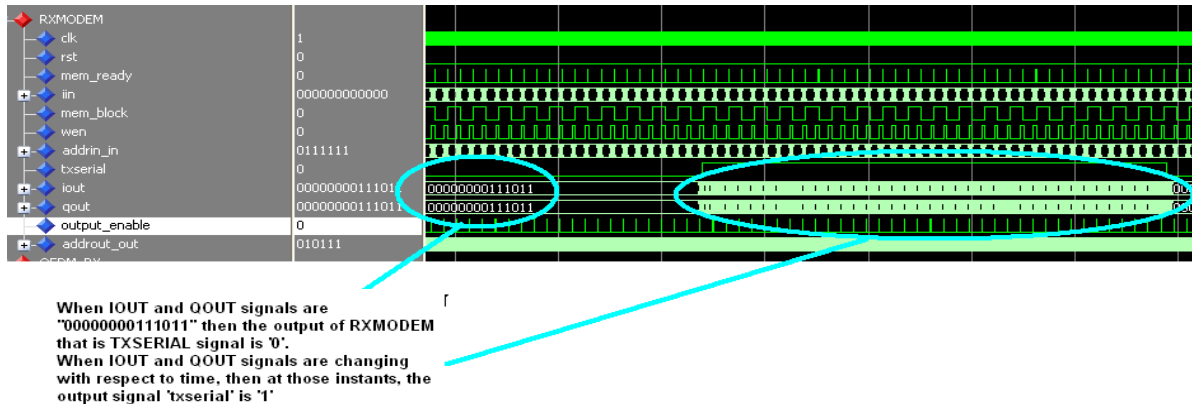
WHEN TXSERIAL IS '0' I AND Q ARE "000010000000"

WHEN TXSERIAL IS '1' THEN I AND Q ARE "110100000000"

Fig. 18 Simulation Results of INPUT module (4-QAM modulator)

5) Results of RXMODEM module

In Fig. 19, when IOUT and QOUT signals are “00000000111011” then the output of RXMODEM, that is, the TXSERIAL signal is ‘0’. When IOUT and QOUT signals are changing with respect to time, then at those instants, the output signal, TXSERIAL is ‘1’.



When IOUT and QOUT signals are "00000000111011" then the output of RXMODEM that is TXSERIAL signal is '0'. When IOUT and QOUT signals are changing with respect to time, then at those instants, the output signal 'txserial' is '1'

Fig. 19 Simulation Results of RXMODEM module

VI. CONCLUSION

The OFDM modem core has been successfully designed, OFDM transmitter chain as well as OFDM receiver chain has been successfully implemented using a single FPGA. The Inverse Fast Fourier Transform (IFFT) in OFDM transmitter and Fast Fourier Transform (FFT) in OFDM receiver module have been implemented. The FFT/IFFT has been chosen in the design instead of the Discrete Fourier Transform and Inverse Discrete Fourier Transform because they offer better speed with less computational time.

The whole OFDM modem design has been carried out using VHDL coding. Direct mathematical method is adopted in the design of FFT/IFFT because it is an efficient and optimized method instead of the structural implementation which is based on butterfly operation. The OFDM core is Compile time configurable. That is the width, points and stages of OFDM can be configurable and there is no limitation (except for the device logic utilization). The OFDM core has designed considering very less latency. Transmitter latency measured to be 4.59us and Receiver latency measured to be 2.25us. OFDM has been designed by considering 31 orthogonal sub-carriers and it is synthesized to 157.3MHz external clock frequency. OFDM has inbuilt Serial-to-parallel converter and Parallel-to-serial converter, thus the core can be directly connected to serial ports. It has lot of advantages when compared with Xilinx Coregen FFT core.

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