STATE-OF-THE-ART DEVELOPMENTS IN ACCELERATOR CONTROLS AT THE APS *

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Abstract

The performance requirements of the Advanced Photon Source (APS) challenge the control system in a number of areas. This paper will review a few applications of advanced technology in the control and monitoring of the APS. The application of digital signal processors (DSPs) and techniques will be discussed, both from the perspective of a large distributed multiprocessor system and from that of embedded systems. In particular, two embedded applications will be highlighted, a beam position monitor processor and a DSP-based power supply controller. Fast data distribution is often a requirement. The application of a high-speed network based on reflective memory will also be discussed in the context of the APS global orbit feedback system. Timing systems provide opportunities to apply technologies such as high-speed logic and fiber optics. Examples of the use of these technologies will also be included. Finally, every modern accelerator control system of any size requires networking. Features of the APS accelerator controls network will be discussed.

1 INTRODUCTION

It is not without some measure of trepidation that the author attempts to address a topic such as "state-of–the-art" developments in accelerator controls at the APS. Such a term tends to inspire anticipation of revelations of completely new and previously unknown applications of technology. Such revelations are a rarity, and this paper does not aspire to such a lofty level. Rather, the author views this as an opportunity to introduce the reader to a sampling of what are hoped to be interesting applications at the APS of currently available technology.

The applications discussed cover three broad areas: digital signal processing and processors, networks, and fast logic.

2 FAST ORBIT FEEDBACK SYSTEM

The APS fast orbit feedback system has been in routine operation with users since June of 1997. Reference [1] contains an extensive description of the details of this system.

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2.1 Overview

The fast orbit feedback system consists of 21 VME crates, (1 master and 20 slaves), distributed around the 1104-m-circumference storage ring. Each crate contains a 68040-based processor running EPICS control software. This processor serves as an interface to the control system and two DSP cards, a Pentek [2] 4284 and a Pentek 4283. The 4284 uses the TI C40 DSP chip and computes vertical orbit corrections, while the 4283 uses the TI C30 chip and computes horizontal corrections. A reflective memory network (discussed later in this paper) is used to distribute data and control information between VME nodes.

Each VME slave node has a direct digital data feed of BPM position data from the rf BPM system [3]. In addition, position data is received from beamline x-ray BPMs and narrow-band rf BPMs [4] straddling each insertion device via VME interface cards located in each node. As this paper is written, these BPMs have not been integrated into the fast orbit feedback system. However, the position data from the x-ray BPMs and the narrow-band rf BPMs is available to the control system through the EPICS processor.

Since the last report [1], the feedback system sampling rate has been increased to 1.67 kHz. Orbit corrections are synchronously computed and corrector values written at the sampling rate. The correction algorithm corrects global orbit errors in an rms sense using 160 BPMs and 38 "fast" correctors in each plane. A high-pass digital filter rolls off frequency response below 100 mHz. Low frequency orbit correction to DC and local steering is handled by a workstation-based program [5] running at 0.5 Hz.

2.2 Performance

Table 1 summarizes performance. Quoted orbit motion is from the latest available data with 1% x-y coupling.

Table 1: Fast Orbit Feedback Performance

	Horizontal (rms)		Vertical (rms)	
	F/B off	F/B on	F/B off	F/B on
Required Orbit stability (with 10% coupling)	17.5 μm		4.5 μm	
Motion 0.016-30 Hz	18.4 μm	3.4 μm	3.1 μm	1.4 μm
Motion 0.25-800 Hz	20.8 μm	13.5 μm	8.0 μm	7.0 μm
β at ID source points	17 m		3 m	

DISCLAIMER

2.3 *Future Development*

Future upgrade plans include integrating the narrow-band rf BPMs and the x-ray BPMs into the fast orbit correction algorithm. In addition, the Pentek boards allow the addition of daughter card DSPs. We plan to add daughter cards to each DSP card. The additional DSP power will allow implementation of more sophisticated regulators and local control at each storage ring insertion device. Presently we do not plan to increase the total number of BPMs used in the correction algorithm. The time to read in the error vectors over VME consumes a significant part of each sample interval. Decreasing this time would require replacing the 4283 DSP boards, which would be a significant expense.

3 REFLECTIVE MEMORY

Reflective memory is a commercially available technology that is a critical component of the fast orbit feedback system. It may even be considered an enabling technology. It is available from at least two vendors that the author is aware of, VMIC [6] and Systran [7].

3.1 *Description*

Reflective memory may be defined as a network of replicated, shared memory. A reflective memory card is located in each node participating in the network. The card appears as random-access memory (RAM) to the node's system bus. Any processor on the system bus (in our case VME) can write or read the reflective memory. The reflective memories are connected head to tail in a ring. When a value is written to a location, that value and its RAM address are transmitted around the ring. Each reflective memory deposits the value into the same address in its RAM. The originating node strips the message from the ring when it is received. Through this mechanism, the RAM image is replicated in each reflective memory participating in the ring. Thus, after a message transit time, each node sees an identical, replicated image of RAM. Figures 1 and 2 illustrate the process.

The VMIC VMIVME-5588DMA, which is used in the fast orbit feedback system, sends and receives data over a 1.2-Gbaud serial fiber optic ring. The actual specified data transmission rate is 29.5 Mbytes/s. A maximum of 256 nodes is allowed; the fast orbit feedback system has 21 nodes. When multimode fiber is used, nodes may be located up to 1 km apart (10 km node spacing is specified with single mode fiber). Memory sizes up to 16 Mbytes are available.

A very attractive feature of reflective memory networks is that they do not require processor involvement in network initialization or management. They are treated as RAM. To communicate values to all nodes in the ring, the values are merely written to reflective memory. The reflective memory hardware

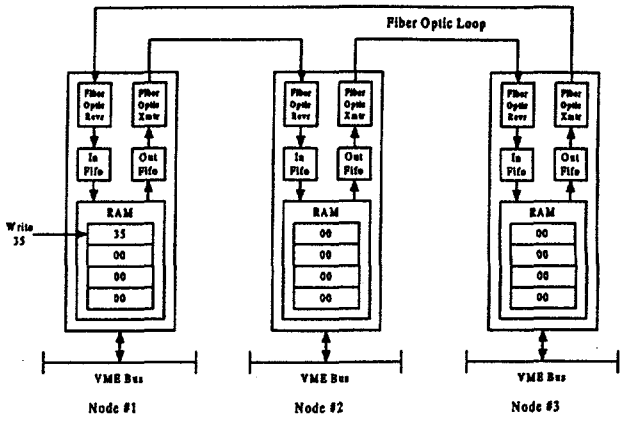

Figure 1: Write to a reflective memory.

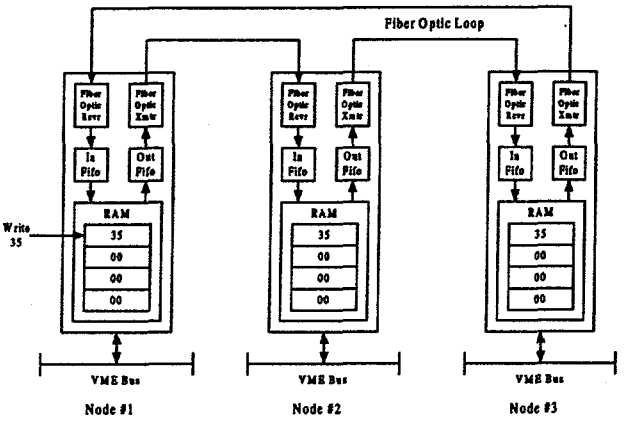

Figure 2: Replication of reflective memory contents.

handles the actual transfer. In addition, the reflective memory network is deterministic as long as the network bandwidth limits are observed. Error detection is provided and corrupted messages are discarded.

3.2 *Application*

The reflective memory is used to communicate data and control information between the nodes of the fast orbit feedback system. At every feedback 1.67-MHz clock tick, each DSP reads BPM data from sectors within its span of control, computes error values, and deposits the result into assigned locations within an error vector located in reflective memory. In addition, each DSP sets a flag in a "done" vector in reflective memory. All DSPs monitor the done vector. When the done vector is complete, all DSPs read the complete error vector and compute corrector error values.

The reflective memory is also used to communicate control information from the master node to the slaves. Parameters such as filter coefficients and controls such as loop on/off are deposited in specific locations in reflective memory by the master node. Slave nodes read new values upon command.

Each DSP deposits into reflective memory additional information such as position data and corrector error

values. The DSPs in the master node can access this data through a 40-channel digital scope feature. This has proven to be a powerful diagnostic tool for determining causes of unwanted beam motion and beam loss.

Reflective memory is an interesting alternative for data communication in any distributed control application.

4 POWER SUPPLY CONTROLLER

The APS has initiated the development of a new power supply controller for the storage ring power supplies. The storage ring uses 1400 power converters, one for each magnet (other than the main dipole bus). The present system uses an analog regulator with control and monitoring performed by a single G64-based 68000 processor per converter cabinet. Each cabinet contains up to eight power converters. BitBus is used to subnet the 68000s to the control system. While this system has served the APS well, its limited power both in computing resources and network performance has limited the tasks that can be accomplished.

A new controller based on DSPs and Ethernet is under development. A single SHARC [8] DSP is used.

4.1 Goals

Primary goals of the new design are:

1. Provide glitch detection to aid the analysis of beam loss events.
2. Provide 18-bit settability for power converters (specifically required for the correctors to meet long-term APS orbit stability goals).

Additional expected benefits are:

1. Fast data collection and anomaly detection (detect noisy converters).
2. Improved power converter dynamic stability.
3. Reduced likelihood of power converter glitches due to replacement of the analog regulator with a digital implementation.
4. Improved reliability and maintainability through a reduction in the number of cables and connectors.

4.2 Implementation

Figure 3 shows the block diagram of the regulator design. A SHARC DSP will implement the digital regulator. The power circuit input voltage and the magnet current are digitized by a pair of 16-bit ADCs. An 18-bit pulse width modulator (PWM) drives the power circuit insulated gate bipolar transistor (IGBT) switches. On-board flash memory stores code and parameters. Communications to a control system processor is via an on-board Ethernet interface.

The control algorithm is implemented in the SHARC. An external 20-kHz clock triggers the PWM and initiates a DSP control cycle. Sets of regulators will be driven by different phases of the 20 kHz to distribute the load presented to the raw supply. Snapshot waveform storage of voltage or current samples will be stored in the SHARC internal RAM and will be accessible to the control system through the network interface. Performance measures such as mean absolute deviation (MAD) and variance will be computed at the 20-kHz rate. Output current glitch detection will be based on MAD exceeding a specified threshold. A continuous circular buffer of measured current will be maintained. Glitch detection will stop the circular buffer a specified number of samples after the glitch. Through this mechanism, the output current both pre- and post-glitch will be recorded.

Glitch detection will be an important new feature in that it will help determine which of the many converters caused a beam dump.

4.3 Status

A VME-based prototype is nearing completion and should be under test at the time of this publication. VME was chosen as the prototype platform because of its modularity. Each major function—DSP, ADC, PWM, network, etc.—is implemented on a separate VME card. This allows replacement of a function without replicating the entire circuit. The final design is expected to be a single board to maximize reliability and minimize cost.

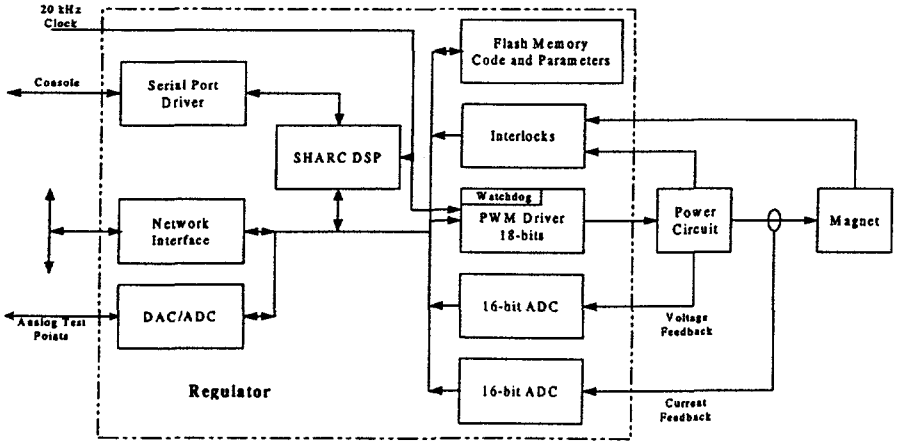

Figure 3: DSP-based power supply regulator.

5 BUNCH CURRENT MONITOR

A bunch current monitor capable of simultaneously measuring the current in every bunch in the ring has been in operation for nearly one year. Figure 4 shows a block diagram. The sum signal from a storage ring strip line is digitized by a high speed 8-bit ADC manufactured by Celerity Systems [9]. The digitizer is driven by an external clock and an external trigger. The storage ring rf, 352 MHz, is used as an external clock input. The storage ring revolution clock is used as an external trigger. Once the digitizer is triggered, it digitizes the input signal at the 352-MHz rate. Digitized values are stored in a 64-kbyte FIFO and read out to VME. Using the storage ring clock as the digitizer's clock input ensures that the digitization process is synchronous with the bunch train.

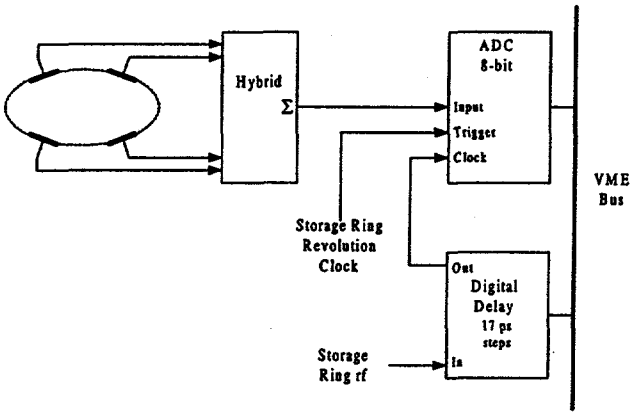

Figure 4: Bunch current monitor.

The storage ring rf is passed through a programmable digital delay with a resolution of 17 ps per step. This delay allows the digitizer to be timed to the input bunch train. Up to 48 consecutive turns of data may be digitized in one pass. The 48 turns of data are averaged to reduce the measurement's variance.

The digitizer has a peculiarity due to its design. It exhibits up to an 8-channel uncertainty between the trigger input and the location in the FIFO of the digitized value corresponding to the trigger time; i.e., the position of the beginning of the bunch train within the record has up to an 8-channel uncertainty. All our storage ring fill patterns place charge in bucket zero. The software searches for the first non-zero value over a limited range of the digitized record to find bunch zero. All further processing is then relative to the position determined to be bunch zero. At normal operating levels, the raw resolution of the digitizer is about 0.037 mA/bit. With averaging of 48 turns, the rms error is less than 0.010 mA.

The bunch current monitor plays a crucial role in storage ring top-up mode. In top-up mode, additional charge is injected into the storage ring at short time intervals (2 minutes) to counteract beam decay due to lifetime. The bunch current monitor output is used to determine which bunch(es) have the least charge. Those bunches are then targeted for injection.

6 BPM PROCESSOR

The existing rf BPM system [3] uses a module known as a memory scanner that applies a boxcar filter to BPM data collected from the BPM digitizers. It is believed that BPM data quality can be enhanced by applying DSP techniques to improve AC performance of the filter. A drop-in replacement is being designed at this time.

The new memory scanner will be a VXI module with six SHARC DSPs connected as a multiprocessor cluster [10]. The SHARC has features that facilitate multiprocessor configurations. BPM x, y and sum values from nine BPM digitizers (one sector's worth) will be available to the module via the VXI local bus. The digitizers alternate between x and y digitizations on every other turn. The incoming data rate will be 2.4 Msamples per second (nine 'x' or nine 'y' values times 270 kHz revolution rate). The board will provide three basic functions:

1. Low pass filtering through multistage decimation filters.
2. BPM beam history storage.
3. Fast Fourier transform (FFT)-based calculations

A 300-Hz low pass filter will provide BPM data to the fast orbit feedback system. Filters with cutoff frequencies in the few Hertz range will provide BPM data to the control system. Other cutoff frequencies may also be implemented depending on future requirements. The beam history function will use an 8-Mbyte RAM to store temporal BPM data as fast as turn by turn. Allocation of RAM to the BPM data sources will be configurable under software control. FFT based calculations, such as power spectral density, will be supported onboard.

One of the six DSPs will be the master, and the remaining five DSPs will serve as compute engines. The master will control slave operation; manage the beam history RAM; and manage the interfaces to the VXI bus, VXI local bus, and the fast orbit feedback system. Presently it is felt that three of the DSPs will be sufficient to perform all low pass filtering requirements. The remaining two slave DSPs will be available for FFT and statistical data computations.

7 TIMING

7.1 Fast Logic

Several digital logic modules have been designed at the APS that operate synchronously at the storage ring rf of 352 MHz [11]. We recently designed a digital divider based on the ECLinPS [12] family of emitter coupled logic (ECL). This circuit divides the 2.865-GHz linac rf by 24 to produce a 119-MHz signal that is used as a reference for a laser driving a photocathode electron gun

and as a sweep input to a streak camera. The circuit is housed on a small daughter card that is mounted on a VME base board. VME is used merely as a convenience, i.e., there are no programmable functions.

7.2 Low-Cost 352-MHz Distribution

Bunch clock generators [13] are in the process of being installed on multiple beamlines. These modules provide beamlines with timing pulses coincident with stored bunches. Each module requires a 352-MHz storage ring rf reference. In the few installations completed to date, single-mode fiber with single-mode fiber optic transmitters and receivers have been used to distribute the 352-MHz reference.

Single-mode fiber optic transmitters and receivers are costly. It was felt that not all beamlines would demand the low jitter performance achieved with the single-mode components. Thus, we devised a lower cost scheme, shown in Figure 5, that permits the use of inexpensive multimode fiber optic components to distribute the 352-MHz to those beamlines that can tolerate a somewhat higher jitter. The method divides down the 352 MHz to a frequency that can be easily handled by the multimode components. In our case we digitally divide the 352 MHz by 8 and transmit the resulting 44 MHz. At each receiving beamline, the 44 MHz is fed into a phase-locked loop that multiplies the 44 MHz by 8 to reconstruct a 352-MHz reference.

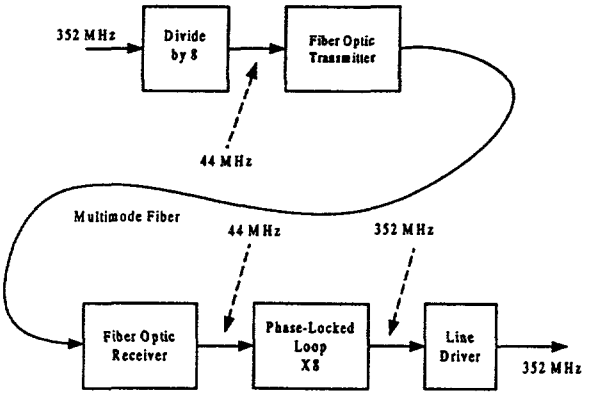

Figure 5: 352-MHz distribution over multimode fiber.

We chose a part manufactured by Micro Networks [14]. With this scheme, we achieve peak-to-peak jitter of 50 ps (rms of 7 ps) over 625 m of multimode fiber. One system has been in use for about six months. We are in the process of installing additional systems.

8 NETWORK

The APS controls network has previously been described [15]. At that time, the network was based on hubs, FDDI, and 10-Mbit fiber Ethernet. We are now in the midst of a major network upgrade. Existing FDDI links will be replaced with 1-Gbit Ethernet. The central enterprise FDDI hub will be replaced with a Gbit Ethernet switch featuring better than a 30-Gbit/s backplane fabric. The existing remote hubs, which are combination repeaters and blocking switches, will be replaced with fully switched 10/100 Ethernet switches with backplane fabrics in excess of 20 Gbits/s. The remote hubs will connect to the central switch via dual 1-Gbit Ethernet uplinks. Redundancy will be maintained from the IOCs up through the central switch and file servers. The servers and operator interface workstations will attach to the central switch through either Gbit or fast Ethernet.

All our existing IOCs use 10BaseFX. We will, however, be upgrading selected IOC processors to PowerPC-based units with 100BaseTX. Dual redundant 100BaseFX transceivers will connect these processors to two independent remote switches.

This upgrade will significantly increase total network bandwidth and eliminate over subscription at the remote hubs.

9 ACKNOWLEDGEMENTS

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